# R.V. COLLEGE OF ENGINEERING

**(Autonomous Institution Affiliated to VTU, Belagavi)**

**R.V. Vidyaniketan Post, Mysore Road**

**Bengaluru – 560 059**


## Bachelor of Engineering (B.E.)

## Scheme and Syllabus for V & VI Semesters

# 2016 SCHEME

# ELECTRONICS & COMMUNICATION ENGINEERING

## Department Vision

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering.

## Department Mission

- To impart quality technical education to produce industry-ready engineers with a research outlook.
- To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.
- To create centres of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.
- To develop entrepreneurial skills among the graduates to create new employment opportunities.

## PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

**PEO1.** To apply concepts of mathematics, science and computing to Electronics and Communication Engineering

**PEO2.** To design and develop interdisciplinary and innovative systems.

**PEO3.** To inculcate effective communication skills, team work, ethics, leadership in preparation for a successful career in industry and R & D organizations.

## PROGRAM SPECIFIC OUTCOMES (PSOs)

| PSO | Description |
|---|---|
| PSO1 | Should be able to clearly understand the concepts and applications in the field of Communication/networking, signal processing, embedded systems and semiconductor technology. |
| PSO2 | Should be able to associate the learning from the courses related to Microelectronics, Signal processing, Microcomputers, Embedded and Communication Systems to arrive at solutions to real world problems. |
| PSO3 | Should have the capability to comprehend the technological advancements in the usage of modern design tools to analyze and design subsystems/processes for a variety of applications. |
| PSO4 | Should possess the skills to communicate in both oral and written forms, the work already done and the future plans with necessary road maps, demonstrating the practice of professional ethics and the concerns for societal and environmental wellbeing. |

Lead Society: Institute of Electrical and Electronics Engineers (IEEE)

# PROGRAM OUTCOMES (POs)

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialisation for the solution of complex engineering problems.

2. **Problem analysis:** Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet t h e specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling to complex engineering activities, with an understanding of the limitations.

6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with t h e society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning:** Recognise the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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## Bachelor of Engineering (B.E.)
## Scheme and Syllabus for V & VI Semesters

# 2016 SCHEME

# ELECTRONICS & COMMUNICATION ENGINEERING

# Abbreviations

| Sl. No. | Abbreviation | Meaning |
|---|---|---|
| 1. | **VTU** | Visvesvaraya Technological University |
| 2. | **BS** | Basic Sciences |
| 3. | **CIE** | Continuous Internal Evaluation |
| 4. | **CS** | Computer Science and Engineering |
| 5. | **CV** | Civil Engineering |
| 6. | **CHY** | Chemistry |
| 7. | **EC** | Electronics and Communication Engineering |
| 8. | **EE** | Electrical and Electronics Engineering |
| 9. | **ES** | Engineering Science |
| 10. | **HSS** | Humanities and Social Sciences |
| 11. | **ME** | Mechanical Engineering |
| 12. | **PHY** | Engineering Physics |
| 13. | **SEE** | Semester End Examination |
| 14. | **MAT** | Engineering Mathematics |

# INDEX

| VI Sem | | | |
|---|---|---|---|
| **Sl. No.** | **Course Code** | **Name of the Course** | **Page No.** |
| 1. | 16HEM61 | Foundations of Management & Economics | |
| 2. | 16EC62 | Communication System II | |
| 3. | 16EC63 | Computer Communication Networks | |
| 4. | 16EC64 | Analog & Mixed Signal IC Design | |
| 5. | 16EC6C1 | Cryptography & Network Security | |
| 6. | 16EC6C2 | Real Time Embedded Systems | |
| 7. | 16EC6C3 | Image Processing | |
| 8. | 16EC6C4 | Low power VLSI Design | |
| 9. | 16EC6C5 | Data structure using C++ | |
| 10. | 16EC6C6 | System Programming & Software | |
| 11. | 16EC6C7 | Flexible Electronics | |
| 12. | 16EC6D1 | Optical Fiber Communication & Networks | |
| 13. | 16EC6D2 | ARM Cortex Processors | |
| 14. | 16EC6D3 | Adaptive Signal Processing | |
| 15. | 16EC6D4 | System Verilog | |
| 16. | 16EC6D5 | Algorithm for VLSI Design Automation | |
| 17. | 16EC6D6 | Database Management Systems (DBMS) | |
| 18. | 16EC6D7 | Internet of Things (IoT) | |
| 19. | 16G6E01 | Bioinspired Engineering | |
| 20. | 16G6E02 | Green Technology | |
| 21. | 16G6E03 | Solid Waste Management | |
| 22. | 16G6E04 | Introduction to Web Programming | |
| 23. | 16G6E05 | Automotive Electronics | |
| 24. | 16G6E06 | Industrial Electronics | |
| 25. | 16G6E07 | Project Management | |
| 26. | 16G6E08 | Virtual Instrumentation | |
| 27. | 16G6E09 | Introduction to Mobile Application Development | |
| 28. | 16G6E10 | Automotive Engineering | |
| 29. | 16G6E11 | Mobile Network System and Standards | |
| 30. | 16G6E12 | Partial Differential Equations | |
| 31. | | | |
| 32. | | | |

# R V COLLEGE OF ENGINEERNG, BENGALURU-560 059

**(Autonomous Institution Affiliated to VTU, Belagavi)**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

| FIFTH SEMESTER CREDIT SCHEME | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Sl. No** | **Course Code** | **Course Title** | **BOS** | **Credit Allocation** | | | | **Total Credits** |
| | | | | **L** | **T** | **P** | **S** | |
| 1 | 16HSI51 | IPR & Entrepreneurship | HSS | 3 | 0 | 0 | 0 | 3 |
| 2 | 16EC52 | Communication System I | ECE | 3 | 1 | 1 | 0 | 5 |
| 3 | 16EC53 | Digital VLSI Design | ECE | 3 | 1 | 1 | 0 | 5 |
| 4 | 16EC54 | Embedded System Design | ECE | 3 | 0 | 0 | 1 | 4 |
| 5 | 16EC55 | Digital Signal Processing | ECE | 3 | 0 | 0 | 1 | 4 |
| 6 | 16EC5AX | Elective A (PE) | ECE | 3 | 0 | 0 | 1 | 4 |
| 7 | 16G5BXX | Elective B (OE)* | Respective BOS | 4 | 0 | 0 | 0 | 4 |
| | | **Total No. of Credits** | | | | | | **29** |
| | | **No. Of Hrs.** | | **22** | **4** | **4** | **12**** | **30** |

*Students should take other department Global Elective courses **Non-contact hours

| **Elective A (PE)** 16EC5AX | **Elective Title** | **Elective B (OE)** 16G5BXX |
|---|---|---|
| 16EC5A1 | Antennas and Wave Propagation | To be opted from electives offered by other Departments. For more information about other electives see following table |
| 16EC5A2 | Transducers & Data Acquisition Systems | |
| 16EC5A3 | Artificial Neural Networks & Deep Learning | |
| 16EC5A4 | Modelling of semiconductor devices | |
| 16EC5A5 | Object Oriented Programming in C++ | |
| 16EC5A6 | Computer Organization and Architecture | |
| 16EC5A7 | Robotics | |

| **PE - PROFESSIONAL ELECTIVE** | **OE- OTHER ELECTIVES** |
|---|---|

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

| SIXTH SEMESTER CREDIT SCHEME | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Sl. No.** | **Course Code** | **Course Title** | **BOS** | **Credit Allocation** | | | | **Total Credits** |
| | | | | **L** | **T** | **P** | **S** | |
| 1 | 16HEM61 | Foundations of Management & Economics | HSS | 2 | 0 | 0 | 0 | 2 |
| 2 | 16EC62 | Communication System II | ECE | 4 | 0 | 1 | 0 | 5 |
| 3 | 16EC63 | Computer Communication Networks | ECE | 3 | 0 | 1 | 1 | 5 |
| 4 | 16EC64 | Analog & Mixed Signal IC Design | ECE | 3 | 1 | 0 | 0 | 4 |
| 5 | 16EC6CX | Elective C (PE) | ECE | 3 | 0 | 0 | 1 | 4 |
| 6 | 16EC6DX | Elective D (PE) | ECE | 3 | 0 | 0 | 1 | 4 |
| 7 | 16G6EXX | Elective E (OE)* | Respective BOS | 3 | 0 | 0 | 0 | 3 |
| 8 | 16HS8 | Professional Practice-III (Employability Skills and Professional Development of Engineers) | HSS | 1 | 0 | 0 | 0 | 1 |
| | | **Total No. of Credits** | | | | | | **28** |
| | | **No. Of Hrs.** | | **22** | **2** | **4** | **12**** | **28** |

*Students should take other department Global Elective courses **Non-contact hours

| **Elective C (PE)** 16EC6CX | **Elective Title** | **Elective D (PE)** 16EC6DX | **Elective Title** | **Elective E (OE)** 16G6EXX |
|---|---|---|---|---|
| 16EC6C1 | Cryptography & Network Security | 16EC6D1 | Optical Fiber Communication & Networks | To be opted from electives offered by other Departments. For more information about other electives see following table |
| 16EC6C2 | Real Time Embedded Systems | 16EC6D2 | ARM Cortex Processors | |
| 16EC6C3 | Image Processing | 16EC6D3 | Adaptive Signal Processing | |
| 16EC6C4 | Low power VLSI Design | 16EC6D4 | System Verilog | |
| 16EC6C5 | Data structure using C++ | 16EC6D5 | Algorithm for VLSI Design Automation | |
| 16EC6C6 | System Programming & Software | 16EC6D6 | Database Management Systems(DBMS) | |
| 16EC6C7 | Flexible Electronics | 16EC6D7 | Internet of Things (IoT) | |

| **PE – PROFESSIONAL ELECTIVE** | **OE- OTHER ELECTIVES** |
|---|---|

## Global Electives offered

### V SEMESTER

| S.No | Course Code | Course | Offering Dept. |
|---|---|---|---|
| 1. | 16G5B01 | Bioinformatics | Biotechnology |
| 2. | 16G5B02 | Fuel Cell Technology | Chemical Engineering |
| 3. | 16G5B03 | Geoinformatics | Civil Engineering |
| 4. | 16G5B04 | Graph Theory | Computer Science Engineering |
| 5. | 16G5B05 | Artificial Neural Networks & Deep Learning | Electronics & Communication Engineering |
| 6. | 16G5B06 | Hybrid Electric Vehicles | Electrical & Electronics Engineering |
| 7. | 16G5B07 | Optimization Techniques | Industrial & Management Engineering |
| 8. | 16G5B08 | Sensors & Applications | Electronics & Instrumentation Engineering |
| 9. | 16G5B09 | Introduction To Management Information Systems | Information Science Engineering |
| 10. | 16G5B10 | Industrial Automation | Mechanical Engineering |
| 11. | 16G5B11 | Telecommunication Systems | Telecommunication Engineering |
| 12. | 16G5B12 | Computational advanced numerical methods | Mathematics |

### VI SEMESTER

| S.No | Course Code | Course | Offering Dept. |
|---|---|---|---|
| 1. | 16G6E01 | Bioinspired Engineering | Biotechnology |
| 2. | 16G6E02 | Green Technology | Chemical Engineering |
| 3. | 16G6E03 | Solid Waste Management | Civil Engineering |
| 4. | 16G6E04 | Introduction to Web Programming | Computer Science Engineering |
| 5. | 16G6E05 | Automotive Electronics | Electronics & Communication Engineering |
| 6. | 16G6E06 | Industrial Electronics | Electrical & Electronics Engineering |
| 7. | 16G6E07 | Project Management | Industrial & Management Engineering |
| 8. | 16G6E08 | Virtual Instrumentation | Electronics & Instrumentation Engineering |
| 9. | 16G6E09 | Introduction to Mobile Application Development | Information Science Engineering |
| 10. | 16G6E10 | Automotive Engineering | Mechanical Engineering |
| 11. | 16G6E11 | Mobile Network System and Standards | Telecommunication Engineering |
| 12. | 16G6E12 | Partial Differential Equations | Mathematics |

**B.E., ECE -ELECTIVE COURSES (Consolidated Stream wise)**

| **Local Elective** | **Semester V** | **Semester VI** | | **Semester VII** | **Semester VII** |
|---|---|---|---|---|---|
| **Streams** | **Sem V-1 (16EC5AX)** | **Sem VI-1 (16EC6CX)** | **Sem VI-2 (16EC6DX)** | **Sem VII-1(16EC7FX)** | **Sem VII-2(16EC7GX)** |
| **L:T:P:S** | 3:0:0:1 | 3:0:0:1 | 3:0:0:1 | 4:0:0:0 | 4:0:0:0 |
| **Communications** | Antennas & Wave Propagation | Cryptography & Network Security | Optical Fiber Communication & Networks | Satellite Communications & GPS | Radar & Navigation |
| **Embedded Systems** | Transducers & Data Acquisition Systems | Real Time Embedded Systems | ARM Cortex Processors | ARM Programming & Optimization | Automotive Electronics |
| **Signal Processing** | Artificial Neural Networks & Deep Learning | Image Processing | Adaptive Signal Processing | Speech Processing | Multimedia Communication |
| **VLSI** | Modelling of semiconductor devices | Low power VLSI Design | System Verilog/Algorithm for VLSI Design Automation | Radio Frequency Integrated Circuits Design | VLSI Testing for ICs |
| **Computer** | Object Oriented Programming in C++ /Computer Organization and Architecture | Data structure using C++/System Programming & Software | Database Management Systems (DBMS) | High Performance Computing | High Speed digital design |
| **Others** | Robotics | Flexible Electronics | Internet of Things (IoT) | Integrated Photonics/Nanoelectronics | MEMS and Smart Systems |
| **Global Elective** | Artificial Neural Networks & Deep Learning (L:T:P:S 4:0:0:0) | Automotive Electronics (L:T:P:S 3:0:0:0**)** | -- | Image Processing (L:T:P:S 3:0:0:0) | -- |

| **Semester: V** | | |
|---|---|---|
| **INTELLECTUAL PROPERTY RIGHTS AND ENTREPRENEURSHIP (Theory) (COMMON TO CS, EC, EE, IS, TC)** | | |
| **Course Code:** 16HSI51 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:0 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 03Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | To build awareness on the various forms of IPR and to build the perspectives on the concepts and to develop the linkages in technology innovation and IPR. |
| **2** | To equip students on the need to protect their own intellectual works and develop ethical standards governing ethical works. |
| **3** | To motivate towards entrepreneurial careers and build strong foundations skills to enable starting, building and growing a viable as well as sustainable venture. |
| **4** | Develop an entrepreneurial outlook and mind set along with critical skills and knowledge to manage risks associated with entrepreneurs. |

| **UNIT-I** | |
|---|---|
| **Introduction:** Types of Intellectual Property, WIPO, WTO, TRIPS.<br>**Patents:** Introduction, Scope and salient features of patent; patentable and non-patentable inventions, Patent Procedure - Overview, Transfer of Patent Rights; Biotechnology patents, protection of traditional knowledge, Infringement of patents and remedy, Case studies<br>**Trade Secrets:** Definition, Significance, Tools to protect Trade secrets in India. | **07 Hrs** |
| **UNIT-II** | |
| **Trade Marks:** Concept, function and different kinds and forms of Trade marks, Registrable and non- registrable marks. Registration of trade mark; Deceptive similarity; Assignment and transmission; ECO Label, Passing off; Offences and penalties. Infringement of trade mark with Case studies | **04 Hrs** |
| **UNIT-III** | |
| **Industrial Design:** Introduction, Protection of Industrial Designs, Protection and Requirements for Industrial \|Design. Procedure for obtaining Design Protection, Revocation, Infringement and Remedies, Case studies<br>**Copy Right:** Introduction, Nature and scope, Rights conferred by copy right, Copy right protection, transfer of copy rights, right of broad casting organizations and performer's rights, Case Studies.<br>**Intellectual property and cyberspace:** Emergence of cyber-crime; Grant in software patent and Copyright in software; Software piracy; Data protection in cyberspace | **09 Hrs** |
| **UNIT-IV** | |
| **Introduction to Entrepreneurship** – Learn how entrepreneurship has changed the world. Identify six entrepreneurial myths and uncover the true facts. Explore E-cells on Campus<br>**Listen to Some Success Stories: -** Global legends Understand how ordinary people become successful global entrepreneurs, their journeys, their challenges, and their success stories. Understand how ordinary people from their own countries have become successful entrepreneurs.<br>**Characteristics of a Successful Entrepreneur** Understand the entrepreneurial journey and learn the concept of different entrepreneurial styles. Identify your own entrepreneurship style based on your personality traits, strengths, and weaknesses. Learn about the 5M Model, each of the five entrepreneurial styles in the model, and how they differ from each other. **Communicate Effectively:** Learn how incorrect assumptions and limiting our opinions about people can negatively impact our communication. Identify the barriers which cause communication breakdown, such as miscommunication and poor listening, and learn how to overcome them.<br>**Communication Best Practices.** Understand the importance of listening in communication | **08 Hrs** |

| | |
|---|---|
| and learn to listen actively. Learn a few body language cues such as eye contact and handshakes to strengthen communication. (Practical Application) | |
| **UNIT-V** | |
| **Design Thinking for Customer Delight: -** Understand Design Thinking as a problem-solving process. Describe the principles of Design Thinking. Describe the Design Thinking process.<br>**Sales Skills to Become an Effective Entrepreneur: -** Understand what is customer focus and how all selling effort should be customer-centric. Use the skills/techniques of personal selling, Show and Tell, and Elevator Pitch to sell effectively.<br>**Managing Risks and Learning from Failures: -** Identify risk-taking and resilience traits. Understand that risk-taking is a positive trait. Learn to cultivate risk-taking traits. (Practical Application) Appreciate the role of failure on the road to success, and understand when to give up. Learn about some entrepreneurs/risk-takers. (Practical Application).<br>**Are You Ready to be an Entrepreneur: -** Let's ask "WHY" Give participants a real picture of the benefits and challenges of being an entrepreneur. Identify the reasons why people want to become entrepreneurs. Help participants identify why they would want to become entrepreneurs. | **08 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Comprehend the applicable source, scope and limitations of Intellectual Property within the perview of engineering domain. |
| CO2: | Knowledge and competence related exposure to the various Legal issues pertaining to Intellectual Property Rights with the utility in engineering perspectives. |
| CO3: | Enable the students to have a direct experience of venture creation through a facilitated learning environment. |
| CO4: | It allows students to learn and apply the latest methodology, frameworks and tools that entrepreneurs use to succeed in real life. |

| **Reference Books** | |
|---|---|
| **1.** | Law Relating to Intellectual Property, Wadehra B L,5th Edition, 2012, Universal Law Pub Co. Ltd.-Delhi, ISBN: 9789350350300 |
| **2.** | Intellectual Property Rights: Unleashing Knowledge Economy, Prabuddha Ganguly, 1st Edition,2001, Tata McGraw Hill Publishing Company Ltd., New Delhi, ISBN: 0074638602. |
| **3.** | Intellectual Property and the Internet, Rodney Ryder, 2002, Lexis Nexis U.K., ISBN: 8180380025, 9788180380020. |
| **4.** | Entrepreneurship, Rajeev Roy, 1st Edition, 2012, Oxford University Press, New Delhi, ISBN: 9780198072638. |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Assignment. A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 60. The marks component for assignment is 10. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **1** | **-** | **-** | **-** | **3** | **3** | **-** | **3** | **1** | **2** | **-** | **3** |
| **CO2** | **1** | | | | **3** | **3** | **3** | **3** | **1** | **2** | **-** | **3** |
| **CO3** | **-** | **3** | **2** | **-** | **-** | **2** | **2** | **3** | **3** | **3** | **3** | **3** |
| **CO4** | **-** | **3** | **2** | **-** | **-** | **3** | **3** | **3** | **3** | **3** | **3** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **COMMUNICATION SYSTEM I (Theory & Practice)** | | |
| **Course Code:** 16EC52 | | **CIE Marks:** 100+50 |
| **Credits: L:T:P:S:** 3:1:2:0 | | **SEE Marks:** 100+50 |
| **Hours:** 36L+24T | | **SEE Duration:** 03Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand the concepts of FM, Low pass and bandpass sampling and Random processes to compute performance parameters |
| **2** | Analyse the concepts of sampling, quantization, encoding and apply them to voice conditioning for communication purposes. |
| **3** | Understand the concepts of information theory as a prerequisite for error detection and correction. |
| **4** | Associate the concepts of Information Theory to the principle of block error coding and decoding for different communication scenario. |

| **UNIT-I** | |
|---|---|
| **Angle (Exponential) Modulation** Nonlinear Modulations, Bandwidth of Angle-Modulated Waves, Generating of FM Waves by direct methods, Demodulation of FM, PLL.<br>**Sampling and Analog to Digital Conversion** Low Pass Sampling Theorem (Impulse, Pulse and Flat top), Bandpass and equivalent low pass signal representation, Quadrature Sampling of bandpass signals, Bandpass Sampling Theorem statement with Applications. | **07 Hrs** |
| **UNIT-II** | |
| **Review of Random Variables and their properties**<br>**Multiple Random Variables:** Properties, Operations**. Random Processes** From Random Variable to Random Process, Classification of Random Processes, properties and operations.<br>**Baseband Pulse Transmission (Line Codes) (RZ and NRZ)** Unipolar, Polar, Bipolar, Manchester signaling, Discrete form statement of Wiener – Khinchine Theorem – Applications to PSD derivations for these pulses. Highlights of other baseband pulses HDB3, B6ZS. | **07 Hrs** |
| **UNIT-III** | |
| **Digital Multiplexing and demultiplexing:** Framing with overheads, Types- Synchronous, Asynchronous, Quasi-Synchronous. Demultiplexing FSM, Retiming FSM with Plesiochronous buffering.<br>**Pulse-Code Modulation (PCM)** – Uniform Quantization, Non uniform Quantization – Optimal quantizer and Robust quantizer (μ-law and A-law), SNR derivations for all types. Differential Pulse Code Modulation (DPCM), Delta Modulation with SNR derivation, Adaptive DM with SNR statement only.<br>Sigma-delta Modulation concept. Applications to Channel Vocoders and LPC Vocoders.(Conceptual treatment) | **08 Hrs** |
| **UNIT-IV** | |
| **Introduction to Information Theory** Measure of Information, Source Encoding, Error-Free Communication over a Noisy Channel, Channel Capacity of a Discrete Memory less Channel, Channel Capacity of a Continuous memory less Channel, Practical Communication Systems in Light of Shannon's Equation, Frequency selective Channel capacity, Multiple input Multiple output Communication System. | **07 Hrs** |
| **UNIT-V** | |
| **Error Correcting Codes**<br>Redundancy for error correction, Linear Block Codes, Cyclic Codes, The effect of error correction, Burst-Error Detecting and Correcting Codes. A brief concept of RS Codes + Interleaving | **07 Hrs** |

| **Practical's: Communication Lab** | |
|---|---|
| 1. Frequency Modulation and Demodulation (Matlab)<br>2. Verification of Sampling theorem<br>3. Implementation of Convolution and DFT<br>4. Realization of FIR filter to meet given specifications (DSP kit)<br>5. Realization of IIR filter to meet given specifications (DSP kit)<br>6. Generation of Noise and study of its properties<br>7. Time Division Multiplexing ( Matlab & Circuit)<br>8. Pulse Code Modulation & Delta Modulation (Matlab & Simulink)<br>9. Linear block code and Huffman code (Matlab)<br>**10.** Line codes generation and Pe & PSD Calculation | |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Associate and apply the concepts of digital formatting, reconstruction to digital transmitter and receivers used in cellular and other communication devices. |
| CO2: | Analyze and compute performance of continuous wave modulation, digital formatting schemes. |
| CO3: | Test and validate digital formatting schemes and block codes under noisy channel conditions to estimate the performance in practical communication systems. |
| CO4: | Design/Demonstrate by way of simulation or emulation of different functional blocks of digital formatting and block error correction |

| **Reference Books** | |
|---|---|
| **1.** | Modern Digital and Analog communication Systems, B.P.Lathi and Zhi Ding, 4th Edition, 2010 , Oxford University Press, ISBN: 9780198073802. |
| **2.** | Analog & Digital Communication Systems, Simon Haykin, 1st Edition, 2014, John Wiley & sons, , ISBN 978-0-471-64735-5. |
| **3.** | Communication Systems, Simon Haykin , 4th Edition, 2004, John Wiley, India Pvt. Ltd, ISBN 0471178691 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Assignment. A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 60. The marks component for assignment is 10. The total marks of CIE are 100.

**Laboratory- 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 40 marks. At the end of the semester a test is conducted for 10 marks. Total marks for the laboratory is 50.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**Laboratory- 50 Marks**

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **2** | **-** | **-** | **-** | **1** | **1** | **-** | **2** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **-** | **-** | **-** | **1** | **1** | **-** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **DIGITAL VLSI DESIGN (Theory & Practice)** | | |
| **Course Code:** 16EC53 | | **CIE Marks:** 100+50 |
| **Credits: L:T:P:S:** 3:1:1:0 | | **SEE Marks:** 100+50 |
| **Hours:** 36L+24T | | **SEE Duration:** 03Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Analyze the impact of fabrication technologies: Methods for optimizing the area, speed, and power of circuit layouts. |
| **2** | Design and implement combinational circuit. |
| **3** | Design and implement sequential system by considering specifications. |
| **4** | Analyze the impact of RC effect in post simulation. |

| **UNIT-I** | |
|---|---|
| **VLSI Design Flow :** Specification, Design entry, Functional simulation, planning placement and routing, timing simulation.**MOS Transistor:** Introduction, Ideal I-V characteristics, C-V Characteristics, Simple MOS Capacitance Models, Detailed MOS Gate Capacitance Model, Non-ideal I-V Effects, Mobility Degradation and Velocity Saturation, Channel Length Modulation, Threshold Voltage Effects, Junction Leakage, Body effect, Tunneling. **DC Transfer Characteristics:** Static CMOS Inverter DC Characteristics, Beta Ratio Effect, Noise Margin, Pass Transistor DC Characteristics. | **07 Hrs** |
| **UNIT-II** | |
| **Combinational Circuit Design:** CMOS Logic, Inverter, NAND Gate, NOR Gate, Combinational Logic, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers. **Circuit Families:** Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Complementary Pass-Transistor Logic Circuits.: **Datapath Subsystem:** Single-Bit Addition, Ripple Carry Adder, Carry Look ahead Adder, Carry Save Adder, Unsigned Array Multiplication, 2's Complement Array Multiplication, Wallace Tree Multiplication. | **08 Hrs** |
| **UNIT-III** | |
| **Sequential MOS Logic Circuitry:** Behavioral of Bistable element, SR Latch Circuitry, Clocked latch and Flip Flop Circuitry, C-MOS D-Latch and Edge Triggered Flip-Flop. **Sequencing Static Circuits:** Sequencing Methods, Max-Delay Constraints, Min-Delay Constraints Time Borrowing, Clock Skew | **07 Hrs** |
| **UNIT-IV** | |
| **Array Sub system SRAM:** Memory cell Read/Write operation, Decoder, Bit-line conditioning and column circuitry and Column Circuitry, Multi-Ported SRAM. **DRAM** Subarray Architectures, Column Circuitry Read-Only Memory Programmable ROMs, NAND ROMs. Content-Addressable Memory | **07 Hrs** |
| **UNIT-V** | |
| **CMOS Processing Technology:** CMOS Technologies, Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Isolation, Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, Methodology**. :** Lambda Design Rules. Transistor Scaling. Inverter (nMOS and CMOS) | **07 Hrs** |
| **Practical's: VLSI Lab**<br>1.<br>a Realize CMOS Logic-universal gates.<br>b Practice question: Realize XOR/XNOR gates<br>2.<br>a Realization of CMOS - adder circuits<br>b Practice question: Realize 4-bit adder/subractor<br>3.<br>a MOS device Characterization | |

| | |
|---|---|
| b Practice question: Plot $g_m$ Vs $V_{gs}$ for NMOS/PMOS<br><br>4.<br>a Inverter Static Characteristics<br>b Practice question: Plot the Voltage Transfer Characteristic graph of CMOS inverter and calculate the switching voltage for the given specification<br>5.<br>a Sequential Circuit Design using Master-Slave configuration<br>b Practice question: Realize 4-bit binary counter<br>6. Inverter layout and post simulation<br>7.<br>a NOR/NAND gates layout and post simulation<br>b Practice question: Realize AND/OR gates<br>8.<br>a Common source single stage amplifier and Differential amplifier<br>b Practice question: Realize Op-amp circuit<br>9. Realize 2-bit multiplier circuit using Mixed mode<br><br>**Case study:** ASIC design flow using cadence. (Students should learn the concept and produce the relevant document) | |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Analyze transistor circuits and its impact on VLSI design flow. |
| CO2: | Apply & analyze the design parameters for speed, area & power optimization. |
| CO3: | Evaluate the functionality of VLSI blocks using various architectures. |
| CO4: | Analyze various fabrication processes for different logic families/designs. |

| **Reference Books** | |
|---|---|
| **1.** | CMOS VLSI Design, Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, 2006, Pearson Education, ISBN: 0321149017 |
| **2.** | CMOS Digital Integrated Circuits, Sung MO Kang, Yousf Leblebici, 3rd Edition, Tata McGrawHill, ISBN: 0-7923-7246-8 |
| **3.** | Basic VLSI Design, Douglas.A.Pucknell, Kamaran Eshraghian, 3rd Edition 2010 ,PHI, ,ISBN: 0-321-26977-2 |
| **4.** | Digital Integrated Circuits- A Design perspective, Jan M rabaey, 2nd Edition, 2005. Prentice Hall |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Assignment. A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 60. The marks component for assignment is 10. The total marks of CIE are 100.

**Laboratory- 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 40 marks. At the end of the semester a test is conducted for 10 marks. Total marks for the laboratory is 50.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I,

IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**Laboratory- 50 Marks**

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **3** | **2** | **-** | **3** | **-** | **-** | **-** | **1** | **-** | **-** | **2** |
| **CO2** | **3** | **2** | **3** | **2** | **3** | **-** | **1** | **-** | **-** | **-** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **3** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO4** | **1** | **1** | **3** | **3** | **3** | **-** | **2** | **1** | **-** | **1** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **EMBEDDED SYSTEM DESIGN (Theory)** | | |
| **Course Code:** 16EC54 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 03Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand embedded computing system, design process and basic building blocks of an embedded system. |
| **2** | Illustrate how microprocessor, memory, peripheral components and buses build an embedded platform and their interaction. |
| **3** | Evaluate how architectural and implementation design decisions influence performance and power dissipation. |
| **4** | Explain the basic operation of a real-time operating system. |
| **5** | Building, testing the operation of real-time embedded application programs through hands-on experience with a single-board computer. |

| **UNIT-I** | |
|---|---|
| **I Introduction to Embedded System Design:** Introduction, Characteristics of Embedding Computing Applications, Concept of Real time Systems, Challenges in Embedded System Design, Design Process: Requirements, Specifications, Hardware Software Partitioning, Architecture Design. **Embedded System Architecture:** Co-Processor & Hardware Accelerators, Processor performance Enhancement: Pipelining, Superscalar Execution, Multi Core CPUs. | **08 Hrs** |
| **UNIT-II** | |
| **Designing Embedded System Hardware –I:** Memory systems: Memory organization, Error detecting and correcting, memory Access times, DRAM interfaces, DRAM refresh techniques, Cache, Unified versus Harvard caches, Cache coherency, Cache, Dual port and shared memory. | **07 Hrs** |
| **UNIT-III** | |
| **Designing Embedded System Hardware –II:** I/O Devices: Watchdog Timers, Interrupt Controllers, Interfacing Protocols: SPI, I2C, CAN: Frame Formats, Wiring Topology, Reset Circuits, Interfacing RTC. | **08 Hrs** |
| **UNIT-IV** | |
| **Designing Embedded System Software** Application Software, System Software, Use of High Level Languages: C, C++, Java, Programming & Integrated Development Environment tools, Debugger, Board Support Library, Chip Support Library Analysis and Optimization: Execution Time, Energy & Power, Program Size; Embedded System Coding Standards: MISRA C 2012. | **07 Hrs** |
| **UNIT-V** | |
| **Designing Embedded System Software –II:** OS based Design, Real Time Kernel, Process& Thread, Multi-threading, Synchronization, Kernel services, Case Study: RTX-ARM. | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Analyse the architecture of embedded system, functional difference between general purpose system, operational & nonoperational attributes of embedded system. |
| CO2: | Analyze the hardware requirements of an embedded system & design according to specifications. |
| CO3: | Develop software architecture & realize optimally using suitable language. |
| CO4: | Engage in self-study to formulate, design, implement, analyze and demonstrate an embedded application developed to control real world operations. |

| **Reference Books** | |
|---|---|
| **1.** | Introduction to Embedded Systems, Shibu K V, 2009, Tata McGraw Hill Education Private Limited, ISBN: 10: 0070678790 |
| **2.** | Embedded System Design, Steve Heath, 2nd Edition, 2004, Elsevier, |
| **3.** | Embedded Systems – A contemporary Design Tool ,James K Peckol, 2008, John Weily, ISBN: 0-444-51616-6 |
| **4.** | MSP430 Microcontroller Basics, John H. Davies, 2008, Newness Publishing House |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **1** | **2** | **1** | **1** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **1** | **2** | **1** | **-** | **-** | **1** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **2** | **1** | **2** | **-** | **1** | **-** | **2** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **3** | **2** | **3** | **3** | **3** | **3** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **DIGITAL SIGNAL PROCESSING (Theory & Practice)** | | |
| **Course Code:** 16EC55 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 03Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand the key theoretical principles underpinning Digital Signal Processing in a design procedure through FIR and IIR filters. |
| **2** | Analyze the effect of up-sampling and down-sampling and interprets the sampling rate conversion in multistage implementation of digital filters |
| **3** | Develop the DFT filter bank using the concept of Maximally decimated DFT filter bank and Transmultiplexer. |
| **4** | Interface the digital system with different sampling rates and Sub-band Coding of Speech Signals with touch tone generation and reception for digital telephones. |

| **UNIT-I** | |
|---|---|
| **Design of IIR Filter:** Analog filter design using Butterworth and Chebyshev filter. IIR Filter design by Bilinear Transformation, digital filter designs based on the Bilinear Transformation using Analog filter. | **07 Hrs** |
| **UNIT-II** | |
| **Design of FIR Filters**: Symmetric and anti-symmetric FIR Filters, FIR Filter structure: Direct form structure, cascade form structures, frequency sampling structures, lattice structure. Design of Linear phase FIR Filters using Windows, Design of Linear phase FIR filters by frequency Sampling method. | **08 Hrs** |
| **UNIT-III** | |
| **Multirate Digital signal Processing:** Introduction, Analysis of down sampling and up-sampling, Sampling rate conversion by a rational factor, Multistage implementation of digital filters, Efficient implementation of Multirate systems | **08 Hrs** |
| **UNIT-IV** | |
| **Applications of Multirate Signal Processing**: Digital to Analog conversion, DFT filter bank, maximally decimated DFT filter bank, Transmultiplexer. | **07 Hrs** |
| **UNIT-V** | |
| **Applications of Digital Filter Banks:** Implementation of Narrow band Low pass Filters, Design of phase shifter, Interfacing of digital system with different sampling rates, Sub band Coding of Speech Signals, Touch tone generation and reception for digital telephones. | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Apply appropriate mathematical skills to describe and solve problems in designing of filters and Multirate signal processing |
| CO2: | Analyse and design the fundamental blocks of Multirate signal processing and DFT filter banks. |
| CO3: | Analyze discrete system and validate the functionality of the same using simulation tool. |
| CO4: | Design discrete systems to meet specific requirement for signal processing application |

| **Reference Books** | |
|---|---|
| **1.** | Proakis G, Dimitris G. Manolakis; "Digital Signal Processing"; PHI; 4th Edition; 2007; ISBN: 978-0131873742 |
| **2.** | Roberto Cristi, "Modern digital signal Processing", Cengage learning, 2004. |
| **3.** | Lonnie C. Ludeman; "Fundamentals of Digital Signal Processing"; John Wiely & Sons; 1986; ISBN: 0471603635 |

| | |
|---|---|
| **4.** | Monson H.Hayes; "Digital Signal Processing"; Schaum's Outline Series; 2nd Edition; 2011; ISBN: 0071635092 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO2** | **3** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **-** | **2** | **-** | **-** | **2** | **3** | **1** | **1** | **2** |
| **CO4** | **3** | **3** | **3** | **-** | **2** | **-** | **-** | **1** | **1** | **1** | **2** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **ANTENNAS AND WAVE PROPAGATION (Theory)** | | |
| **Course Code:** 16EC5A1 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Analyze how an antenna radiates and capture radio wave energy from the concepts of radiation by dynamic currents, charges and retarded potentials. |
| **2** | Demonstrate properties and parameters of antenna such as radiation pattern, radiation impedance, directivity, antenna gain and effective area. |
| **3** | Apply the Friss transmission expression and reciprocity principle effectively to predict the receive power in a system consisting of transmit and receive antenna. |
| **4** | Develop an antenna system including the shape of the antenna, feed property, the requirement on the arrangement of the radiating elements in an array, given the radiation parameters such as radiation pattern, gain, operating frequency, transmit/receive power |

| **UNIT-I** | |
|---|---|
| **Antenna Basics**<br>Parameters, Patterns, Beam Solid Angle, Radiation Intensity, Directivity and Gain, Radio Communication Link, Polarization, Antenna Temperature.<br>**Types of Antennas**<br>Point Source, Monopole & Dipole, Loop Antenna, Slot Antenna, Horn Antenna, Reflector Antenna, Lens Antenna, Helical Antenna, Reflector Antennas, Smart Antennas, Diversity Reception, MIMO | **08 Hrs** |
| **UNIT-II** | |
| **Electric Dipole**<br>Short Electric Dipole, Fields, Radiation Resistance, λ/2 Dipole and its Characteristics, Folded Dipole, Rhombic Antenna and V Antenna.<br>**Antenna Arrays**<br>Linear Array, Principle of Pattern Multiplication, Broadside and End Fire Arrays, Uniform and Non- Uniform Arrays. | **07 Hrs** |
| **UNIT-III** | |
| **Special Types of Antennas**<br>Babinet's Principle and Complementary Antennas, Lens Antenna, Turnstile Antenna, Base Station and Mobile Antenna, Embedded Antenna.<br>**Broadband and Frequency Independent Antennas**<br>Basics, Biconical Antenna, Log Periodic Antenna, UWB Antennas for Digital Applications | **07 Hrs** |
| **UNIT-IV** | |
| **Micro-Strip and Patch Antennas**<br>Salient Features, Advantages and Limitations, Feed Methods, Characteristics, Array of Micro-Strip Antennas, Applications.<br>**Antenna measurements**<br>Measurement Range, Radiation Pattern Measurement, Gain and Directivity, Polarization, Power Measurements | **07 Hrs** |
| **UNIT-V** | |
| **Basics of Wave Propagation** Guided Waves, Unguided Waves, Classification of EM Spectrum, Noise, Tropo and Iono Scatter, Mobile Propagation Models<br>**Ground, Sky & Space Wave Propagation** Ground Reflection, Diffraction, Wave Tilt, Ionosphere Layers and Its Properties, Critical Frequency, MUF, LUF, Virtual Height& Skip Distance', Effect of Earth's Magnetic Field, Space Propagation, Effects of Earth's Curvature, Radio Horizon , Variation of Field Strength with Height. | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Apply the concepts of physics to understand the mechanism of antenna radiation and working of different antennas. |
| CO2: | Apply basic concepts of electromagnetics to determine different performance parameters of antennas. |
| CO3: | Analyze the antenna parameters such as radiation pattern, directivity, gain, etc of various antennas. |
| CO4: | Design the antennas to achieve prescribe specification for different RF applications. |

| **Reference Books** | |
|---|---|
| **1.** | Antennas and wave propagation, John D Kraus, Ronald J Marhefka, Ahmad S Khan, 4th Edition, 2010, McGraw Hill, ISBN: 0-07-067155-9 |
| **2.** | Antennas and Wave Propagation , A.R.Harish, M.Sachidananda, 2007, Oxford University Press, ISBN: 978-0195686661 |
| **3.** | Antenna Theory: Analysis & Design ,C A Balanis, 3rd Edition, John-Wiley, ISBN: 978-0471025900 |
| **4.** | Antenna Theory & Design , Warren L. Stutzman, Gary A. Thiele, 3rd Edition ,Wiley India Pvt. Ltd, ISBN 9788126523771 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **1** | **2** | **-** | **-** | **-** | **-** | **1** | **2** | **2** |
| **CO4** | **3** | **3** | **3** | **1** | **2** | **-** | **-** | **1** | **1** | **1** | **2** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **TRANSDUCERS & DATA ACQUISITION SYSTEMS (Theory)** | | |
| **Course Code:** 16EC5A2 | | **CIE Marks: 100** |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks: 100** |
| **Hours:** 36L | | **SEE Duration: 3Hrs** |
| **Course Learning Objectives: The students will be able to** | | |
| **1** | Understand the architecture & importance of data acquisition systems. | |
| **2** | Impart an in-depth knowledge in sensor signal conditioning, signal conversion, data acquisition, signal processing, transmission and analysis. | |
| **3** | Provide a comprehensive coverage of data acquisition methods for sensor systems and hardware interface cards available commercially. | |
| **4** | Introduce the students to pSpice and LabView through practical sessions. | |

| **UNIT-I** | |
|---|---|
| **Fundamentals of Data Acquisition**<br>Fundamentals of Data Acquisition-Configuration and Structure-Interface Systems-Interface Bus. Analog and Digital Signals. Review of Quantization in Amplitude and Time Axis.<br>**Signal Conditioners**<br>Signal Conditioners- Voltage and Current Amplifiers-Voltage Conditioners-Integrated Signal Conditioners for Temperature Sensors, Strain Gages, Piezoelectric Sensors and Linear Position Sensors | **08 Hrs** |
| **UNIT-II** | |
| **Mechanical Transducers**<br>Introduction, Basics of Temperature Measurement: Absolute thermodynamic or Kelvin Scale, Bimetallic Element, Basics of Pressure Measurement: Manometers, Ring Balance, Bell Type, Thin Plate diaphragms, Basics of Flow Measurement: Pitot Static Tube, Displacement to Pressure Transducer | **07 Hrs** |
| **UNIT-III** | |
| **Passive Electrical Transducers**<br>Resistance Thermometers: Thermistors, Semiconductor Temperature sensors, Errors in Temperature Measurements, Hot Wire Resistive Transducers, Capacitive transducers: Thickness transducers, Capacitive displacement Transducers, proximity Transducers, Capacitive Pressure Transducer, Capacitive Moisture Transducer. Introduction to Inductive Transducers. | **07 Hrs** |
| **UNIT-IV** | |
| **Active Electrical Transducers**<br>Introduction, Thermoelectric Transducer: Thermoelectric Phenomenon, Common Thermocouple Systems, Piezo electric Transducer: Piezoelectric Phenomenon, Piezoelectric Materials, Hall- effect Transducer, Electromechanical Transducer: Tachometers, Variable Reluctance Tachometers, Digital Transducers: Digital Displacement transducers, Optical Encoder. | **07 Hrs** |
| **UNIT-V** | |
| **Signal Processing Circuits**<br>Signal Conditioning Modules for Plug-In Board, Two-Wire Transmitter, Distributed I/O - High Speed Digital Transmitter. Field Wiring and Signal Measurement-Grounded and Floated Signal Source-Single Ended and Differential Ended Measurements. Ground Loop and System Isolation-Noise and Interference- Shielding. | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Identify and interpret different sensor design & analyze data acquisition system |
| CO2: | Design suitable sensor front end to monitor real world signals without information loss. |
| CO3: | Realization of sensors and data acquisition system for real time application. |
| CO4: | Usage of modern engineering tools for realizing the working of sensors and data acquisition system. |

| Reference Books | |
|---|---|
| **1.** | Transducers and Instrumentation, D V S Murthy, 2nd Edition, 2008, PHI Publisher |
| **2.** | Practical Data acquisition for Instrumentation and Control, John Park and Steve Mackay, 2003, Newness publishers |
| **3.** | Data Acquisition systems- from fundamentals to Applied Design, Maurizio Di Paolo Emilio, 2013, Springer |
| **4.** | Introduction to Data Acquisition with LabVIEW, Robert H King, 2nd edition, 2012, McGraw Hill, |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **1** | **1** | **1** | **1** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO2** | **2** | **2** | **2** | **2** | **1** | **1** | **-** | **-** | **1** | **1** | **1** | **1** |
| **CO3** | **2** | **2** | **2** | **2** | **1** | **1** | **2** | **-** | **2** | **1** | **2** | **2** |
| **CO4** | **2** | **1** | **2** | **2** | **3** | **-** | **-** | **2** | **3** | **1** | **2** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **ARTIFICIAL NEURAL NETWORKS &DEEP LEARNING (Theory)** | | |
| **Course Code:** 16EC5A3 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:4 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand Neural Network and model a Neuron and Express both Artificial Intelligence and Neural Network |
| **2** | Analyze ANN learning, Error correction learning, Memory-based learning, Hebbian learning, Competitive learning and Boltzmann learning |
| **3** | Implement Simple perception, Perception learning algorithm, Modified Perception learning algorithm, and Adaptive linear combiner, Continuous perception, learning in continuous perception. |
| **4** | Analyze the limitation of Single layer Perceptron and Develop MLP with 2 hidden layers, Develop Delta learning rule of the output layer and Multilayer feed forward neural network with continuous perceptions |

| **UNIT-I** | |
|---|---|
| **Introduction to Neural Networks:** Neural Network, Human Brain, Models of Neuron, Neural networks viewed as directed graphs, Biological Neural Network, Artificial neuron, Artificial Neural Network architecture, ANN learning, analysis and applications, Historical notes. | **08 Hrs** |
| **UNIT-II** | |
| **Learning Processes:** Introduction, Error correction learning, Memory-based learning, Hebbian learning, Competitive learning, Boltzmann learning, credit assignment problem, Learning with and without teacher, learning tasks, Memory and Adaptation. | **07 Hrs** |
| **UNIT-III** | |
| **Single layer Perception:** Introduction, Pattern Recognition, Linear classifier, Simple perception, Perception learning algorithm, Modified Perception learning algorithm, Adaptive linear combiner, Continuous perception, Learning in continuous perception. Limitation of Perception. | **07 Hrs** |
| **UNIT-IV** | |
| **Multi-Layer Perceptron Networks:** Introduction, MLP with 2 hidden layers, Simple layer of a MLP, Delta learning rule of the output layer, Multilayer feed forward neural network with continuous perceptions, Generalized delta learning rule, Back propagation algorithm | **07 Hrs** |
| **UNIT-V** | |
| **Introduction to Deep learning**: Neuro architectures as necessary building blocks for the DL techniques, Deep Learning & Neocognitron, Deep Convolutional Neural Networks, Recurrent Neural Networks (RNN), feature extraction, Deep Belief Networks, Restricted Boltzman Machines, Autoencoders, Training of Deep neural Networks, Applications and examples (Google, image/speech recognition) | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Model Neuron and Neural Network, and to analyze ANN learning, and its applications. |
| CO2: | Perform Pattern Recognition, Linear classification. |
| CO3: | Develop different single layer/multiple layer Perception learning algorithms |
| CO4: | Design of another class of layered networks using deep learning principles. |

| **Reference Books** | |
|---|---|
| **1.** | Neural Network- A Comprehensive Foundation , Simon Haykins, 2nd Edition, 1999, Pearson Prentice Hall, ISBN-13: 978-0-13-147139-9 |

| | |
|---|---|
| **2.** | Introduction to Artificial Neural Systems, Zurada and Jacek M, 1992, West Publishing Company, ISBN: 9780534954604 |
| **3.** | Learning & Soft Computing, Vojislav Kecman, 1st Edition, 2004, Pearson Education, ISBN:0-262-11255-8 |
| **4.** | Neural Networks Design, M T Hagan, H B Demoth, M Beale, 2002, Thomson Learning, ISBN-10: 0-9717321-1-6/ ISBN-13: 978-0-9717321-1-7 |


**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **1** | **1** | **-** | **-** | **1** | **-** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **1** | **1** | **-** | **-** | **1** | **-** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **1** | **1** | **-** | **-** | **1** | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **1** | **1** | **-** | **-** | **1** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **MODELLING OF SEMICONDUCTOR DEVICES (Theory)** | | |
| **Course Code:** 16EC5A4 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Explain and apply basic concepts of semiconductor physics relevant to devices |
| **2** | Describe, explain, and analyze the operation of important semiconductor devices in terms of their physical structure |
| **3** | Explain, describe, and use physics-based device and circuit models for semiconductor devices of varying levels of complexity, select models appropriate to a specific need, and apply those models to analyze multi-component circuits |
| **4** | Analyze and design microelectronic circuits for linear amplifier and digital applications |

| **UNIT-I** | |
|---|---|
| **Charge Carriers and Transport Modelling** Crystal Structure, Semiconductor Models, Carrier Properties, State and Carrier Distributions, Equilibrium Carrier Concentrations, Drift, Diffusion, Recombination-Generation, Equations of State, Modelling & Simulation examples. | **08 Hrs** |
| **UNIT-II** | |
| **Modelling of PN Junction Diodes:** pn Junction Electrostatics, Preliminaries, Quantitative Electrostatic Relationships, I-V Characteristics, The Ideal Diode Equation, Deviations from the Ideal, Small-Signal Admittance, Reverse-Bias Junction Capacitance, Forward-Bias Diffusion Admittance, MS Contacts and Schottky Diodes, Modelling & Simulation examples. | **07 Hrs** |
| **UNIT-III** | |
| **Modelling of BJT**: Electrostatics, Performance Parameters, Ideal Transistor Analysis, General Solution, Simplified Relationships, Ebers-Moll Equations and Model, Deviations from the Ideal, Modern BJT Structures, Modelling & Simulation examples. | **07 Hrs** |
| **UNIT-IV** | |
| **Modelling of MOS:** Electrostatics, Capacitance-Voltage Characteristics, Quantitative $I_D/V_D$ Relationships, Square-Law Theory, Bulk-Charge Theory, a.c. Response, Small-Signal Equivalent Circuits, Cutoff Frequency, Small-Signal Characteristics, Modelling & Simulation examples. | **07 Hrs** |
| **UNIT-V** | |
| **Emerging semiconductor devices (Qualitative approach):** Introduction, HEMT, HBT, Fin-FET. Nanowire-FET, quantum and molecular devices, energy storage and harvesting Electronics devices | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Apply semiconductor models to analyze carrier densities and carrier transport. |
| CO2: | Analyze basic governing equations to analyze semiconductor devices. |
| CO3: | Design the p-n junction, Schottky barrier diodes and emerging semiconductor devices. |
| CO4: | Simulate characteristics of a simple device using MATLAB, SPICE and ATLAS / SYNOPSYS |

| **Reference Books** | |
|---|---|
| **1.** | Semiconductor Device Fundamentals, Robert F. Pierret, 2006, Pearson, ISBN 9780201543933 |
| **2.** | Operation and Modeling of the MOS Transitor , Y.P. Tsividis, Colin McAndrew, 3rd Edition, 2014, Oxford Univ Press, ISBN:978-0195170153 |
| **3.** | Fundamentals of Modern VLSI Devices , Yuan Taur,Tak H. Ning, "",2nd edition , 2013 Cambridge University Press, ISBN: 978-1107635715 |
| **4.** | Semiconductor Simulation Tools, "https://nanohub.org/groups/semiconductors" |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **1** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO2** | **3** | **2** | **2** | **1** | **1** | **-** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO4** | **3** | **3** | **3** | **3** | **3** | **1** | **-** | **-** | **1** | **2** | **1** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **OBJECT ORIENTED PROGRAMMING IN C++ (Theory)** | | |
| **Course Code:** 16EC5A5 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Analyze the basic programming concepts and primitives of object-oriented programming. |
| **2** | Analyze new programming concept which should help in developing high quality software. |
| **3** | Interpret basic data structures & dimensionality of arrays to store data efficiently. |
| **4** | Design an algorithmic solution for a given problem |

| **UNIT-I** | |
|---|---|
| **Introduction to C++:** Procedure–Oriented Programming, Object Oriented Programming, Comparison of C++ with C, Input/output in C++, Bool data types, Enumerated data types, structures, Unions, Pointers, Pointer arithmetic, Pointers to different data types, Reference, Operators: new, delete, volatile, size of ,typecasting, Storage classes **Functions:** Function components, Function arguments, Function overloading, Function with default arguments, Inline function, #define macros, Function templates | **08 Hrs** |
| **UNIT-II** | |
| **Pointers & 1D Arrays**<br>Introduction, accessing array elements using pointers, pointer to strings, dynamic arrays, pointers to structures, passing pointers to functions.<br>**Classes and Objects**<br>Introduction to classes and objects, Member function and member data, Access specifiers, constructors, destructors, static members, friend function, friend class, Copy constructor, Overloaded assignment operator, this pointer, class templates. | **07 Hrs** |
| **UNIT-III** | |
| **Operator Overloading**<br>Operator overloading, overloading the increment and the Decrement operators (Prefix and Post fix), Overloading the Unary Minus and unary plus operator, Overloading the arithmetic operators, Over loading the relational operators, Overloading the insertion and extraction operator, Data Conversion using Member function. | **07 Hrs** |
| **UNIT-IV** | |
| **Data Representation using Arrays**<br>1-D arrays, arrays as a member of the class, creating array using dynamic constructors, array of object, strings, Implementation of stack and queue using arrays. **Data Representation using Linked List** Single-Linked List, Implementation of stack and queue using Linked list. | **07 Hrs** |
| **UNIT-V** | |
| **Inheritance**<br>Types of inheritance, Visibility mode, Function overriding, Need for virtual function, virtual function, Pure virtual function.<br>**Stream Handling**<br>Streams, Text Input/Output, Opening and Closing Files, Object Input/Output through Member Functions. Exception Handling in C++ | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Explain the concepts & constructs of object-oriented programming. |
| CO2: | Analyze the basic constructs, operations, control structures and advanced features of the C++ programming language and apply this knowledge to develop algorithms for given problem. |
| CO3: | Perform analysis of real-world problems and implement C++ software solutions to meet the industry requirements with the help of modern engineering tools. |
| CO4: | Engage in self-study as a team member/individual to formulate, design, implement, analyze and demonstrate the C++ software developed for a given assignments. |

| Reference Books | |
|---|---|
| **1.** | Mastering C++, K.RVenugopal, Rajkumar, T Ravishankar, 4th Edition, 2008, Tata McGraw-Hill Pubications, ISBN-13: 978-81-7758-373-1 |
| **2.** | Object-oriented Programming in Turbo C ++, Robert Lafore, 3rd Edition,2009, Galgotia Publishing House, |
| **3.** | C++:The Complete Reference ,Herbert Schildt, 4th Edition, 2007, McGraw-Hill, , ISBN-10: 0078824761/ ISBN-13: 978-0078824760 |
| **4.** | Object Oriented Programming with C++, E.Balagurusamy, 2008, Tata McGraw-Hill Publications, ISBN-13: 9780070669079 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

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| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | | | | | **3** | | | | | | | **2** |
| **CO2** | **3** | **3** | **3** | **2** | | | | **2** | **2** | | | **2** |
| **CO3** | **3** | **2** | **3** | **3** | **3** | | | **2** | **2** | | | |
| **CO4** | **3** | **3** | **3** | **3** | **3** | **1** | **1** | **3** | **3** | **3** | **2** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **COMPUTER ORGANISATION AND ARCHITECTURE (Theory)** | | |
| **Course Code:** 16EC5A6 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand the fundamentals of computer System and its Organization. |
| **2** | Appreciate the functionalities of basic processing unit and its control system in processing the Instruction. |
| **3** | Understand the role of bus system. |
| **4** | Develop a clear understanding on the pipelining. |
| **5** | Present an adequate Instruction Set Architectures for better understanding of the assembly level programming. |

| **UNIT-I** | |
|---|---|
| **Basic Structures of Computers:** Functional units, Basic Operational Concepts, Bus Structures, Performance measurement. **Machine Instructions and Programs:** Numbers, Number Notation, Arithmetic operations and characters. Memory Locations and Addresses, Memory Operation, Instruction and Instruction Sequencing, Addressing Modes, implementation of Variables & Constants, Indirection & pointers, Indexing & Arrays, Relative Addressing, Example Programs. | **08 Hrs** |
| **UNIT-II** | |
| **Machine Instructions and Programs:** Additional addressing Modes, Assembly Language, Stacks & Queues, Subroutines, Subroutine Nesting & Processor Stack, Parameter passing, The stack frame. Additional Instructions, Example programs. | **06 Hrs** |
| **UNIT-III** | |
| **Input / Output Organization:** Basic Input / Output Operations, Accessing I/O devices, Interrupts: Interrupt Hardware, Enabling & Disabling Interrupt, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access: Bus arbitration.<br>**Basics of memory:** Memory Hierarchy, Speed, Size and cost, Performance considerations: Hit Rate and miss penalty | **08 Hrs** |
| **UNIT-IV** | |
| **Arithmetic Operations:** Booth Algorithm, Fast Multiplication: Bit-pair Recording of Multipliers; Integer division; IEEE Standard for floating – point Numbers.<br>**Control Unit Logic:** Fundamental Concepts: Register Transfers, Performing an Arithmetic or Logic operation, Fetching a Word from Memory, Storing a Word in Memory, Execution of a Complete Instruction, Branch instruction. Multiple Bus Organization, Micro programmed control: Micro Instructions and its comparison with hardwired control. | **07 Hrs** |
| **UNIT-V** | |
| **Pipelining:** Basic concepts: Role of Cache Memory, Pipeline Performance; data hazards: Operand forwarding, Handling Data Hazards in software, Side Effects; Instruction Hazards: Unconditional Branches, Conditional Branches: delayed branch; Influence on Instruction sets. **Super Scalar Operation:** Out-of-order Execution, Execution Completion, Dispatch Operations. | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Analyze the basic operation and organization of computer system |
| CO2: | Identify the design requirements in organizing computer system components |
| CO3: | Develop assembly language program for different instruction set architecture and its data representation |
| CO4: | Examine the different interfaces of a computer system |

| **Reference Books** | |
|---|---|
| **1.** | Computer Organization, Carl Hamacher, Z Vranesic& S Zaky, 5th Edition, 2011, Mc Graw Hill, ISBN 10: 1259005275 / ISBN 13: 9781259005275. |
| **2.** | Computer Organization and Architecture: Designing for Performance, William Stallings, 8th edition, 2010, Prentice Hall, ISBN-13: 978-0-13-607373-4 ISBN-10: 0-13-607373-5. |
| **3.** | Computer Organization and Design, David A. Patterson & John L. Hennessy, 5th Edition, 2013 Morgan Kaufmann, ISBN : 9780124077263 |
| **4.** | Fundamentals of Computer Organization and Architecture, Mostafa Abd-El-Barr, Hesham El-Rewini, 2005, Wiley publishers, ISBN10: 0-471-46741-3. |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **1** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO2** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **3** | **-** | **-** | **-** | **2** | **1** | **-** | **2** |
| **CO4** | **3** | **3** | **3** | **3** | **3** | **-** | **-** | **-** | **2** | **1** | **-** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: V** | | |
|---|---|---|
| **ROBOTICS (Theory)** | | |
| **Course Code:** 16EC5A7 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Explain the basic principles of Robotic technology, configurations, control and programming of Robots. |
| **2** | Describe the concept of Robot kinematics and dynamics, latest algorithms & analytical Approaches. |
| **3** | Discuss and apply the concepts of dynamics for a typical Pick and Place robot |
| **4** | Choose the appropriate Sensor and Machine vision system for a given application. |

| **UNIT-I** | |
|---|---|
| **Introduction:** Automation and Robotics, Historical Development, Definitions, Basic Structure of Robots, Robot Anatomy, Complete Classification of Robots, Fundamentals about Robot Technology, Factors related to use Robot Performance, Basic Robot Configurations and their Relative Merits and Demerits, the Wrist & Gripper Subassemblies. | **07 Hrs** |
| **UNIT-II** | |
| **Kinematics of Robot Manipulator:** Introduction, Geometry Based Direct kinematics problem, Composite Rotation matrix, Homogenous Transformations, Robotic Manipulator, Joint Co-Ordinate System, Roll Pitch-Yaw (RPY) Transformation. DH Representation & Displacement Matrices for Standard Configurations, Jacobian Transformation in Robotic Manipulation. | **07 Hrs** |
| **UNIT-III** | |
| **Trajectory Planning:** – Introduction, Trajectory Interpolators, Basic Structure of Trajectory Interpolators, Cubic Joint Trajectories. General Design Consideration on Trajectories. | **07 Hrs** |
| **UNIT-IV** | |
| **Dynamics of Robotic Manipulators:** Introduction, Preliminary Definitions, Generalized Robotic Coordinates, Jacobian for a Two link Manipulator, Euler Equations, The Lagrangian Equations of motion. Dynamic Modeling of Robotic Manipulators: - Velocity of Joints, Kinetic Energy of Arm, Potential Energy of Robotic Arm, The Lagrange, Two Link Robotic Dynamics with Distributed Mass. | **07 Hrs** |
| **UNIT-V** | |
| **Robot Sensing & Controlling:** Various Sensors and their Classification, Use of Sensors and Sensor Based System in Robotics, Machine Vision System, Description, Sensing, Digitizing, Image Processing, Analysis and Application of Machine Vision System, Robotic Assembly Sensors and Intelligent Sensors. Industrial Applications: Automation in Manufacturing, Robot Application in Industry, Task Programming, Robot Intelligence and Task Planning, Modern Robots, Goals of AI Research and AI Techniques- Case Study. | **08 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Explain the basic principles of Robotic technology, configurations, control and programming of Robots. |
| CO2: | Describe the concept of Robot kinematics and dynamics, latest algorithms & analytical Approaches. |
| CO3: | Discuss and apply the concepts of dynamics for a typical Pick and Place robot |
| CO4: | Choose the appropriate Sensor and Machine vision system for a given application. |

| **Reference Books** | |
|---|---|
| **1.** | Robotics, control vision and intelligence, Fu, Lee and Gonzalez, 2nd edition, 2007, McGraw Hill International publication |
| **2.** | Introduction to Robotics, John J. Craig, 3rd edition, 2010, Addison Wesley Publishing |
| **3.** | Robotics for Engineers, Yoram Koren, 1st edition, 1985, McGraw Hill International |
| **4.** | Robotics Engineering-An Integrated Approach ,Klafer, Chmielewski and Negin, 1st Edition, 2009, PHI. |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **2** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **-** | **-** | **-** | **2** | **1** | **-** | **1** |
| **CO3** | **2** | **3** | **2** | **2** | **2** | **-** | **1** | **-** | **1** | **1** | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **1** | **-** | **-** | **-** | **1** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: V(Global Elective-B)** | | |
|---|---|---|
| **Artificial Neural Networks &Deep Learning** | | |
| **Course Code:** 16G5B05 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 4:0:0:0 | | **SEE Marks:** 100 |
| **Hours:** 46L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Define what is Neural Network and model a Neuron and Express both Artificial Intelligence and Neural Network |
| **2** | Analyze ANN learning, Error correction learning, Memory-based learning, Hebbian learning, Competitive learning and Boltzmann learning |
| **3** | Implement Simple perception, Perception learning algorithm, Modified Perception learning algorithm, and Adaptive linear combiner, Continuous perception, learning in continuous perception. |
| **4** | Analyze the limitation of Single layer Perceptron and Develop MLP with 2 hidden layers, Develop Delta learning rule of the output layer and Multilayer feed forward neural network with continuous perceptions, |

| **UNIT-I** | |
|---|---|
| **Introduction to Neural Networks:** Neural Network, Human Brain, Models of Neuron, Neural networks viewed as directed graphs, Biological Neural Network, Artificial neuron, Artificial Neural Network architecture, ANN learning, analysis and applications, Historical notes. | **08 Hrs** |
| **UNIT-II** | |
| **Learning Processes:** Introduction, Error correction learning, Memory-based learning, Hebbian learning, Competitive learning, Boltzmann learning, credit assignment problem, learning with and without teacher, learning tasks, Memory and Adaptation. | **10 Hrs** |
| **UNIT-III** | |
| **Single layer Perception:** Introduction, Pattern Recognition, Linear classifier, Simple perception, Perception learning algorithm, Modified Perception learning algorithm, Adaptive linear combiner, Continuous perception, Learning in continuous perception. Limitation of Perception. | **10 Hrs** |
| **UNIT-IV** | |
| **Multi-Layer Perceptron Networks:** Introduction, MLP with 2 hidden layers, Simple layer of a MLP, Delta learning rule of the output layer, Multilayer feed forward neural network with continuous perceptions, Generalized delta learning rule, Back propagation algorithm | **10 Hrs** |
| **UNIT-V** | |
| **Introduction to Deep learning**: Neuro architectures as necessary building blocks for the DL techniques, Deep Learning & Neocognitron, Deep Convolutional Neural Networks, Recurrent Neural Networks (RNN), feature extraction, Deep Belief Networks, Restricted Boltzman Machines, Autoencoders, Training of Deep neural Networks, Applications and examples (Google, image/speech recognition) | **08 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| **CO1:** | Model Neuron and Neural Network, and to analyze ANN learning, and its applications. |
| **CO2:** | Perform Pattern Recognition, Linear classification. |
| **CO3:** | Develop different single layer/multiple layer Perception learning algorithms |
| **CO4:** | Design of another class of layered networks using deep learning principles. |

| **Reference Books** | |
|---|---|
| **1.** | Neural Network- A Comprehensive Foundation , Simon Haykins, 2nd Edition, 1999, Pearson Prentice Hall, ISBN-13: 978-0-13-147139-9 |

| | |
|---|---|
| **2.** | Introduction to Artificial Neural Systems, Zurada and Jacek M, 1992, West Publishing Company, ISBN: 9780534954604 |
| **3.** | Learning & Soft Computing, Vojislav Kecman, 1st Edition, 2004, Pearson Education, ISBN:0-262-11255-8 |
| **4.** | Neural Networks Design, M T Hagan, H B Demoth, M Beale, 2002, Thomson Learning, ISBN-10: 0-9717321-1-6/ ISBN-13: 978-0-9717321-1-7 |


**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Assignment. A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 60. The marks component for assignment is 10. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **FOUNDATIONS OF MANAGEMENT & ECONOMICS (Theory & Practice) (COMMON TO CS, EC, EE, IS, TC)** | | |
| **Course Code:** 16HEM61 | | **CIE Marks:** 50 |
| **Credits: L:T:P:S:** 2:0:0:0 | | **SEE Marks:** 50 |
| **Hours:** 23L | | **SEE Duration:** 2 Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand the evolution of management thought. |
| **2** | Acquire knowledge of the functions of Management. |
| **3** | Gain basic knowledge of essentials of Micro economics and Macroeconomics. |
| **4** | Understand the concepts of macroeconomics relevant to different organizational contexts. |

| **UNIT-I** | |
|---|---|
| **Introduction to Management:** Management Functions, Roles & Skills, Management History – Classical Approach: Scientific Management & Administrative Theory, Quantitative Approach: Operations Research, Behavioral Approach: Hawthorne Studies, Contemporary Approach: Systems & Contingency Theory. | **04 Hrs** |
| **UNIT-II** | |
| **Foundations of Planning:** Types of Goals & Plans, Approaches to Setting Goals & Plans, Strategic Management Process, Corporate & Competitive Strategies.<br>**Organizational Structure & Design:** Overview of Designing Organizational Structure: Work Specialization, Departmentalization, Chain of Command, Span of Control, Centralization & Decentralization, Formalization, Mechanistic & Organic Structures. | **05 Hrs** |
| **UNIT-III** | |
| **Motivating Employees:** Early Theories of Motivation: Maslow's Hierarchy of Needs Theory, McGregor's Theory X & Theory Y, Herzberg's Two Factor Theory, Contemporary Theories of Motivation: Adam's Equity & Vroom's Expectancy Theory.<br>**Managers as Leaders:** Behavioral Theories: Ohio State & University of Michigan Studies, Blake & Mouton's Managerial Grid, Contingency Theories of Leadership: Hersey & Blanchard's Situational Leadership, Contemporary Views of Leadership: Transactional & Transformational Leadership. | **06 Hrs** |
| **UNIT-IV** | |
| **Introduction to Economics:** Concept of Economy and its working, basic problems of an Economy, Market mechanism to solve economic problems, Government and the economy,<br>**Essentials of Micro Economics:** Concept and scope, tools of Microeconomics, themes of microeconomics, Decisions: some central themes, Markets: Some central themes, Uses of Microeconomics. . | **04Hrs** |
| **UNIT-V** | |
| **Essentials of Macroeconomics:** Prices and inflation, Exchange rate, Gross domestic product (GDP) , components of GDP, the Labor Market, Money and banks, Interest rate, Macroeconomic models- an overview, Growth theory, The classical model, Keynesian cross model, IS-LM-model, The AS-AD-model, The complete Keynesian model, The neo-classical synthesis, Exchange rate determination and the Mundell-Fleming model. | **04 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Explain the principles of management theory & recognize the characteristics of an organization. |
| CO2: | Demonstrate the importance of key performance areas in strategic management and design appropriate organizational structures and possess an ability to conceive various organizational dynamics. |

| | |
|---|---|
| CO3: | Select & Implement the right leadership practices in organizations that would enable systems orientation. |
| CO4: | Understand the basic concepts and principles of Micro economics and Macroeconomics |

| **Reference Books** | |
|---|---|
| **1.** | Management, Stephen Robbins, Mary Coulter & Neharika Vohra, 10th Edition, Pearson Education Publications, , ISBN: 978-81-317-2720-1. |
| **2.** | Management, James Stoner, Edward Freeman & Daniel Gilbert Jr, 6th Edition, PHI, ISBN: 81-203-0981-2. |
| **3.** | Microeconomics, Douglas Bernheim B & Michael D Whinston, 2009 Edition, TMH Pub.Co.Ltd, ISBN: 13:978-0-07-008056-0. |
| **4.** | Macroeconomics: Theory and Policy, Dwivedi. D.N, 3rd Edition, 2010, McGraw Hill Education, ISBN-13: 978-0070091450. |
| **5.** | Essentials of Macroeconomics, Peter Jochumzen, 1st Edition, e-book(www.bookboon.com), 2010, ISBN:978-87-7681-558-5. |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Assignment. A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 60. The marks component for assignment is 10. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level. .

| **.CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **-** | **1** | **-** | **-** | **3** | **-** | **3** | **3** | **3** | **3** | **3** |
| **CO2** | **3** | **2** | | **-** | **-** | **-** | **-** | **1** | **2** | **3** | **2** | **2** |
| **CO3** | **-** | **-** | **1** | **-** | **-** | **2** | **-** | **2** | **2** | **3** | **3** | **3** |
| **CO4** | **2** | **-** | **2** | **-** | **-** | **3** | **1** | **3** | **2** | **2** | **3** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **COMMUNICATION SYSTEM II (Theory & Practice)** | | |
| **Course Code:** 16EC62 | | **CIE Marks:** 100+50 |
| **Credits: L:T:P:S:** 4:0:1:0 | | **SEE Marks:** 100+50 |
| **Hours:**46L | | **SEE Duration:** 03Hrs+03Hrs |
| **Course Learning Objectives: The students will be able to** | | |
| **1** | Identify the digital communication system as a series of functional blocks and the concepts of signal and channel representation. | |
| **2** | Apply the concept of signal conversion to symbols and symbol processing in transmitter and receiver blocks. | |
| **3** | Compute performance issues and parameters for symbol processing and recovery in ideal and corrupted channel conditions. | |
| **4** | Compute and mitigate for performance parameters in corrupted and distorted channel conditions. | |

| **UNIT-I** | |
|---|---|
| **Digital Communication Transmitter:** Digital communication blocks and impediments. Review of Lowpass and Bandpass signals. Geometric Representation of Signals in terms of a low pass basis set, Gram Schmidt procedure, conversion statement to bandpass basis set. Geometric representation of baseband modulated signals as examples Geometric representation of low pass equivalents of bandpass signals - BPSK, QPSK, M-PSK, M-QAM. Transmitter Architectures and, Computation of Transmit PSD. Applications to GPRS, 3G. Orthogonal symbol modulation – Geometric representation of BFSK, MSK (Simple Cases). Applications to GSM, Training. | **10 Hrs** |
| **UNIT-II** | |
| **Communication through AWGN Channels:** Demodulation and Detection - Center point sampling, Matched Filter, and Correlation Receiver. **Estimation Basics** - MAP and MLI Estimation of Binary signals with AWGN, Probability of error for binary signaling, Probability of error for binary baseband pulses (Line codes) using center point sampling and Matched filters. **Coherent demodulation scheme** – Receiver Architecture, Probability of symbol error for BPSK, QPSK, BFSK. **Coherent Demodulation scheme for multiple signals** – M-PAM, M-PSK and M-QAM. Union Bounded Probability of error these signals, Lower and upper bounds. | **09 Hrs** |
| **UNIT-III** | |
| **Communication Through AWGN Signals** (contd) - Non-Coherent demodulation of BFSK and DPSK – Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (Without derivation).<br>**Communication through Band Limited Channels:** Digital Transmission through Band limited channels - Inter Symbol Interference, Signal design for Band limited ideal channel with zero ISI – Nyquist Criterion (statement only), Sinc and Raised pulse shaping.<br>Signal design for Band limited channel with controlled ISI – Correlative coding, DB and MDB, with and without Precoding. | **09 Hrs** |
| **UNIT-IV** | |
| **Convolution Codes**: Encoding of convolution Codes, Transfer function and distance properties, Maximum Likelihood sequence decoding – Viterbi search Algorithm with Hard and soft decision, Probability of error statement only (No derivation). | **09 Hrs** |
| **UNIT-V** | |
| **Principles of Spread Spectrum (SS)** Concept of Spread Spectrum, Direct Sequence/SS, Frequency Hopped SS, Processing Gain, Interference, and probability of error statement only. **PN sequences for Spread Spectrum** – M- sequences with Properties; Gold, Kasami sequences with basic properties. Spread Spectrum Synchronization (Block diagram treatment) - Code Acquisition and Tracking. | **09 Hrs** |

| **Practical's: Communication systems 2 Lab** | |
|---|---|
| 1. Pulse Amplitude Modulation and Demodulation<br>2. ASK Modulation and Demodulation<br>3. FSK modulation and demodulation<br>4. BPSK modulation and demodulation<br>5. QPSK modulation and DPSK modulation and demodulation<br>6. MSK Modulation & Demodulation<br>7. QAM modulation and demodulation<br>8. Convolution coding decoding<br>9. Correlative coding and Study of Inter symbol Interference using eye pattern<br>10. Spread Spectrum sequences | |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Associate and apply the concepts of Bandpass sampling to well specified signals and channels. |
| CO2: | Analyze and compute performance parameters and transfer rates for low pas and bandpass symbol under ideal and corrupted non band limited channels. |
| CO3: | Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels. |
| CO4: | Demonstrate by simulation and emulation bandpass signals subjected to convolution coding and symbol processed at transmitter and correspondingly demodulated and estimated at receiver after passing through a corrupted channel. |

| **Reference Books** | |
|---|---|
| **1.** | Communication Systems, Simon Haykin and Michael Moher, 5th Edition, 2014, John Wiley and sons, ISBN-978 81 265 2151 7. |
| **2.** | Communication systems, Simon Haykin, 3rd or 4th Edition, Reprinted 2013, John Wiley & sons, ISBN 0-471- 17869-1. |
| **3.** | Modern Digital and Analog communication Systems, B.P.Lathi and Zhi Ding, 4th Edition, 2010, Oxford University Press, , ISBN: 9780198073802.. |
| **4.** | Digital Communications, Ian A. Glover, Peter M. Grant, 3rd Edition, 2010, Pearson Educations, ISBN:978-0-273-71830-7 |
| **5.** | Communication System, Bruce Carlson and P.B Chilly, 5th Edition,2011, Tata McGraw-Hill, |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Assignment. A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 60. The marks component for assignment is 10. The total marks of CIE are 100.

**Laboratory- 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 40 marks. At the end of the semester a test is conducted for 10 marks. Total marks for the laboratory is 50.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**Laboratory- 50 Marks**

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **3** | **-** | **-** | **1** | **-** | **1** | **-** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **3** | **-** | **-** | **1** | **-** | **1** | **-** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **3** | **-** | **-** | **1** | **-** | **1** | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **3** | **-** | **-** | **1** | **-** | **1** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **COMPUTER COMMUNICATION NETWORKS (Theory & Practice)** | | |
| **Course Code:** 16EC63 | | **CIE Marks:** 100+50 |
| **Credits: L:T:P:S:** 3:0:1:1 | | **SEE Marks:** 100+50 |
| **Hours:** 36L | | **SEE Duration:** 03Hrs+03Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Develop awareness towards basic internetworking principles. |
| **2** | Analyze various aspects involved in multiple accesses, various data switching techniques. |
| **3** | Explain protocols operating at different layers of computer networks |
| **4** | Analyze various data compression techniques and security issues. |
| **5** | Analyze various aspects involved in network control and traffic management. |

| **UNIT-I** | |
|---|---|
| **Computer Networks and the Internet**: Internet, Protocol, Network Edge, Network Core, Access Networks and Physical Media, Delay and Loss in Packet-Switched Networks, Protocol Layers and Their Service Models, Internet Backbones, NAPs, and ISPs. Network models, OSI, TCP/IP. Physical Layer: Introduction to Guided and unguided physical media**.** | **07Hrs** |
| **UNIT-II** | |
| **Local Area Networks and Connecting Devices:**<br>Data Link layer Services, Data link control-Framing, Flow & error control, Multiple Access Protocols-Random Access protocols<br>LAN Addresses and ARP, IEEE 802.3 LANs, Ethernet, Hubs, Bridges, and Switches, Virtual LAN, PPP: The Point-to-Point Protocol, X.25 and Frame Relay. IEEE 802.11 LANs | **07 Hrs** |
| **UNIT-III** | |
| **Network Layer-Logical Addressing& Internet Protocol**<br>Network Layer, Logical Addressing, IPV4 Addresses, Structure, Address Space, Classful Addressing, Classless Addressing, Network Address Translation.<br>IPv6 Addresses, Structure, Address Space of IPV6, Transition from IPV4 to IPV6<br>Forwarding. Subnet addressing. Inter- and intra-domain routing. Datagram networks; virtual circuits. RIP, OSPF, BGP. CI | **07 Hrs** |
| **UNIT-IV** | |
| **Transport Layer:** Process to Process Delivery, Connectionless Versus Connection Oriented Service, UDP, TCP.<br>Congestion control and resource allocation-Issues in resource allocation, Queuing disciplines congestion control. Slow start. Fast retransmit. Fast recovery. Rate-based congestion control. Congestion avoidance mechanisms. Leaky Bucket Algorithm | **07 Hrs** |
| **UNIT-V** | |
| **Naming and the DNS.**<br>Cell switching & ATM service classes. Switch architectures. Switching fabrics. Space-division multiplexing vs. shared-memory switches. Source Coding. Data Compression, Security and Cryptography | **08 Hrs** |
| **Practical's: CCN Lab**<br>**Practical's: Computer Communication Networks Lab**<br>**Part –I: Experiments Using C/C++ programming.**<br>1) a)Implement Bit stuffing Algorithm<br>b)Character stuffing algorithms and<br>c)Cyclic Redundancy Check codes for error detection using C programs.<br>2) Implement Encryption and Decryption algorithms using C program.<br>3) Implement following Minimum Spanning Tree algorithms using C program<br>i) Kruskal's Algorithm | |

| | |
|---|---|
| ii) Prim's Algorithms<br>4) Implement STOP and WAIT protocol using socket programming concept using C Program.<br>5) Implement RSA algorithm using C program.<br>**Part-II: Experiments that may be carried out using QualNet/NS-3/Packet Tracer**<br>1 Simulate & Analyze CSMA/CD and CSMA/CA Protocols.<br>2 Test and verify Network configurations using Packet Tracer.<br>3 Configure Inter VLAN network using Packet Tracer<br>4 Configure and test a given network using Packet Tracer<br>Simulation of congestion control algorithms using NS-3 | |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Acquire the knowledge of network architecture, topologies and security issues. |
| CO2: | Design a network for given configuration by assigning IP addresses. |
| CO3: | Analyze various aspects involved in network control and traffic management |
| CO4: | Analyze the performance of various scheduling algorithms |

| **Reference Books** | |
|---|---|
| **1.** | Computer Networks- A System Approach, Larry L Peterson, Bruce S Davie, 4th edition, 2007, ELSEVIER publication, ISBN: 978-0123705488 |
| **2.** | Data Communication and Networking, B Forouzan, 4th Edition, 2006, TMH, ISBN: 0-07-010829-3 |
| **3.** | Computer Networks, James F. Kurose, Keith W. Ross, 2nd Edition, 2003, Pearson Education, ISBN: 0199217637 |
| **4.** | Computer Communication Networks, Andrew S Tanenbaum and David J Wetherall, 5th Edition, 2010, Person Education. |
| **5.** | Introduction To Data Compression, Sayood Khalid, 3rd Edition, Elsevier, 2010, ISBN: 978-8131206249 |

**Continuous Internal Evaluation (CIE): Total marks: 100+50=150**

**Theory – 100 Marks**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total CIE for theory is 100.

**Laboratory- 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 40 marks. At the end of the semester a test is conducted for 10 marks. Total marks for the laboratory is 50.

**Semester End Evaluation (SEE): Total marks: 100+50=150**

**Theory – 100 Marks**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**Laboratory- 50 Marks**

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **ANALOG AND MIXED SIGNAL IC DESIGN (Theory)** | | |
|---|---|---|
| **Course Code:** 16EC64 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:1:0:0 | | **SEE Marks:** 100 |
| **Hours:**36L+24T | | **SEE Duration:** 03Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Design basic amplifiers, differential amplifiers and current mirrors using MOSFETs. |
| **2** | Design different opamp topologies for a given specification using CAD tools |
| **3** | Analyze stability of OPAMPs and apply the appropriate compensation technique. |
| **4** | Analyze amplifier circuits by considering noise effects & Design and analyze sampling switches and switched capacitor amplifiers |

| **UNIT-I** | |
|---|---|
| **Introduction to Analog Integrated Design:** Models for analog design, output resistance ($r_o$), body transconductance, transition frequency: **Single-stage Amplifiers** – CS stage, diode connected load, current source load and source degeneration, review of CD and CG stages (all amplifier analysis with body effect), Cascode stage & folded cascode concepts. Design of amplifier from specifications. **Differential Amplifiers** – Half circuit analysis, Common mode response. | **08 Hrs** |
| **UNIT-II** | |
| **Current mirror –** Cascode current mirror, active current mirror – analysis.<br>**Operational Amplifiers:** General considerations – performance parameters, One-Stage Op amps – cascode opamps, telescopic opamps, folded cascode opamps, Two-Stage Op amps, Gain Boosting, Comparison of performance of various opamp topologies. Design of opamps from specifications. | **08 Hrs** |
| **UNIT-III** | |
| **Stability and Frequency Compensation:** Frequency response of CS amplifier - Miller effect, poles in a system, pole-splitting, Miller compensation. Two stage opamp - Compensation techniques, gain-phase crossovers, closed-loop stability, optimal phase margin.<br>**Noise:** MOSFET noise models, types of noise – thermal, flicker, Representation of noise in circuits, Noise in single stage amplifiers (Common source only). | **08 Hrs** |
| **UNIT-IV** | |
| **Bandgap references**: Temperature independent references - Bipolar CTAT, PTAT, Band gap references (BGR)<br>**Introduction to Switched-capacitor Circuits: Sampling** Switches – MOSFETs as switches, Distortion due to switch, Channel Charge injection, Capacitive feedthrough, bottom plate sampling, Parasitic insensitive Switched Capacitor Integrator, Switched Capacitor Common-Mode Feedback | **06 Hrs** |
| **UNIT-V** | |
| **Data Converter Fundamentals:** Digital-to-Analog Converter Specifications, Analog-to-Digital Converter Specifications. **DAC Architectures:** Current Steering DAC **ADC Architectures -** Successive Approximation ADC, Oversampling ADC - Benefits of oversampling, First Order Sigma Delta ADC. | **06 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Apply the knowledge of MOSFET & amplifiers to investigate various design trends of analog IC design |
| CO2: | Analyze the functionality of analog/mixed signal circuits & systems |
| CO3: | Design and implement analog integrated circuits |
| CO4: | Evaluate the different performance parameters of analog/mixed signal integrated circuits |

| Reference Books | |
|---|---|
| **1.** | Design of Analog CMOS Integrated Circuits, Behzad Razavi, 2002, Mc GrawHill Edition, ISBN: 0-07-238032-2 |
| **2.** | CMOS Circuit Design, Layout and Simulation, R. Jacob Baker, Harry W. Li and David E. Boyce, 2002, IEEE Press, ISBN: 81-203-1682-7 |
| **3.** | CMOS Mixed-signal Circuit Design, R. Jacob Baker, 2009, IEEE Press, ISBN: 978-81-265-1657-5 |
| **4.** | Analysis and Design of Analog Integrated Circuits, Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "", 4th edition, 2008, Wiley India Private Limited, ISBN:978-8126515691 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Assignment. A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 60. The marks component for assignment is 10. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **3** | **3** | **3** | **3** | **-** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO2** | **3** | **2** | **3** | **-** | **3** | **-** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **3** | **-** | **-** | **-** | **2** | **-** | **-** | **2** |
| **CO4** | **3** | **3** | **-** | **2** | **3** | **-** | **-** | **-** | **2** | **-** | **-** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **CRYPTOGRAPHY & NETWORK SECURITY (Theory)** | | |
| **Course Code:** 16EC6C1 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:**36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Analyze the needs, principles and practices of cryptography and network security |
| **2** | Evaluate conventional encryption algorithms and design principles. |
| **3** | Analyze the use of conventional encryption for confidentiality & evaluate public key algorithm design issues. |
| **4** | Apply the knowledge of message authentication codes and hash functions to provide authentication. |

| **UNIT-I** | |
|---|---|
| **Introduction**<br>Services, Mechanism and attacks, OSI security architecture, Model for network security,<br>**Classical Encryption Techniques**<br>Symmetric cipher model, Substitution techniques, Transposition techniques, Simplified DES. Problems<br>**Block Ciphers and DES (Data Encryption Standards)**<br>Simplified DES Block, Cipher Principles, DES and strength of DES, Block cipher design principles and modes of operation, The AES Cipher. | **08 Hrs** |
| **UNIT-II** | |
| **Public Key Cryptography and RSA**<br>Principles of public key cryptosystems, RSA algorithm. Problems<br>**Other Public Key Cryptosystems and Key Management**<br>Key Management, Diffie-Hellman exchange, Elliptic curve arithmetic, Elliptic curve cryptography.<br>**Message Authentication and Hash Functions**<br>Authentication requirements, Authentication functions, Message Authentication codes, Hash functions, Security of Hash functions and MAC's | **07 Hrs** |
| **UNIT-III** | |
| **Digital Signature and Authentication Protocol:** Digital signature, Authentication protocols, Digital signature standard. **Authentication Applications** Kerberos encryption technique, Problems. | **07 Hrs** |
| **UNIT-IV** | |
| **Transport-Level Security: Web security Issues,** Security socket layer (SSL) and Transport layer Security, HTTPS and Secure Shell<br>**Wireless network security:** IEEE 802.11 Wireless LAN Overview, IEEE 802.11i Wireless LAN Security, Wireless application Protocol Overview, wireless transport layer Security, WAP End-End Security | **07 Hrs** |
| **UNIT-V** | |
| **Electronic Mail Security** Pretty good privacy, S/MIME, Data compression using ZIP, Radix-64 conversion, PGP random number generator. **IP Security** IP security architecture, Authentication header, ESP (encapsulating security pay load), Security associations, Key management, Problems | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Identifying external and internal threats to an organization. |
| CO2: | Master fundamentals of secret, public key cryptography and Analyze advanced security issues and technologies. |
| CO3: | Evaluate & Compare different encryption algorithms. |
| CO4: | Use of modern tools for implementing different security algorithms and comparing their robustness. |

| Reference Books | |
|---|---|
| **1.** | Cryptography and Network Security, William Stallings, 5th Edition, 2003, Prentice Hall of India, ISBN 10: 0-13-609704-9/ISBN 13: 978-0-13-609704-4 |
| **2.** | Network Security: Private Communication in a Public World, Kaufman, R. Perlman, and M. Speciner, 2nd Edition, 2002, Pearson Education (Asia), ISBN13: 9780130460196 |
| **3.** | Cryptography and Network Security,Atul Kahate, 2003, Tata McGraw-Hill, ISBN 13:9781259029882 |
| **4.** | Fundamentals of Network Security, Eric Maiwald, 2003, McGraw-Hill, ISBN-13:978-0072230932 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO2** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO3** | **2** | **3** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO4** | **2** | **3** | **3** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **REAL TIME EMBEDDED SYSTEMS (Theory)** | | |
| **Course Code:** 16EC6C2 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand functional differences between different real time systems. |
| **2** | Examine and evaluate the hardware functionality required by embedded system to achieve real-time operation. |
| **3** | Analyse, evaluate and implement task control and real-time scheduling algorithms required to perform multitasking. |
| **4** | Demonstrate the concept of real-time programming using tasks and gain knowledge and skills necessary to design and develop embedded applications by means of real-time operating systems. |

| **UNIT-I** | |
|---|---|
| **Introduction:** Overview, Architecture Real Time Systems, Real Time Services, Real Time Standards, **System Resources:** Resource Analysis, Real Time Service Utility, Cyclic Executives **Basics of RTOS:** Kernel Features, Real-time Kernels: Polled Loops System, Co-routines, Interrupt-driven System, Multi-rate System; Processes, Threads, Tasks, States, Context Switching: Cooperative Multi-tasking, Pre-emptive Multi-tasking | **08 Hrs** |
| **UNIT-II** | |
| **Processing:** Scheduling Classes, Scheduler Concepts, Pre-emptive Fixed Priority Policy, Feasibility, Rate Monotonic LUB, Necessary & Sufficient Feasibility, Dead Line Monotonic, Dynamic Priority Policies **I/O Resources:** WCET, Intermediate I/O, Execution Efficiency **Memory:** Physical Hierarchy, Cache, Memory Planning, Memory shadowing | **07 Hrs** |
| **UNIT-III** | |
| **RTOS Services:** Task Creation, Inter Task Communication: Pipes, Message Queues, Mail Box, Memory Mapped Objects; Critical Section, Shared Data Problem, Synchronization: Signals, Semaphores Mutex; Remote Procedure and Sockets, Real Time Memory Management: Process Stack Management, Dynamic Allocation | **07 Hrs** |
| **UNIT-IV** | |
| **Timer & Timer Services:** Real Time Clocks & System Clocks, Programmable Interval Timers, Timer Interrupt Service Routine, Soft-timer Handling, Soft Timers elated Task **Synchronization Issues:** Resource Classification, Racing, Deadlock, Live lock, Starvation, Priority Inversion, Priority Ceiling & Inheritance | **07 Hrs** |
| **UNIT-V** | |
| **Examples of Real Time OS:** Vx-Works, RTX-ARM: Task Management, Scheduling, Primitive Kernel Services, Application Program development using APIs | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Understand the fundamental concepts of real-time system and real-time operating system. |
| CO2: | Analyze given requirements, design hardware & software for real time systems. |
| CO3: | Apply modern engineering tools for real time firmware development & performance analysis. |
| CO4: | Verify the specifications of various real time operating systems used for meeting timing constraints of given problem. |

| Reference Books | |
|---|---|
| **1.** | Real-Time Embedded Systems and Components, Sam Siewert, 2007, Cengage Learning India Edition, ISBN: 9788131502532 |
| **2.** | Real time systems, Krishna CM and Kang Singh G, 2003, Tata McGraw Hill, ISBN: 0-07-114243-64 |
| **3.** | Real-Time Concepts for Embedded Systems, Qing Li and Carolyn Yao, 2003 CMP Books, ISBN:1578201241 |
| **4.** | Real Time Systems, Jane W. S. Liu, 2000, Prentice Hall, ISBN:0130996513 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **1** | **1** | **1** | **2** | **-** | **-** | **-** | **-** | **-** | | **-** | |
| **CO2** | **3** | **2** | **2** | **1** | **2** | **1** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **3** | **1** | **1** | **1** | **-** | **1** | **-** | **1** |
| **CO4** | **2** | **3** | **2** | **2** | **1** | **1** | **2** | **2** | **2** | **2** | **2** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **IMAGE PROCESSING (Theory)** | | |
| **Course Code:** 16EC6C3 | | **CIE Marks:** 100 |
| **Credits: L: T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Get an introduction to basic concepts and methodologies of Digital Image processing, image formation and color image representation |
| **2** | Differentiate between the image enhancement and restoration techniques. Enhance the image by various methods in spatial and frequency domain. Perform image restoration using convolution, discrete linear operators and filters |
| **3** | Perform image segmentation using different algorithms suitable for various applications. |
| **4** | Recognize the different image patterns using supervised and unsupervised classification algorithms. |

| **UNIT-I** | |
|---|---|
| **Digital Image Fundamentals**<br>Fundamentals of Image Processing, Applications of Image Processing, Components of Image Processing System, Image Formation, Representation. | **08 Hrs** |
| **UNIT-II** | |
| **Image Enhancement & Restoration**<br>Distinction between image enhancement and restoration, Spatial Image Enhancement Techniques, Histogram-based Contrast Enhancement, Frequency Domain Methods of Image Enhancement, Noise Modeling, Image Restoration, Image Reconstruction. | **07 Hrs** |
| **UNIT-III** | |
| **Image Segmentation**<br>Edge, Line, and Point Detection, Edge Detector, Image Thresholding Techniques, Region Growing, Waterfall algorithm for segmentation, Connected component labeling. | **07 Hrs** |
| **UNIT-IV** | |
| **Recognition of Image Patterns**<br>Decision Theoretic Pattern Classification, Bayesian Decision Theory, Nonparametric Classification, Linear Discriminant Analysis, Unsupervised Classification Strategies – clustering, K-Means Clustering Algorithm. | **07 Hrs** |
| **UNIT-V** | |
| **Texture and Shape Analysis**<br>Introduction, Gray Level Co-occurrence Matrix, Texture Classification using Fractals, Shape Analysis, Region Based Shape Descriptors,<br>**Morphological image processing**<br>Preliminaries, Dilation and Erosion, Opening and Closing, the Hit-or-Miss Transformation, Some Basic Morphological Algorithms | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Understand digital image processing fundamentals: hardware and software, digitization, enhancement and restoration, encoding, segmentation, feature detection |
| CO2: | Apply image processing techniques in both the spatial and frequency (Fourier) domains |
| CO3: | Write image processing programs in MATLAB |
| CO4: | Perform image segmentation using different algorithms suitable for various applications. |

| Reference Books | |
|---|---|
| **1.** | Image Processing-Principles and Applications, Tinku Acharya and Ajoy K. Ray, 2005, John Wiley & Sons Inc., ISBN: 978-0-471-71998-4. |
| **2.** | Digital Image Processing, Rafael C. Gonzalez and Richard E. Woods, 2001, Pearson Education Edition, ISBN 0-201-18075-8. |
| **3.** | Fundamentals of Digital Image Processing , Anil K. Jain, 2001, Pearson Education, PHI, ISBN: 0071412379 |
| **4.** | Digital Image Processing and Analysis , Chanda and D. Dutta Majumdar, 2nd Edition, 2003, PHI, ISBN: 9788120343252 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **3** | **-** | **-** | **-** | **2** | **2** | **-** | **3** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **2** | **1** | **-** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **LOW POWER VLSI DESIGN (Theory)** | | |
| **Course Code:** 16EC6C4 | | **CIE Marks:** 100 |
| **Credits: L: T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Explain the need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. |
| **2** | Analyze the impact of Device Technology such as Transistor sizing & gate oxide thickness and Device innovation on Low Power. |
| **3** | Evaluate various probabilistic based power analysis techniques at various levels of abstraction. |
| **4** | Compare the trade-off between accuracy and resources for both simulations based and probability-based power analysis. |
| **5** | Apply various logic level techniques to optimize the power dissipation of the design reducing the switching activities in the design |
| **6** | Design and analyze digital circuits like combinational, sequential circuits using low power concepts. |

| **UNIT-I** | |
|---|---|
| **Introduction**<br>Need for Low Power VLSI Design, Sources of power dissipation, Physics of Power Dissipation in CMOS devices, MIS structure, long channel effect, sub-micron MOSFET, Gate induced drain leakage, Power dissipation in CMOS circuits: Short Circuit dissipation, Dynamic dissipation, load capacitance Charging and Discharging, Static Power: Leakage Currents, Static Currents, Emerging low power approaches and limits. | **08 Hrs** |
| **UNIT-II** | |
| **Power Estimation** -Signal Modeling and probability calculation, Probabilistic techniques for signal activity estimation, statistical techniques, Estimation of glitching power, sensitivity analysis, power estimation using input vector compaction, power estimation at circuit level, information theory-based approach, estimation of maximum power. | **07 Hrs** |
| **UNIT-III** | |
| **Device and Technology Impact on Low Power Electronics** Introduction, Dynamic Dissipation in CMOS, Effects of $V_{DD}$ and $V_t$ on speed, Constraints on $V_t$ Reduction, Transistor and Gate Sizing, Transistor Sizing and Optimal Gate Oxide Thickness, Impact of Technology Scaling, Equivalent Pin Ordering, Network Restructuring and Reorganization, Technology and Device Innovations, Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-computational Logic | **07 Hrs** |
| **UNIT-IV** | |
| **Low Power Circuit Techniques**<br>Introduction, Power consumption in circuits, Circuit design styles, Analysis of adders, multipliers, Flip-Flops and Latches, Low Power Cell Library.<br>Low power SRAM architectures: SRAM organization, MOS SRAM cells-4T and 6T, Banked organization of SRAMs, Reducing voltage swings on bit-lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits. | **07 Hrs** |
| **UNIT-V** | |
| **Synthesis for Low Power**<br>Behavioral level transforms, logic level optimizations, circuit level transforms, CMOS gates, Power Reduction in Clock Networks:power dissipation in clock distribution, single driver Vs distributed buffers, buffer and device sizing, zero sew Vs tolerable skew, CMOS Floating Nodes, Low Power Bus, Delay Balancing, Energy recovery CMOS and Adiabatic computation. | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Acquire the knowledge with regard to the physical principles, analysis and the characteristics of the low power designs. |
| CO2: | Identify, formulate, and solve engineering problems in the area of low power VLSI designs. |
| CO3: | Use the techniques and skills in system designing through modern engineering tools such as logic works SPICE and description languages such as VHDL and Verilog. |
| CO4: | Design a digital system, components or process to meet desired needs of low power within realistic constraints. |

| Reference Books | |
|---|---|
| **1.** | Low-Power CMOS VLSI Circuit Design, Kaushik Roy and Sharat Prasad, 2009, John Wiley India press, ISBN: 978-81-265-2023-7, |
| **2.** | Practical Low Power Digital VLSI Design, Gary K. Yeap, 2009, Kluwer Academic Publishers, ISBN: 978-1-4613-77778-8. |
| **3.** | Low Power Design Methodologies, Jan M. Rabaey and MassoudPedram, 5th reprint, Kluwer Academic Publishers, , ISBN: 978-1-4613-5975-3, 2002. |
| **4.** | Low Power CMOS design , Anantha Chandrakasan and Robert W. Brodersen, 1998, Wiley-IEEE press, ISBN: 0-7803-3429-9. |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **1** | **2** | **2** | **1** | **1** | **1** | **-** | **-** | **1** | **1** | **-** | **3** |
| **CO2** | **2** | **2** | **2** | **1** | **1** | **1** | **-** | **-** | **1** | **1** | **-** | **3** |
| **CO3** | **2** | **2** | **2** | **1** | **3** | **2** | **-** | **-** | **2** | **1** | **-** | **3** |
| **CO4** | **2** | **2** | **2** | **1** | **3** | **2** | **-** | **-** | **2** | **1** | **-** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **DATASTRUCTURE USING C++ (Theory)** | | |
| **Course Code:** 16EC6C5 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Analyze the need for data structuring techniques. |
| **2** | Implement standard data structures like stack, queue, list and tree. |
| **3** | Demonstrate the use of standard data structures using relevant applications. |
| **4** | Write appropriate data structures while building applications. |

| **UNIT-I** | |
|---|---|
| **Data Representation**:Overview of C++, Introduction to data representation, Linear Lists, Formula – Based Representation, Linked Representation, Indirect Addressing-Representation<br>**+Arrays and Matrices:** Arrays- The abstract data type, Indexing a C++ array, row and column major mapping, class Array1D, class Array2D, Matrices -definition and operations. Special Matrices-Definition and application, Diagonal Matrices, Tridiagonal Matrices, Triangular Matrices, Symmetric matrices, Sparse Matrices. | **07 Hrs** |
| **UNIT-II** | |
| **Stacks**: The Abstract Data Types, Derived Classes and Inheritance, Formula-based Representation, Linked Representation, Applications- Parenthesis matching, Towers of Hanoi. **Queues:** The Abstract Data Types, Derived Classes and Inheritance, Formula-based representation, Linked Representation, Applications- Rearranging railroad cars, Wire routing. | **07 Hrs** |
| **UNIT-III** | |
| **Skip List and Hashing:** Dictionaries, Linear List Representation- The ideal case, insertion and deletion, Assigning levels, class skipnode, the class skiplist, Skip list representation, Hash table representation-ideal hashing, hashing with linear open addressing, hash tables with chains.<br>**Binary and other Trees:** Trees, Binary Trees, Properties and Representation of Binary Trees-Formula – Based Representation, Linked Representation, Common Binary Tree Operations, Binary Tree Traversal The ADT Binary Tree, ADT and class Extensions | **08 Hrs** |
| **UNIT-IV** | |
| **Priority Queues:** Linear Lists, Heaps-Definitions, Insertion and Deletions from MaxHeap, MaxHeap Initialization, the class max Heap. Left list Trees-Height and Weight biased Min and Max lefist trees, Insertion and Deletion from a Max HBLT, Melding two max HBLTs, Initialization, the class Max HBLT | **07 Hrs** |
| **UNIT-V** | |
| **Graphs**: Definitions, Properties, Representation of Graphs, Representation of Networks, Class definitions, Graph Search methods, applications of Graphs. | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Acquire the knowledge of importance of data structures in computer programs. |
| CO2: | Represent and solve data analytics problems using graph algorithms. |
| CO3: | Implement classic data structures: array lists, linked lists, stacks, queues, heaps, binary trees, hash tables. |
| CO4: | Evaluate the performance of applications built using different data structures. |

| Reference Books | |
|---|---|
| **1.** | Data Structures, Algorithms and Applications in C++, Sartaj Sahni, 2000, McGraw Hill, ISBN: 10: 007236226X. |
| **2.** | C++:The Complete Reference , Herbert Schildt, 4th Edition, 2007, McGraw-Hill, , ISBN: 0-07-213485-2 |
| **3.** | Data Structures Using C++, D.S. Malik, 2nd Edition, 2009, Cengage Learning, |
| **4.** | Mastering C++, K.R Venugopal, Rajkumar, and T Ravishankar, 4th Edition, 2008, Tata McGraw-Hill Pubications. |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** |
| **CO2** | **3** | **3** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **2** | **-** | **1** |
| **CO3** | **3** | **3** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **2** | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **1** | **-** | **-** | **-** | **2** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **SYSTEM PROGRAMMING & SOFTWARE (Theory)** | | |
| **Course Code:** 16EC6C6 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Explain the need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. |
| **2** | Analyze the impact of Device Technology such as Transistor sizing & gate oxide thickness and Device innovation on Low Power. |
| **3** | Evaluate various probabilistic based power analysis techniques at various levels of abstraction. |
| **4** | Compare the trade-off between accuracy and resources for both simulation based and probability based power analysis. |
| **5** | Apply various logic level techniques to optimize the power dissipation of the design reducing the switching activities in the design |
| **6** | Design and analyze digital circuits like combinational, sequential circuits using low power concepts. |

| **UNIT-I** | |
|---|---|
| **Assemblers:** Introduction, Basic Assembler functions, algorithms and data structures; Machine-dependent assembler features, Machine-independent assembler features, Assembler design options: One- pass and Multi-pass assemblers, Case study: MASM assembler, SPARC assembler. | **08 Hrs** |
| **UNIT-II** | |
| **Loaders and Linkers:** Basic Loader functions: Absolute loader, Bootstrap loader, Machine-dependent loader features: re-location, program linking, Algorithm and Data structures of a linking loader, Machine-independent loader features, loader design options, linkage editors, dynamic linking, bootstrap loader, Case study: MS-DOS linker, SunOS linkers. | **07 Hrs** |
| **UNIT-III** | |
| **Macro-processors:** Basic Macro-processor functions: macro definition and expansion, Algorithm and Data structures of macro-processor, Machine-dependent macro-processor features: concatenation of macro-processor parameter, generation of unique labels, conditional macro expansion, keyword macro parameters, macro-processor design options, recursive macro expansion, general purpose macro processors, Case study: MASM macro processor, ELENA macro processor, ANSI Macro language. | **07 Hrs** |
| **UNIT-IV** | |
| **Compilers:** Basic compiler functions, Machine-dependent compiler features: intermediate form of the program, machine dependent code optimization, Machine-independent compiler features: structured variables, machine independent code optimization, storage allocation, block structured languages, Compiler design options: Interpreters, P-code compilers, Compiler-compilers, Case study: SunOS C compiler, Java compiler. | **07 Hrs** |
| **UNIT-V** | |
| **Operating Systems:** Basic operating system functions, Machine-dependent operating system features: interrupt processing, process scheduling, IO supervision, Real memory management, virtual memory management, Machine-independent operating system features: File processing, Job scheduling, Resource allocation, protection, Operating system design options: Hierarchical structure, Multiprocessor OS, Distributed OS, Object oriented OS, Case | **07 Hrs** |

| | |
|---|---|
| study: MS-DOS, SunOS and Windows | |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Acquire the knowledge with regard to the physical principles, analysis and the characteristics of the low power designs. |
| CO2: | Identify, formulate, and solve engineering problems in the area of low power VLSI designs. |
| CO3: | Use the techniques and skills in system designing through modern engineering tools such as logic works SPICE and description languages such as VHDL and Verilog. |
| CO4: | Design a digital system, components or process to meet desired needs of low power within realistic constraints. |

| Reference Books | |
|---|---|
| **1.** | System Software-An Introduction to System Programming, Leland L. Beck, 3rd Edition, 2009, Pearon Education, ISBN: 978-81-317-2700-3 |
| **2.** | System Programming, John J. Donovan, 2009, Tata McGraw Hill Edition, ISBN-13: 978-0-07-460482-3 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **2** | **1** | **2** | **1** | **1** | **1** | **-** | **-** | **1** | **1** | **-** | **3** |
| **CO2** | **2** | **1** | **2** | **1** | **1** | **1** | **-** | **-** | **1** | **1** | **-** | **3** |
| **CO3** | **2** | **1** | **2** | **1** | **1** | **1** | **-** | **-** | **1** | **1** | **-** | **3** |
| **CO4** | **2** | **1** | **2** | **1** | **1** | **1** | **-** | **-** | **1** | **1** | **-** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **FLEXIBLE ELECTRONICS (Theory)** | | |
| **Course Code:** 16EC6C7 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Realize the importance and advantages of Large Area and Flexible Electronics. |
| **2** | Understand the processes and equipments used for Large Area and Flexible Electronics. |
| **3** | Familiarization with the materials, substrates and interfaces in Large Area and Flexible Electronics. |
| **4** | Selection of materials and formulation of processes for various possible applications of Large Area and Flexible Electronics. |

| **UNIT-I** | |
|---|---|
| **Introduction to Flexible Electronics and their Materials Systems:** Background and history, trends, emerging technologies, general applications.<br>**Introduction to Semiconductors & Circuit Elements:** Carrier transport, doping, band structure, thin-film electronic devices. Thin-film Deposition and Processing Methods for Flexible Devices -CVD, PECVD, PVD, etching, photolithography, low-temperature process integration. | **08 Hrs** |
| **UNIT-II** | |
| **Materials for Flexible and Printed Electronics: Nanowire** and nanoparticle synthesis, transition metal oxides, amorphous thin films, polymeric semiconductors, structure and property relationships, paper-based electronics, textile substrates, barrier materials. | **07 Hrs** |
| **UNIT-III** | |
| **Thin Film Transistors 1: device structure and performance:** I-V characteristics, gradual channel approximation, electrical stability, lifetime extraction, characterization methods for rigid and flexible devices. Metal Oxide TFT's, Carbon Nanotube TFT's | **07 Hrs** |
| **UNIT-IV** | |
| **Solution-based Patterning Processes:** Ink-jet printing, gravure, imprint lithography, spray pyrolysis, surface energy effects, multilayer patterning, design rule considerations. Substrates for Flexible electronics | **07 Hrs** |
| **UNIT-V** | |
| **Contacts and Interfaces to Organic and Inorganic Electronic Devices** Schottky contacts, defects, carrier recombination, effect of applied mechanical strain.**Flexible Electronics Applications :**Displays, sensor arrays, memory devices, MEMS, lab-on-a-chip, and photovoltaics | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Define the requirements of materials, working and fabrication for flexible electronics devices |
| CO2: | Categorize fabrication/Patterning/Printing techniques various flexible electronics application |
| CO3 | Analyze thin film devices & circuits for flexible electronics applications |
| CO4: | Engage in selfstudy for modeling & simulation of various materials & devices used in flexible electronics |

| **Reference Books** | |
|---|---|
| **1.** | Flexible Electronics – Materials and applications, William S Wong, Salleo, Alberto, 2009, Springer, ISBN 978-0-387-74363-9 |
| **2.** | Large Area and Flexible Electronics, Mario Carioni, Yong-Yong Noh, 2015, Wiley ISBN: 978-3-527-67999-7 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **-** | **-** | **-** | **2** |
| **CO2** | **3** | **2** | **1** | **-** | **-** | **1** | **2** | **-** | **-** | **-** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **1** | **1** | **2** | **-** | **-** | **-** | **-** | **2** |
| **CO4** | **3** | **3** | **2** | **2** | **3** | **1** | **2** | **-** | **3** | **2** | **1** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **OPTICAL FIBER COMMUNICATION & NETWORKS (Theory)** | | |
| **Course Code:** 16EC6D1 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:**36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Analyze Optical spectral band and incorporate the standards for optical fiber communication |
| **2** | Analyze Single-mode Fibers, Graded-index Fiber Structure, Mechanical Properties of Fibers and Fiber Optic Cables |
| **3** | Demonstrate light sources using Light-Emitting Diodes (LEDs), Laser Diodes |
| **4** | Develop optimum Source-to-Fiber Power Launching & Lensing Schemes for Coupling Improvement. |

| **UNIT-I** | |
|---|---|
| **Introduction**<br>Ray theory transmission, Total internal reflection, Acceptance angle , Numerical aperture, Skew rays, Electromagnetic mode theory of optical propagation, EM waves, modes in planar guide, phase and group velocity, cylindrical fibers, SM fibers. | **08 Hrs** |
| **UNIT-II** | |
| **Transmission Characteristics of Optical Fibers**<br>Attenuation, Material absorption losses in silica glass fibers,Linear and Nonlinear Scattering losses,Fiber Bend losses, Midband and far band, infra-red transmission, Intra and inter Modal Dispersion, over all Fiber Dispersion, Polarization, nonlinear Phenomena. Optical fiber connectors**,** Fiber alignment and Joint Losses, Fiber Splices, Fiber connectors, Expanded Beam Connectors, Fiber Couplers. | **07 Hrs** |
| **UNIT-III** | |
| **Sources and Detectors**<br>Optical sources: Light Emitting Diodes, LED structures, surface and edge emitters, mono and hetero structures, internal, quantum efficiency, injection laser diode structures, comparison of LED and ILD<br>Optical Detectors: PIN Photo detectors, Avalanche photo diodes, construction, characteristics and properties, Comparison of performance, Photo detector noise, Noise sources, Signal to Noise ratio, Detector response time. | **07 Hrs** |
| **UNIT-IV** | |
| **Fiber Optic Receiver and Measurements**<br>Fundamental receiver operation, Pre-amplifiers, Error sources, Receiver Configuration, Probability of Error, Quantum limit.<br>Fiber Attenuation measurements- Dispersion measurements, Fiber Refractive index Profile measurements, Fiber cut- off Wave length Measurements, Fiber Numerical Aperture Measurements, Fiber diameter measurements. | **07 Hrs** |
| **UNIT-V** | |
| **Optical Networks**<br>Basic Networks, SONET / SDH, Broadcast and select WDM Networks, Wavelength Routed Networks, Nonlinear effects on Network performance<br>Performance of WDM + EDFA system, Solitons, Isolators, Circulators, Optical CDMA, Ultra High Capacity Networks.<br>**Self-Study:**<br>Seminars, Projects, Paper publication, etc. on emerging technologies pertaining to the subject 4 Hrs/Week: 1 Credit | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Select the proper Optical spectral band and incorporate the standards for optical fiber communication. |
| CO2: | Analyze various WDM Concepts and Apply different Optical Network concepts and topologies and design WDM Networks. |
| CO3: | Analyze the Optical Fiber Modes and Configurations of the Single-mode Fibers, Graded-index Fiber Structure, Mechanical Properties of Fibers and Fiber Optic Cables. |
| CO4: | Design the light sources using Light-Emitting Diodes (LEDs), Laser Diodes and evaluate Light Source Linearity, and analyze the Reliability considerations. |

| Reference Books | |
|---|---|
| **1.** | Optical Fiber Communication, Gerd Keiser, 2008, Tata McGraw Hill Publication, |
| **2.** | Optical Fiber Communications, John M. Senior, "", 3rd Edition, 2007, Pearson Education, ISBN |
| **3.** | Optical Networks: A Practical Perspective, Rajiv Ramaswami, Kumar N. Sivarajan and Galen H. Sasaki, 3rd Edition, 2010, The Morgan Kaufmann Series in Networking. |
| **4.** | Fiber Optics and Optoelectronics, R.P. Khare, 2007, Oxford University Press |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **2** | **3** | **1** | **2** | **-** | **3** | **-** | **-** | **2** | **3** | **1** | **2** |
| **CO2** | **1** | **2** | **3** | **3** | **-** | **2** | **-** | **-** | **3** | **2** | **1** | **3** |
| **CO3** | **3** | **1** | **2** | **2** | **-** | **1** | **-** | **-** | **3** | **2** | **3** | **1** |
| **CO4** | **2** | **3** | **1** | **3** | **-** | **2** | **-** | **-** | **2** | **2** | **1** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **ARM CORTEX PROCESSORS (Theory)** | | |
| **Course Code:** 16EC6D2 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understand the architecture of different processors suitable for embedded system. |
| **2** | To gain knowledge on ARM cortex-M series CPU architecture, instruction set, exceptions, memory & special OS features. |
| **3** | Identify the design issues ARM based embedded system with the basic knowledge of firmware, embedded OS & ARM architectures. |
| **4** | Analyse the execution of instructions/program knowing the basic principles of ARM architecture and assembly language & the special features of Cortex-M3/M4 to realize signal processing applications. |

| **UNIT-I** | |
|---|---|
| **Introduction:** Embedded Processor Selection, PowerPC, ARM Cortex, SoC, Digital Signal Processors **ARM Cortex-2 Series Overview:** Cortex-M Processor Family, Product Portfolio, Advantages, Applications, Cortex Microcontroller Software Interface Standard (CMSIS), General Information, Features | **08 Hrs** |
| **UNIT-II** | |
| **Architecture of ARM Cortex-2 Processor:** Programmer's Model, Application Program Status Register (APSR), Memory System, Exceptions & Interrupts, System Control Block, Debug, Reset & Reset Sequence **Instruction Set-I:** Assembly Language Syntax, Suffixes for Assembly Instructions, Unified Assembly Language, Assembly Instructions | **07 Hrs** |
| **UNIT-III** | |
| **Instruction Set-II:** Cortex-M4/M7 Specific Instructions, Barrel Shifter **Memory System:** Memory Map, Connecting Cortex-M3/M4 with Memory & Peripherals, Endianness, Data Alignment & Unaligned Data Access Support, Bit Band Operations, Memory Access Attributes, Exclusive Access, Memory Barriers, Memory System in a MCU. | **07 Hrs** |
| **UNIT-IV** | |
| **Exceptions & Interrupts:** Overview of Exceptions and Interrupts, Exception Types, Interrupt Management, Vector Table & Vector Table Relocation, Interrupts Inputs & Pending Behaviors, Exceptions Sequence, Overview, Details of NVIC Registers for Interrupt Control, SCB Registers for Exceptions & Interrupt Control, Special Registers for Exceptions Masking, Procedures in Setting up Interrupts, Software Interrupts. Exception Handler in C, Stack Frames, Exception Sequences. | **07Hrs** |
| **UNIT-V** | |
| **Low Power and System Control Features:** Low Power Designs, Low Power Features, Using WFI & WFE Instructions in for Programming, Developing Low Power Applications, The SysTick Timer, Self-Reset, CPU ID Base Register, Configuration Control Register, Auxiliary Control Registers, Co-Processor Access Control Register.**OS Support Features :** Shadowed Stack Pointer, SVC Exception, PendSV Exception, Context Switching in Action, Exclusive Accesses | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Understand the architecture, instruction set, memory organization and addressing modes of the embedded processors. |
| CO2: | Realize real time signal processing applications & primitive OS operations on different ARM architectures by making use of software libraries. |
| CO3: | Perform market survey of available embedded processors & arrive at the required processor for solving the given problem statement. |

| | |
|---|---|
| CO4: | Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments. |

| **Reference Books** | |
|---|---|
| **1.** | The Definitive Guide to the ARM Cortex-M3& M4 Processors, Joseph Yiu, 3rd Edition, 2014 Newnes (Elsevier), ISBN:978-93-5107-175-4 |
| **2.** | ARM System Developers Guide, Andrew N Sloss, Dominic Symes, Chris Wright, 2008, Elsevier, Morgan Kaufman publishers, ISBN-13:9788181476463 |
| **3.** | ARM System on Chip Architecture , Steve Furber, 2nd Edition, 2000, Pearson Education Limited, ISBN-13:9780201675191 |
| **4.** | Technical reference manual for ARM processor cores, including Cortex M3, M4, M7 processor families. |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | | **-** | **-** |
| **CO2** | **3** | **2** | **2** | **3** | **-** | **2** | **-** | **2** | **2** | | **-** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **2** | **-** | **2** | **2** | | **-** | **1** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **3** | **2** | **3** | **3** | **3** | **3** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **ADAPTIVE SIGNAL PROCESSING (Theory)** | | |
| **Course Code:** 16EC6D3 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Identify applications in which it would be possible to use the different adaptive filtering approaches. |
| **2** | Design, implement and apply LMS filter to given application. |
| **3** | Design and apply optimal minimum mean square estimators and in particular linear estimators. To understand and compute their expected performance and verify it. |
| **4** | Design, implement and apply filters (FIR, non-causal, causal) and evaluate their performance. |

| **UNIT-I** | |
|---|---|
| **Adaptive Systems:** Definition and characteristics, Areas of application, General properties, Open-and closed-loop adaptation, Applications of closed-loop adaptation, Example of an adaptive system. **The Adaptive Linear Combiner:** General description, Input signal and weight vectors, Desired response and error, the performance function, gradient and minimum mean-square error, Example of a performance surface, Alternative expression of the gradient, Decorrelation of error and input components. | **08 Hrs** |
| **UNIT-II** | |
| **Quadratic Performance Surface:** Normal of the input correlation matrix, Eigen values and Eigen vectors of the input correlation matrix, an example with two weights, Significance of Eigenvectors**,** Geometrical significance of eigenvectors and Eigen values. **Searching the Performance Surface:** Methods of searching the performance surface, Basic ideas of gradient search methods, a simple gradient search algorithm and its solution, Stability and rate of convergence, the learning curve. Newton's method in multidimensional space, Steepest descent method, Comparison of learning curves. | **07 Hrs** |
| **UNIT-III** | |
| **Adaptive Modeling and System Identification:** General description, Adaptive modeling of multipath communication channel, adaptive modeling in geophysical exploration, Adaptive modeling in FIR digital filter synthesis.**Gradient Estimation and Its Effects on Adaptation:** Gradient component estimation by derivative measurement. The performance penalty, Derivative measurement and performance penalties with multiple weights, variance of the gradient estimate, effects on the weight-over solution, excess mean-square error and time constants, misadjustment, comparative performance of Newton's and steepest-descent methods, Total misadjustment and other practical considerations. | **07 Hrs** |
| **UNIT-IV** | |
| **The LMS Algorithm:** Derivation of the LMS algorithm, convergence of the weight vector, an example of convergence, learning curve, noise in the weight-vector solution, misadjustment, performance. **Adaptive Interference Canceling:** The concept of adaptive noise canceling, stationary noise-canceling solutions, effects of signal components in the reference input, The adaptive interference canceller as a notch filter, The adaptive interface canceller as a high-pass filter. | **07 Hrs** |
| **UNIT-V** | |
| **Digital Models for Speech Signals:** Process of Speech Production, Lossless tube models, Digital models for Speech signals.**Time Domain Models for Speech Processing:** Time dependent of speech, Short time average zero crossing rate, Speech vs. silence discrimination using energy and zero crossing, pitch period estimation using parallel processing approach, short time autocorrelation function, Short time average magnitude difference function, Pitch period estimation using autocorrelation function | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Understand the concepts of linear algebra & linear adaptive systems. |
| CO2: | Applying the concepts of adaptive algorithms to various engineering problems. |
| CO3: | Analyze the effect various parameters in developing an adaptive systems. |
| CO4: | Design and implement simple adaptive systems for any computational applications. |

| Reference Books | |
|---|---|
| **1.** | Adaptive Signal Processing, Bernard Widrow and Samuel d. Stearns, 2001, Pearson Education Asia, ISBN:9788131705322 |
| **2.** | Adaptive Filter Theory, Simon Haykin, 4th Edition, 2002, Pearson Education Asia, ISBN 0-13-090126-1 |
| **3.** | Theory and Design of Adaptive Filters, John R. Treichler C. Richard Johnson, Jr. and Michael G. Larimore, 2002, Pearson Education, , ISBN-10: 0130402656 |
| **4.** | Digital Processing of Speech Signals , L R Rabiner and R W Schafer, 2004, Pearson Education, ISBN 978-1848822535 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO2** | **2** | **2** | **2** | **1** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO3** | **2** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO4** | **2** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **1** | **-** | **1** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **SYSTEM VERILOG (Theory)** | | |
| **Course Code:** 16EC6D4 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |
| **Course Learning Objectives: The students will be able to** | | |
| **1** | Build a System Verilog verification environment | |
| **2** | Define test bench components using object-oriented programming | |
| **3** | Develop functional coverage to measure completeness of test | |
| **4** | Develop a stimulus generator to create constrained random test stimulus | |

| **UNIT-I** | |
|---|---|
| **System Verilog data types, Operators, Loops, Functions**<br>Data types, Built-In Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing a Storage Type, Creating New Types with typedef, Creating User-Defined Structures, Type conversion, Enumerated Types, Constants, Strings, Procedural Statements, Tasks, Functions, and Void Functions, Routine Arguments, Returning from a Routine. | **08 Hrs** |
| **UNIT-II** | |
| **Class and Randomization**<br>System verilog class basics, class declaration, class members and methods, class handles, class object construction, super and this keywords, object handles, user defined constructors, class extension and inheritance, chaining new() constructors, overriding class methods, extending class methods, local and protected keywords, constrained random variables, directed vs random testing, rand and randc class data types, randomize-randomizing class variables, randcase, built-in-randomization methods, randsequence and examples. | **07 Hrs** |
| **UNIT-III** | |
| **Interfaces, Program block and Clocking**<br>Interface overview, generic interfaces, interfaces Vs records, how interfaces work, requirements of good interface, interface constructs, interface modports, Fundamental test bench construction, program blocks, program block interaction with modules, final blocks, Test bench stimulus/Verification vector timing strategies, Clocking blocks, clocking skews, clocking block scheduling, fork-join processes. | **07 Hrs** |
| **UNIT-IV** | |
| **Constrained Random variables, Coverage, Methods and interfaces**<br>Randomization constraints, simple and multi-statement constraints, constraint distribution and set membership, constraint distribution operators, external constraints, cover groups, cover points, cover point bins and labels, cross coverage, cover group options, coverage capabilities. Virtual class, why to use virtual class, virtual class methods and restrictions, polymorphism using virtual methods, pure virtual methods, pure constraints, passing type parameters, virtual interfaces. | **07 Hrs** |
| **UNIT-V** | |
| **System Verilog Assertions**<br>Assertion definition, assertion benefits, system Verilog assertion types, immediate assertions, concurrent assertions, assert and cover properties and labels, overlapping and non-overlapping implications, edge testing functions, sequences, Vacuous success, property styles, System Verilog assertion system functions, Assertion severity tasks, assertion and coverage examples of an FSM design. | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Explain the behavior of different digital blocks by writing HDL code. |
| CO2: | Apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification. |
| CO3: | Integrate various digital blocks and implement a complete digital system. |
| CO4: | Design different architectures of various digital blocks and optimize the area, speed and power. |

| Reference Books | |
|---|---|
| **1.** | System Verilog for Verification: A guide to learning the Test bench Language Features, Christian B Spear, 3rd Edition, Springer Publications. |
| **2.** | System Verilog Assertions, Vijaya Raghavan, 2005, Springer Publications, ISBN 978-0-387-26173-7 |
| **3.** | System Verilog for Design , Stuart Sutherland, Smon Davidmann Peter Flake, 2nd Edition, Springer Publications. |
| **4.** | System Verilog Primer , J Bhaskar, 2010, Star Galaxy Publishing, ISBN 13: 9780965039116 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **3** | **-** | **1** | **-** | **1** | **-** | **-** | **2** |
| **CO2** | **3** | **2** | **2** | **1** | **3** | **1** | **2** | **-** | **2** | **-** | **-** | **2** |
| **CO3** | **3** | **3** | **2** | **2** | **3** | **-** | **1** | **1** | **1** | **-** | **-** | **2** |
| **CO4** | **3** | **3** | **3** | **3** | **3** | **1** | **3** | **-** | **1** | **-** | **-** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **Algorithm for VLSI Design Automation** | | |
| **Course Code:** 16EC6D5 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |
| **Course Learning Objectives: The students will be able to** | | |
| **1** | Analyze the concept of digital systems, how they can be optimized for area, power and cost, why it is advantageous to use physical design tools. | |
| **2** | Implement the concept of the physical design cycle and develop algorithms (tools)for each design cycle step. | |
| **3** | Optimize the digital system at architectural level. | |
| **4** | Synthesize a given system starting with problem requirements, identifying and designing the building blocks, and then integrating blocks designed earlier | |

| **UNIT-I** | |
|---|---|
| **Architectural Level Synthesis:** Introduction, Circuit specifications for architectural synthesis, the fundamentals of architectural synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization **Scheduling Algorithms:** Introduction, A model for scheduling problems, Scheduling without and with resource constraints, Scheduling algorithms for extended sequencing models, Scheduling pipelined circuits, Resource sharing and binding. | **08 Hrs** |
| **UNIT-II** | |
| **Data Structure and Basic Algorithms:** Basic Terminology, Graph Search Algorithms, Computational Geometry Algorithms, Basic Data structures. **Partitioning:** Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms | **07 Hrs** |
| **UNIT-III** | |
| **Floor Planning and Pin Assignment:** Problem formulation, classification, Constraint based, Integer programming based, rectangular Dualization, simulated evolution floor planning algorithms. **Placement:** Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms | **07 Hrs** |
| **UNIT-IV** | |
| **Global Routing: Problem** formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path-based Algorithms, Steiner tree-based Algorithms Detailed **Routing:** Problem formulation, Classification single Layer routing, General river routing, Single row routing | **07Hrs** |
| **UNIT-V** | |
| **Channel, Clock and Power Routing:** Two-layer channel routing Algorithms, Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, **Clock Tree Routing:** H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms. | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Analyze each stage of VLSI design flow to develop a CAD tool for physical design. |
| CO2: | Apply design knowledge to develop algorithms for VLSI design automation. |
| CO3: | Evaluate the algorithms for optimizing VLSI design with respect to speed, power and area. |
| CO4: | Create an optimized VLSI IC design technique using various algorithms. |

| Reference Books | |
|---|---|
| **1.** | Synthesis and Optimization of Digital Circuit, 1994, Giovanni De Micheli, McGraw- Hill, ISBN: 10- 0070163332 |
| **2.** | Algorithms for VLSI Physical Design Automation, N.A. Sherwani, 2002, Kluwar Academic Publishers, ISBN: 0-7923-8393-1 |
| **3.** | An Introduction to VLSI Physical Design, M Sarraf Zadeh, C K Wong, 1996, McGraw Hill, ISBN:0070571945 |
| **4.** | Algorithms for VLSI Design Automation , S.H. Gerez, 1998, John Wiley & Sons, ISBN: 978-0-471-98489-4 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **-** | **1** | **3** | **2** | **3** | **-** | **-** | **-** | **1** | **1** | **2** | **3** |
| **CO2** | **3** | **2** | **3** | **1** | **3** | **-** | **1** | **1** | **2** | **2** | **3** | **3** |
| **CO3** | **3** | **2** | **3** | **3** | **3** | **1** | **-** | **-** | **1** | **1** | **3** | **3** |
| **CO4** | **3** | **3** | **3** | **1** | **3** | **-** | **-** | **1** | **2** | **1** | **1** | **3** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **Database Management Systems** | | |
| **Course Code:** 16EC6D6 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |
| **Course Learning Objectives: The students will be able to** | | |
| **1** | Understand the differences between logical and physical database design. | |
| **2** | Understand the context, phases and techniques for designing and building database information systems in business. | |
| **3** | Analyse database requirements and determine the entities involved in the system and their relationship to one another. | |
| **4** | Design and build a simple database system and demonstrate competence with the fundamental tasks involved with modelling, designing, and implementing a DBMS. | |

| **UNIT-I** | |
|---|---|
| **Introduction:** An example, Characteristics of Database approach, Actors on the screen, Workers behind the scene, Advantages of using DBMS approach, A brief history of database applications. **Data models:** schemas and instances, Three-schema architecture and data independence, Database languages and interfaces, The database system environment, Centralized and client-server architectures, Classification of Database Management systems. **Entity-Relationship Model:** Using High-Level Conceptual Data Models for Database Design, An Example Database Application, Entity Types, Entity Sets, Attributes and Keys, Relationship types, Relationship Sets, Roles and Structural Constraints, Weak Entity Types, Refining the ER Design, ER Diagrams, Naming Conventions and Design Issues, Relationship types of degree higher than two. | **08 Hrs** |
| **UNIT-II** | |
| **Relational Model and Relational Algebra:** Relational Model Concepts, Relational Model Constraints and Relational Database Schemas, Update Operations, Transactions and dealing with constraint violations, Unary Relational Operations: SELECT and PROJECT, Relational Algebra Operations from Set Theory.<br>**SQL basics:** SQL Data Definition and Data Types, Specifying constraints in SQL, Basic retrieval queries in SQL. Insert, Delete and Update statements in SQL. | **07 Hrs** |
| **UNIT-III** | |
| **SQL programming:** complex SQL queries. Specifying constraints as Assertion and actions as Trigger, Views (Virtual Tables) in SQL, schema change statements in SQL.<br>**Introduction to Python:** SQL Database connection using python, Creating and searching tables, Reading and storing configurations information on database, Programming using database connections | **07 Hrs** |
| **UNIT-IV** | |
| **Database Design –1:** Informal Design Guidelines for Relation Schemas, Functional Dependencies, Normal Forms Based on Primary Keys, General Definitions of Second and Third Normal Forms, Boyce-Codd Normal Form. **Database Design -2** Properties of Relational Decompositions, Algorithms for Relational Database Schema Design, Multivalued Dependencies and Fourth Normal Form, Join Dependencies and Fifth Normal Form, Inclusion Dependencies | **07 Hrs** |
| **UNIT-V** | |
| **Transaction Management** The ACID Properties, Transactions and Schedules, Concurrent Execution of Transactions, Lock- Based Concurrency Control, Performance of locking, Transaction support in SQL, Introduction to crash recovery, 2PL, Serializability and Recoverability, Lock Management, Introduction to ARIES, The log, Other recovery-related structures, The write-ahead log protocol, Check pointing, Recovering from a System Crash, Media Recovery, Other approaches and interaction with concurrency control. | **07 Hrs** |

| Course Outcomes: After completing the course, the students will be able to | |
|---|---|
| CO1: | Demonstrate the understanding of the fundamentals of Data Base management system, entity-relationship model, Relational Algebra, Database Design, Transaction Management. |
| CO2: | Use an SQL interface of a multi-user relational DBMS package to create, secure, populate, maintain, and query a database. |
| CO3: | Analyse an information storage problem and derive an information model expressed in the form of an entity relation diagram and other optional analysis forms, such as a data dictionary. |
| CO4: | Design a data model that satisfies relational theory and provides users with business Queries, business forms and business reports. |

| Reference Books | |
|---|---|
| **1.** | Fundamentals of Database Systems, Elmasri, Navathe, 5th Edition, 2007, Pearson Education, ISBN-13: 978-0-136-08620-8 |
| **2.** | Database Management Systems, Raghu Ramakrishnan, Johannes Gehrke, 3rd Edition, 2003, McGraw-Hill, ISBN-10: 007246563 |
| **3.** | Data base System Concepts, Silberschatz, Korth, Sudharshan, 6th Edition, 2010, Mc-GrawHill, ISBN-10: 0073523321/ISBN-13: 978-0073523323 |
| **4.** | An Introduction to Database Systems, C.J. Date, A. Kannan, S. Swamynatham, 8th Edition, 2006, Pearson Education, ISBN: 9788177585568. |

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**Semester End Evaluation (SEE); Theory (100 Marks)**

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| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **1** | **3** | **3** | **1** | **1** | **1** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO2** | **1** | **2** | **2** | **1** | **1** | **1** | **-** | **-** | **-** | **-** | **-** | **2** |
| **CO3** | **1** | **2** | **2** | **1** | **1** | **1** | **-** | **-** | **2** | **1** | **-** | **2** |
| **CO4** | **1** | **3** | **3** | **1** | **1** | **-** | **-** | **-** | **2** | **1** | **-** | **2** |

**Low-1 Medium-2 High-3**

| **Semester: VI** | | |
|---|---|---|
| **Internet of Things (IoT)** | | |
| **Course Code:** 16EC6D7 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:1 | | **SEE Marks:** 100 |
| **Hours:** 36L | | **SEE Duration:** 3Hrs |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Understands the mechanisms used in the design of IoT device. |
| **2** | Aware of the role and importance of the Internet of Things in the enterprise, economy and society. |
| **3** | Design the architecture and technologies needed to implement IoT devices. |
| **4** | Create software for devices equipped with sensors interacting with environment |

| **UNIT-I** | |
|---|---|
| **Introduction to IoT**, IoT Network Architecture and Design, Drivers Behind New Network Architectures, Comparing IoT Architectures, A Simplified IoT Architecture, IoT Data Management and Compute Stack | **07 Hrs** |
| **UNIT-II** | |
| **Engineering IoT Networks**: Smart Objects: The "Things" in IoT, Sensors, Actuators, and Smart Objects, Sensor Networks, Wireless Sensor Networks, Connecting Smart Objects, Communications Criteria, Range, Frequency Bands, Power Consumption, Constrained-Node Networks, Data Rate and Throughput, Latency and Determinism, Overhead and Payload | **07 Hrs** |
| **UNIT-III** | |
| **IoT Access Technologies:** IEEE 802.15.4, IEEE 802.15.4g and 802.15.4e, IEEE 1901.2a, IEEE 802.11ah, Physical Layer, MAC Layer, Topology, Security, LoRaWAN, | **07 Hrs** |
| **UNIT-IV** | |
| **IP as the IoT Network Layer,** The Need for Optimization, Optimizing IP for IoT, Profiles and Compliances, Application Protocols for IoT, IoT Application Transport Methods, SCADA, SCADA Transport over LLNs with MAP-T, IoT Application Layer Protocols | **07 Hrs** |
| **UNIT-V** | |
| **Programming IoT using C:** Introduction to Raspberry Pi, Pi vs. Microcontroller, Getting started with IDE, Introduction to GPIO, Inputs and interrupts, Memory mapped GPIO, Programming examples. | **08 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Demonstrate the working of IoT Networks, IoT Access Technologies |
| CO2: | Analyze the different IoT Access & Network Technologies and sensing elements |
| CO3: | Design the Communications & Payload for IoT applications |
| CO4: | Design the application using sensing elements though various networks & protocol |

| **Reference Books** | |
|---|---|
| **1.** | IoT Fundamentals: Networking Technologies, Protocols and Use Cases for the Internet of Things , Hanes David,Salgueiro Gonzalo, Grossetete Patrick ,Henry Jerome, 1st edition, 2017, Pearson Education, ISBN-13:978-9386873743 |
| **2.** | Raspberry Pi Iot in C , Harry Fairhead , 1st edition, 2016, I/O Press;, ISBN-13: 978-1871962468. |
| **3.** | Internet of Things: A Hands-On Approach, Arsheep Bahga, Vijay Madisetti, 1st edition , 2015, Orient Blackswan Private Limited - New Delhi,ISBN-13: 978-8173719547 |
| **4.** | Getting Started with Sensors, Kimmo Karvinen ,Tero Karvinen, 1st edition 2014, O′Reilly;, ISBN-13: 978-1449367084 |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Self-Study(S). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for Self-study is 20. The total marks of CIE are 100.

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level

| CO-PO Mapping | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **2** | **-** | **-** | **2** | **-** | **-** | **-** | **-** | **1** | **1** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **2** | **-** | **-** | **-** | **-** | **1** | **1** | **1** |
| **CO3** | **3** | **3** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** |
| **CO4** | **3** | **3** | **3** | **3** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** |

**Low-1 Medium-2 High-3**

| **Semester: V& VI** | | |
|---|---|---|
| **Professional Practice – III**<br>**Communication Skills and Professional Ethics** | | |
| **Course Code:** 16HS68 | | **CIE Marks:** 50 |
| **Credits: L:T:P:S:** 1:0:0:0 | | **SEE Marks:** -- |
| **Hours:** 36 | | **SEE Duration:** -- |

| **Course Learning Objectives: The students will be able to** | |
|---|---|
| **1** | Improve qualitative and quantitative problem-solving skills. |
| **2** | Apply critical and logical thinking process to specific problems. |
| **3** | Ability to verbally compare and contrast words and arrive at relationships between concepts, based on verbal reasoning. |
| **4** | Applying good mind maps that help in communicating ideas as well as in technical documentation. |

| **V Semester** **UNIT-I** | |
|---|---|
| **Aptitude Test Preparation**- Importance of Aptitude tests, Key Components, Quantitative **Aptitude** – Problem Solving, Data Sufficiency, Data Analysis - Number Systems, Math Vocabulary, fraction decimals, digit places etc.<br>**Reasoning and Logical Aptitude**, - Introduction to puzzle and games organizing information, parts of an argument, common flaws, arguments and assumptions. Analytical Reasoning, Critical Reasoning, | **06 Hrs** |
| **UNIT-II** | |
| **Verbal Analogies** - What are Analogies, How to Solve Verbal Analogies & developing Higher Vocabulary, Grammar, Comprehension and Application, Written Ability. Non-Verbal Reasoning, Brain Teasers. Creativity Aptitude.<br>**Group Discussion**- Theory &Evaluation: Understanding why and how is the group discussion conducted, The techniques of group discussion, Discuss the FAQs of group discussion, body language during GD. | **06 Hrs** |
| **UNIT-III-A** | |
| **Resume Writing-** Writing Resume, how to write effective resume, Understanding the basic essentials for a resume, Resume writing tips Guidelines for better presentation of facts. | **06 Hrs** |
| **VI Semester** **UNIT- III-B** | |
| **Technical Documentation** - Introduction to technical writing- Emphasis on language difference between general and technical writing, Contents in a technical document, Report design overview & format Headings, list & special notes, Writing processes, Translating technical information, Power revision techniques, Patterns & elements of sentences, Common grammar, usage & punctuation problems. | **06 Hrs** |
| **UNIT-IV** | |
| **Interview Skills** -a) Personal Interviews , b) Group Interviews , c) Mock Interviews - Questions asked & how to handle them, Body language in interview, Etiquette, Dress code in interview, Behavioral and technical interviews, Mock interviews - Mock interviews with different Panels. Practice on stress interviews, technical interviews, General HR interviews etc. | **06 Hrs** |
| **UNIT-V** | |
| **Interpersonal Relations** - Optimal Co-existence, Cultural Sensitivity, Gender sensitivity Adapting to the Corporate Culture- Capability & Maturity Model, Decision Making Analysis, Brain Storm. Adapting to the Corporate Culture. | **06 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| CO1: | Inculcate employability skill to suit the industry requirement. |
| CO2: | Analyze problems using quantitative and reasoning skills |
| CO3: | Exhibit verbal aptitude skills with appropriate comprehension and application. |
| CO4: | Focus on Personal Strengths and Competent to face interviews and answer the aptitude |

| Reference Books | |
|---|---|
| 1 | The 7 Habits of Highly Effective People, Stephen R Covey, 2004 Edition, Free Press, ISBN: 0743272455 |
| 2 | How to win friends and influence people, Dale Carnegie, “”,1st Edition, 2016, General Press, ISBN: 9789380914787 |
| 3 | Crucial Conversation: Tools for Talking When Stakes are High , Kerry Patterson, Joseph Grenny, Ron Mcmillan, “”, McGraw-Hill Publication, 2012 Edition, ISBN: 9780071772204 |
| 4 | Aptimithra: Best Aptitude Book ,Ethnus, 2014 Edition, Tata McGraw Hill, ISBN: 9781259058738 |

**Scheme of Continuous Internal Examination (CIE)**

Evaluation will be carried out in TWO Phases.

| Phase | Activity | Weightage |
|---|---|---|
| I | Test 1 is conducted in V Sem for 50 marks (15 Marks Quiz and 35 Marks Descriptive answers) after completion of Unit-1, Unit-2 and Unit -3.A for 18 hours of training sessions. | 50% |
| II | Test 2 is conducted in VI Sem for 50 marks ((15 Marks Quiz and 35 Marks Descriptive answers) after completion of Unit -3B, Unit - 4 and Unit-5 for 18 hours of training sessions. | 50% |
| | At the end of the VI sem Marks of Test 1 and Test 2 is consolidated for 50 marks and grading is done. The final CIE marks is scrutinized by the committee comprising of HSS-Chairman, Training Co-ordinator, respective department Staff Placement co-ordinator before submitting to CoE. | |

**Mapping of Course Outcomes (CO) to Program Outcomes (PO)**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | - | 1 | - | - | 3 | - | 3 | 3 | 3 | 3 |
| CO2 | 3 | 2 | 3 | - | - | - | - | - | 2 | 3 | 2 |
| CO3 | - | - | 1 | - | - | 2 | - | 2 | 2 | 3 | 3 |
| CO4 | - | - | 2 | - | - | 3 | 1 | 3 | 2 | 2 | 3 |

**Low-1 Medium-2 High-3**

| **Semester: VI (Global Elective-E)** | | |
|---|---|---|
| **Automotive Electronics** | | |
| **Course Code:** 16G6E05 | | **CIE Marks:** 100 |
| **Credits: L:T:P:S:** 3:0:0:0 | | **SEE Marks:** 100 |
| **Hours:**36L | | **SEE Duration:** 3Hrs |
| **Course Learning Objectives: The students will be able to** | | |
| **1** | Understand the application of principles of sensing technology in automotive field | |
| **2** | Apply control systems in the automotive domain | |
| **3** | Understand automotive specific communication protocols / techniques | |
| **4** | Analyze fault tolerant real time embedded systems | |

| **UNIT-I** | |
|---|---|
| **Power Train Engineering and Fundamentals of Automotive:** Fundamentals of Petrol, diesel and gas engines, electric motors and control systems. Basic Automotive System, System Components, Evolution of Electronics in Automotive. Alternators and charging, battery technology, Ignition systems. Working principles of various electronic components and accessories used in Automotive. Developments in existing engine forms and alternatives. Hybrid designs (solar power, electric/gasoline, LPG, CNG, fuel cells). Basic Transmission systems. | **08 Hrs** |
| **UNIT-II** | |
| **Sensor Technologies in Automotive:** In-vehicle sensors: Working principles, Characteristics, limitations and use within the automotive context of the following: Temperature sensing e g. coolant, air intake. Position sensing e.g. crankshaft, throttle plate. Pressure sensing e.g. manifold, exhaust differential, tyre. Distance sensing e.g. anti-Collision, Velocity sensing e.g. speedometer, anti-skid. Torque sensing e.g. automatic transmission. Vibration sensing e.g. Airbags. flow sensing and measurement e.g. fuel injection. Interfacing principles: Operation, topologies and limitations of all sensors covered in the above to in-vehicle processing or communications nodes. Use of Actuators: Types, working principle, Characteristics, limitations and use within the automotive context of each type. | **07 Hrs** |
| **UNIT-III** | |
| **Automotive Control Systems:** Control system approach in Automotive: Analog and Digital control methods, stability augmentation, control augmentation. Transmission control, System components and functions. Cruise control, traction control, actuator limiting, wind-up, gain scheduling, adaptive control. Special Control Schemes: Vehicle braking fundamentals, Antilock systems. Variable assist steering and steering control. Controls for Lighting. Wipers, Air conditioning /heating. Remote keyless Entry and Anti-theft System, Emission Course-system control. Control techniques used in hybrid system. Electronic Engine control: Motion equations, modeling of linear and non-linear systems, numerical methods, system responses Objective of Electronic Engine control. Spark Ignition and Compression Ignition Engines and their electronic controls. Engine management testing: Engine management system strategies and implementation. Simulation and implementation methods. Methods of improving engine performance and efficiency. Model Based Development (MBD) Technology. AUTOSAR: Objectives and Architecture. | **07 Hrs** |
| **UNIT-IV** | |
| **Automotive Communication Systems:** Communication interface with ECU's: Interfacing techniques and interfacing with infotainment gadgets. Relevance of internet protocols, such as TCP/IP for automotive applications. Wireless LANs standards, such as Bluetooth, IEEE802.11x. Communication protocols for automotive applications. Automotive Buses: Use of various buses such as CAN, LIN, Flex Ray. Recent trends in automotive buses (Such as OBDI1. MOST, IE, IELI.I, D2B and DSI). Application of Telematics in Automotive: Global Positioning Systems (GPS) and General Packet Radio Service (GPRS), | **07 Hrs** |

| | |
|---|---|
| for use in an automotive environment. Vehicle to Vehicle Communication Higher End Technology: Comparative Study and applications of ARM Cortex-Ascries/M-scries. ARM 9 and ARM11. | |
| **UNIT-V** | |
| **Diagnostics and Safety in Automotive:** Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system. Preliminary checks and adjustments, Self-Diagnostic system. Fault finding and corrective measures. Electronic transmission checks and Diagnosis, Diagnostic procedures and sequence. On board and off board diagnostics in Automotive. Safety in Automotive: Safety norms and standards. Passenger comfort and security systems. Future trends in Automotive Electronics. | **07 Hrs** |

| **Course Outcomes: After completing the course, the students will be able to** | |
|---|---|
| **CO1:** | Acquire the knowledge of automotive domain fundamentals and need of electronics in Automotive systems |
| **CO2:** | Apply various sensors and actuators for Automotive applications |
| **CO3:** | Analyze different control systems and communication interfaces used in automotive systems. |
| **CO4:** | Evaluate the performance of telematics Diagnostics and safety norms in Automotive Systems. |

| **Reference Books** | |
|---|---|
| **1.** | Understanding Automotive Electronics, Williams. B. Ribbens, 6th Edition, 2003, Elsevier science, Newness publication, ISBN-9780080481494. |
| **2.** | Automotive Electronics Handbook, Robert Bosch, 2004, John Wiley and Sons, |
| **3.** | Automotive Embedded Systems Handbook, Nicolas Navet, F Simonot-Lion, Industrial Information Technology Series, CRC press. |
| **4.** | Automotive Control Systems Engine, Driveline and vehicle, Uwekiencke and lars Nielsen, Springer, 2nd Edition, 2005, ISBN 0-387-95368X |

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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| **CO-PO Mapping** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **3** | **1** | **2** | **1** | **-** | **-** | **1** | **-** | **-** | **-** | **-** | **1** |
| **CO2** | **3** | **2** | **2** | **1** | **-** | **1** | **-** | **-** | **-** | **1** | **-** | **1** |
| **CO3** | **3** | **2** | **2** | **1** | **-** | **1** | **-** | **-** | **2** | **-** | **1** | **1** |
| **CO4** | **3** | **1** | **2** | **1** | **2** | **1** | **-** | **-** | **1** | **-** | **-** | **-** |

**Low-1 Medium-2 High-3**

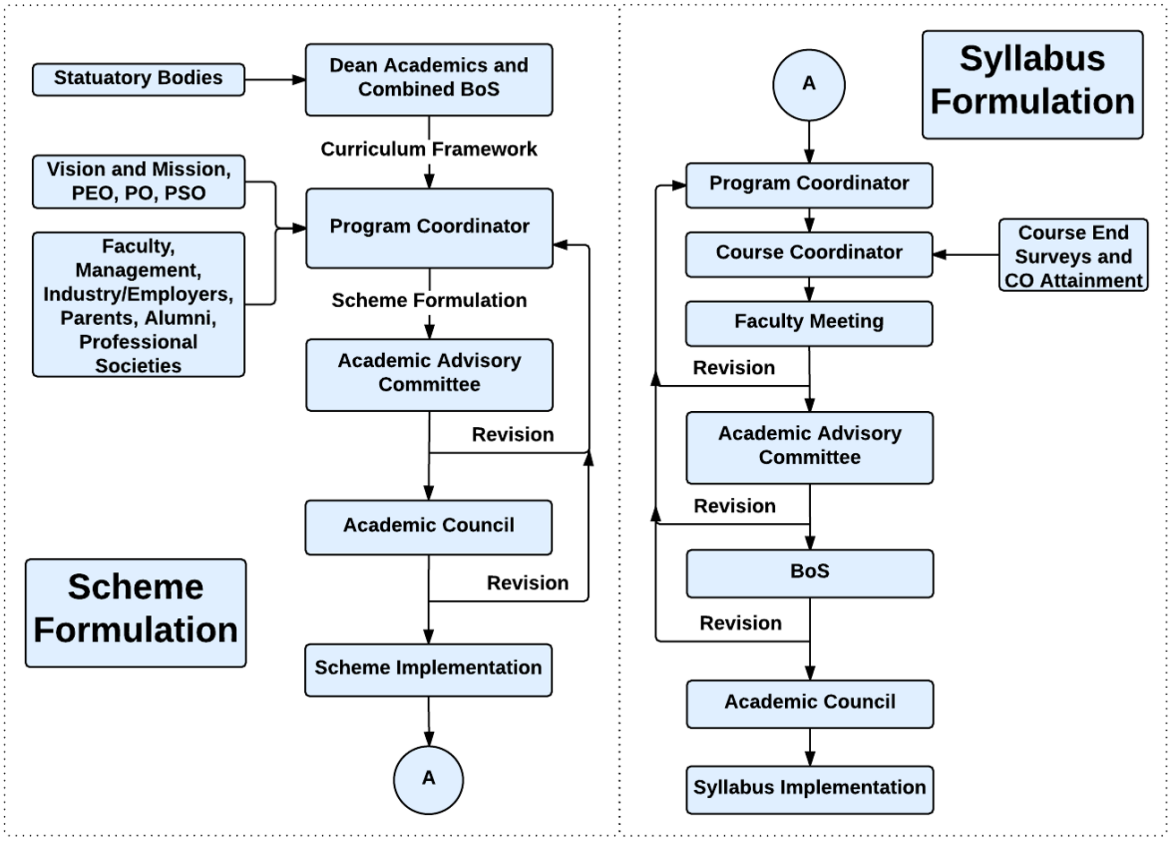
## Credits Distribution as per UGC/VTU

| Sl. No. | Category | Percentage (%) | Minimum No. of credits | Assigned No. Of credits 2012 | 2016 scheme | |
|---|---|---|---|---|---|---|
| | | | | | Without Mini Project | With Mini Project |
| 1 | Humanities | 5-10 | 10 | 10 | 9+2 | 9+2 |
| 2 | Basic Science | 15-20 | 30 | 28 | 30 | 30 |
| 3 | Engineering Science | 15-20 | 30 | 28 | 30 | 30 |
| 4 | Professional Core Courses (PC) | 30-40 | 60 | 80 | 78+3=81 (3 credits core in place of Minor project in 7th semester) | 81-3=78 (3 Credits for minor project in 7th semester) |
| 5 | Professional Elective Courses | 10-15 | 20 | 20 | 20 | 20 |
| 6 | Other Electives | 5-10 | 10 | 11 | 10 | 10 |
| 7 | Project Work | 10-15 | 20 | 23 + 2 | 16+2 Major project +Tech. Seminar | 16+2+3 Major project +Tech. Seminar +Mini Project |
| **Total No. of Credits** | | | | | 200 | 200 |

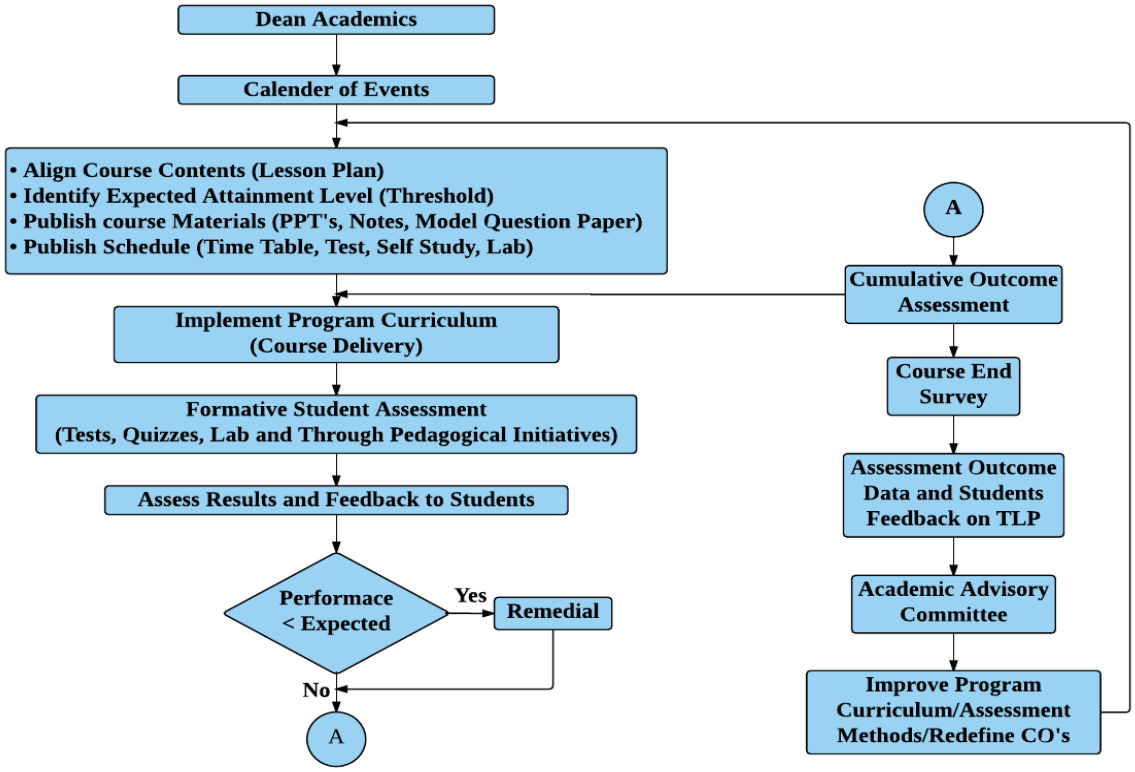
| SEMESTER WISE CREDIT DISTRIBUTION (SELF STUDY CREDIT INCLUDED EXCEPT FOR VII SEM) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **I** | **II** | **III** | **IV** | **V** | **VI** | **VII** | **VIII** | **TOTAL** |
| 25 (P)/25( C ) | 25/25 | 25 | 25 | 29 | 28 | 23 | 20 | 200 |

| PROFESSIONAL CORE COURSE(PC) | PROFESSIONAL ELECTIVE COURSES(PES) | OTHER ELECTIVES(OE) |
|---|---|---|
| Common syllabus to be set jointly for such core Courses offered by two or more departments (Mandatory requirement) | Branch specific latest/Advanced Courses. | Include Courses which can be offered by various departments as group/global elective to other departments. |

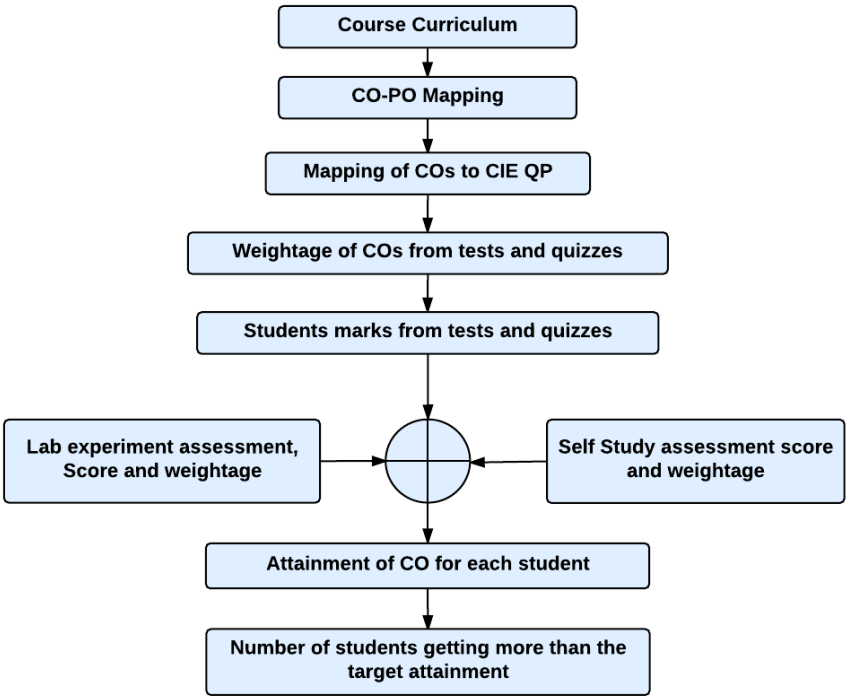
## Curriculum Design Process



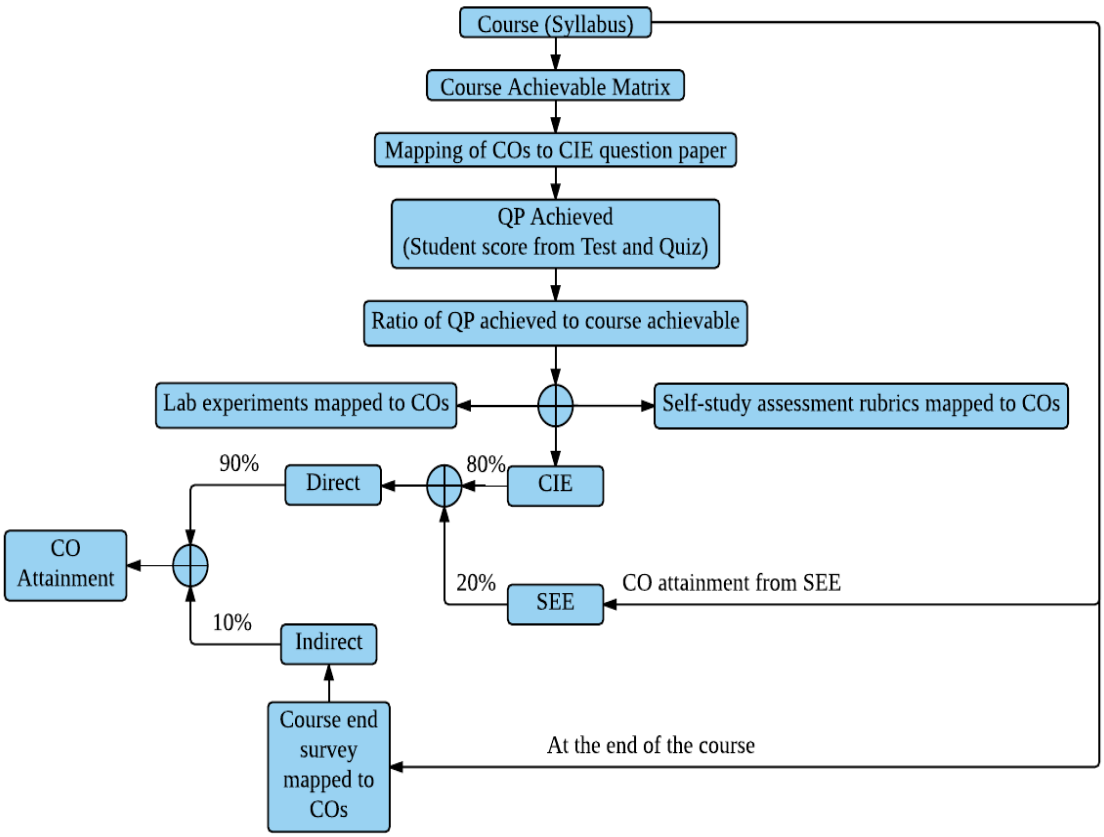

## Academic Planning and Implementation



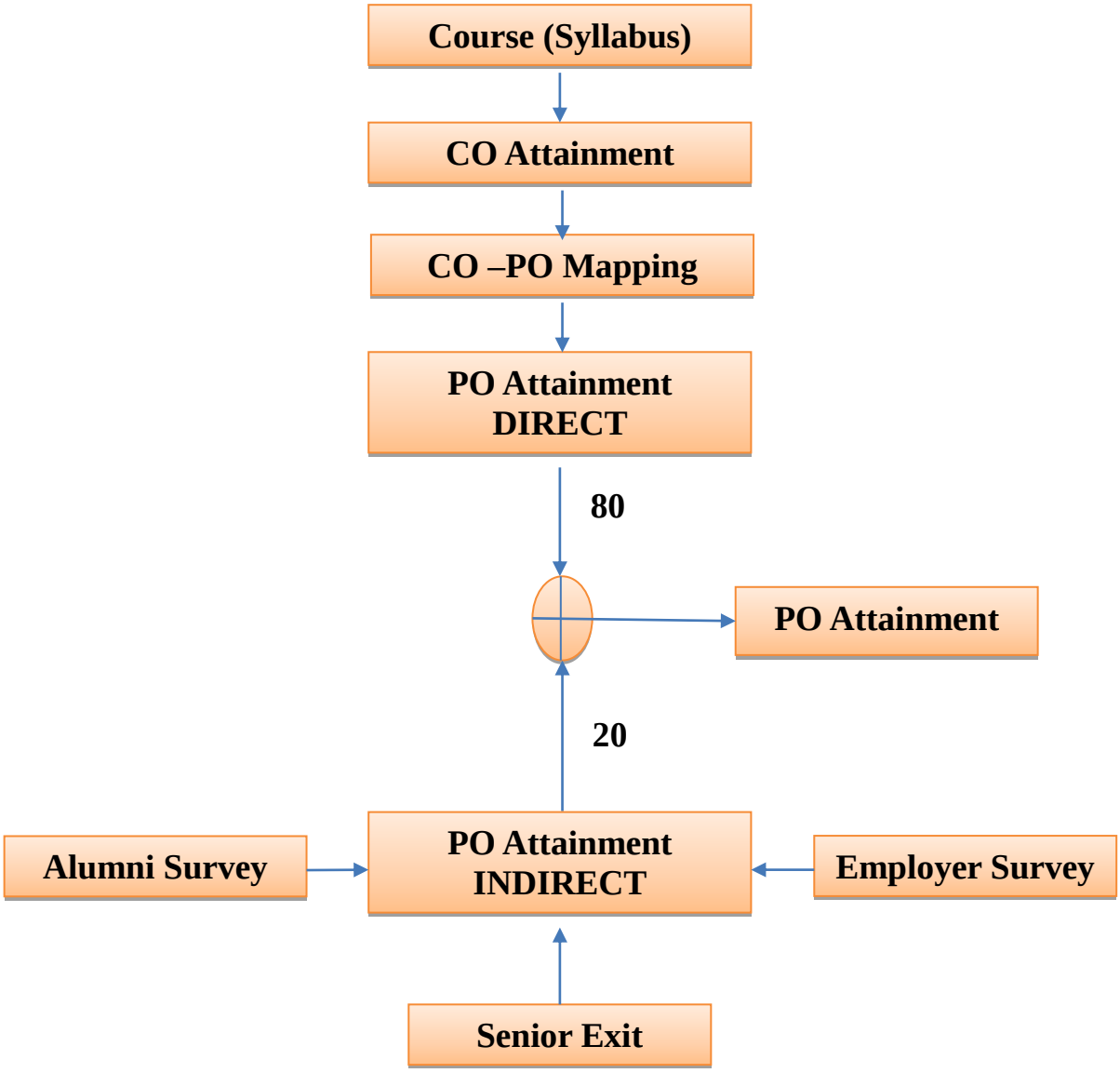
## PROCESS FOR COURSE OUTCOME ATTAINMENT




## Final CO Attainment Process



**Program Outcome Attainment Process**




Guidelines for Fixing Targets

- The target may be fixed based on last 3 years' average attainment