Rashtreeya Sikshana Samithi Trust

R. V. College of Engineering

(Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi)

Department of Electronics & Communication Engineering

Master of Technology (M. Tech.)

VLSI DESIGN & EMBEDDED SYSTEMS

Scheme and Syllabus of Autonomous System w.e.f 2016

R.V. College of Engineering, Bengaluru – 59

(Autonomous Institution affiliated to Visvesvaraya Technological University, Belagavi)

Department of Electronics & Communication Engineering

Vision:

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering.

Mission:

- To impart quality technical education to produce industry-ready engineers with a research outlook.
- To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.
- To create centers of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.
- To develop entrepreneurial skills among the graduates to create new employment opportunities.

MASTER OF VLSI DESIGN & EMBEDDED SYSTEMS - Program

Program Educational Objectives (PEO)

M. Tech. in VLSI design and Embedded Systems Program, graduates will be able to:

PEO 1. Identify and apply appropriate Electronic Design Automation (EDA) to solve real world problems in VLSI and Embedded Systems domain to create innovative products and systems

PEO 2. Develop managerial skill and apply appropriate approaches in the domains of VLSI design and Embedded Systems incorporating safety, sustainability and become a successful professional or an Entrepreneur in the domain

PEO 3. Pursue career in research in VLSI Design and Embedded Systems domain through self learning and self directed on cutting edge technologies

Program Outcomes (PO)

M. Tech. in VLSI Design and Embedded Systems Program graduates will be able to:

PO 1. Scholarship of Knowledge: Acquire in-depth knowledge of VLSI and Embedded systems in wider and global perspective, with an ability to discriminate, evaluate, analyze, synthesize and integrate for enhancement of knowledge.

PO 2. Critical Thinking: Analyze electronics engineering problems critically; apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research.

PO 3. Problem Solving: Think laterally and originally, conceptualize and solve technical problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

PO 4. Research Skill: Extract information through literature survey and experiments pertinent to unfamiliar problems, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze, demonstrate higher order skill, contribute individually/in group(s) to the development of scientific/technological knowledge in techno-managerial systems.

PO 5. Usage of modern tools: Create, select, learn and apply appropriate techniques, resources, and modern engineering and EDA tools including emulators for modeling and prototyping with an understanding of the tools limitations.

PO 6. Collaborative and Multidisciplinary work: Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

PO 7. Project Management and Finance: Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors.

PO 8. Communication: Communicate with the engineering community and society at large confidently and effectively to comprehend and write effective reports/design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

PO 9. Life-long Learning: Recognize the need for, and have the preparation and ability to engage in lifelong learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO 10. Ethical Practices and Social Responsibility: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO 11. Independent and Reflective Learning: Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes with or without depending on external feedback.

Program Specific Criteria (PSC)

Lead Society: Institute of Electrical and Electronics Engineers

1. Curriculum:

The curriculum shall include competency areas in VLSI Design & Embedded Systems including IC designing concepts & Embedded system designing concepts to analyze and design complex systems containing hardware and software components. The curriculum must prepare graduates for design and development of VLSI as well as Embedded Systems for different applications.

2. Faculty

The professional competence of the faculty must be in Analog IC Design, Digital IC Design, Embedded Systems Design and allied areas of VLSI as well as Embedded domains.

Program Specific Outcomes (PSO)

M. Tech. in VLSI Design and Embedded Systems Program graduates will be able to:

PSO 1. Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing, Verification and prototype development focusing on applications.

PSO 2. Integrate multiple sub-systems to develop System On Chip, optimize its performance and excel in industry sectors related to VLSI / Embedded domain.

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Department of Electronics & Communication Engineering

M. Tech. VLSI Design & Embedded Systems

FIRST SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MEM11R	Research Methodology	IM	3	1	0	0	4
2	16MVE12	Digital IC Design (Theory and Practice)	EC	4	0	1	0	5
3	16MVE13	Advanced Embedded System Design	EC	4	0	0	1	5
4	16MVE14	Digital System Design using Verilog	EC	4	0	0	0	4
5	16MVE15x	Elective 1	EC	4	0	0	0	4
6	16HSS16	Professional Skill Development	HSS	0	0	2	0	2
		Total		**19**	**1**	**3**	**1**	**24**

Elective-1			
16MVE151	Advanced Embedded Processors	16MVE152	ASIC Design

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Department of Electronics & Communication Engineering

M. Tech. VLSI Design & Embedded Systems

SECOND SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MEM21P	Project Management	IM	3	1	0	0	4
2	16MVE22	Analog IC Design (Theory and Practice)	EC	4	0	1	0	5
3	16MVE23x	Elective-2	EC	4	0	0	0	4
4	16MVE24x	Elective-3	EC	4	0	0	0	4
5	16MVE25x	Elective-4	EC	4	0	0	0	4
6	16MVE26	Minor Project	EC	0	0	5	0	5
		Total		**19**	**1**	**6**	**0**	**26**

Elective-2			
16MVE231	CAD Tools for VLSI	16MVE232	Real Time Embedded Systems
Elective-3			
16MVE241	Low Power VLSI Design	16MVE242	Advanced Embedded Programming
Elective-4			
16MVE251	High Speed VLSI Design	16MVE252	MEMS and Smart Systems

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Department of Electronics & Communication Engineering

M. Tech. VLSI Design & Embedded Systems

THIRD SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MVE31	System Verilog for Design & Verification of Digital Systems (Theory and Practice)	EC	4	0	1	0	5
2	16MVE32x	Elective-5	EC	4	0	0	0	4
3	16MVE33x	Elective-6	EC	4	0	0	0	4
4	16MVE34x	Elective-7	EC	4	0	0	0	4
5	16MVE35	Internship/Industrial Training	EC	0	0	3	0	3
6	16MVE36	Technical Seminar	EC	0	0	2	0	2
		Total		**16**	**0**	**6**	**0**	**22**

Elective-5			
16MVE321	Embedded System for Networking	16MVE322	Radio Frequency IC Design
Elective-6			
16MVE331	ARM programming and optimization	16MVE332	VLSI Testing
Elective-7			
16MVE341	Mixed Signal IC Design	16MVE342	Synthesis & Optimization of Digital Circuits

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M. Tech. VLSI Design & Embedded Systems

FOURTH SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MVE41	Major Project	EC	0	0	26	0	26
2	16MVE42	Seminar	EC	0	0	2	0	2
		Total		**0**	**0**	**28**	**0**	**28**

FIRST SEMESTER

RESEARCH METHODOLOGY						
Course Code	**:**	**16MEM11R**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L: T: P: S**	**3:2:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**04**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

Students are able to

1. Understand of the underlying principles of quantitative and qualitative research
2. Perform the gap analysis and identify the overall process of designing a research study.
3. Choose the most appropriate research methodology to address a particular research problem
4. Explain a range of quantitative and qualitative approaches to analyze data and suggest possible solutions.

Unit – I	**7 Hours**

Overview of Research

Meaning of Research, Types of Research, Research and Scientific Method, Defining the Research Problem, Research Design, Different Research Designs.

Unit – II	**7 Hours**

Methods of Data Collection

Collection of Primary Data, Observation Method, Interview Method, Collection of Data through Questionnaires, Collection of Data through Schedules, Collection of Secondary Data, Selection of Appropriate Method for Data Collection.

Unit – III	**8 Hours**

Sampling Methods

Sampling process, Non-probability sampling, probability sampling: simple random sampling, stratified sampling, cluster sampling systematic random sampling, Determination of sample size, simple numerical problems.

Unit – IV	**7 Hours**

Processing and analysis of Data

Processing Operations, Types of Analysis, Statistics in Research, Measures of: Central Tendency, Dispersion, Asymmetry and Relationship, correlation and regression, Testing of Hypotheses for single sampling: Parametric (t, z and F) Chi Square, ANOVA, and non-parametric tests, numerical problems.

Unit-V	**7 Hours**

Essential of Report writing and Ethical issues:

Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Precautions for Writing Research Reports.

Syllabus includes 12 hours of tutorials in which:

- Faculty is expected to discuss research methodology for specializations under consideration.
- Numerical problems on statistical analysis as required for the domains in which students are studying must be discussed.
- Statistical analysis using MINITAB/ MATLAB and such other software's can be introduced.

Course Outcomes:

After going through this course the students will be able to

CO 1. Explain various principles and concepts of research methodology.

CO 2. Apply appropriate method of data collection and analyze using statistical methods.

CO 3. Analyze research outputs in a structured manner and prepare report as per the technical and ethical standards.

CO 4. Formulate research methodology for a given engineering and management problem situation.

Reference Books:

1. Kothari C.R., "Research Methodology Methods and techniques", New Age International, 2004, ISBN: 9788122415223
2. Krishnaswami, K.N., Sivakumar, A. I. and Mathirajan, M., "Management Research Methodology", Pearson Education India, 2009 Edition, ISBN:9788177585636
3. Levin, R.I. and Rubin, D.S., "Statistics for Management", 7th Edition, Pearson Education: New Delhi, ISBN-13: 978-8177585841

Scheme of Continuous Internal Evaluation (CIE)

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE)

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	M	---	---	M	----	----	---	H	---	H	-----
CO2	---	L	H	H	M	M	L	L	----	M	L
CO3	L	M	M	M	H	M	L	M	---	---	M
CO4	H	H	H	H	----	L	L	M	H	---	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2	PSO3
CO1			
CO2			L
CO3			
CO4	L		

DIGITAL IC DESIGN (Theory and Practice)						
Course Code	**:**	**16MVE12**		**CIE Marks**	**:**	**100+50**
Hrs/Week	**:**	**L:T:P:S**	**4:0:2:0**	**SEE Marks**	**:**	**100+50**
Credits	**:**	**5**		**SEE Duration**	**:**	**3 Hrs + 3 Hrs**

Course Learning Objectives (CLOs):

Student shall be able to

1. Estimate the static parameters of the CMOS inverter voltage transfer curve and use a circuit simulator to study the circuit response
2. Use transistor sizing techniques for minimizing delay through a single combinational logic gate or a chain of logic gates
3. Appreciate and estimate the interconnect parasitics, particular capacitance and resistance and timing issues in a digital system
4. Understand, analyze and design arithmetic as well as memory circuits

Unit – I	**10 Hrs**

Introduction: Issues in Digital IC Design, Design abstraction levels in digital circuits, Quality Metrics of a Digital Design

MOS Transistor: Device structure, MOSFET- static & dynamic behavior, secondary effects, technology scaling

Manufacturing CMOS Integrated Circuits: Silicon wafer, Photolithography

Unit – II	**10Hrs**

CMOS inverter: Static CMOS Inverter: static and dynamic Behavior, Components of Energy and Power

CMOS Combinational Logic Circuit Design: Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic. Dynamic CMOS Design: Dynamic Logic Design Considerations. Speed and Power Dissipation of Dynamic logic, Signal integrity issues, Cascading Dynamic gates.

Unit – III	**10Hrs**

CMOS Sequential Logic Circuit Design: Static Latches and Registers. Dynamic Latches and Registers. Pulse Based Registers. Sense Amplifier based registers. Pipelining concepts.

Implementation strategies for Digital ICs: Digital circuit implementation approaches- overview Custom circuit design, cell based design methodology, semicustom design flow.

Unit – IV	**10Hrs**

Interconnects: Resistive, Capacitive and Inductive Parasitics (basics)

Timing Issues: Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and Impact on Performance. Clock Distribution techniques, Latch based clocking.

Unit – V	**10Hrs**

Arithmetic building blocks design: Data paths in digital processor architectures – Adder, binary adder, static adder, mirror adder, TG based adder, carry bypass adder, linear and square root carry select adder, carry lookahead adder, Multiplier- array, carry save multiplier

Memory & Array structures design: Memory core – ROM, SRAM, DRAM, Sense amplifiers,

CAM

Lab Component

1. Introduction to Cadence environment; setup Linux environment; create schematic and symbol, introduction to netlist, technology library.
2. DC and transient analysis of CMOS inverter
3. Layout, DRC, LVS, RCX and post-layout simulation of CMOS Inverter
4. Design and Analysis of NAND, NOR and complex gates
5. Design and Analysis of CMOS Adders
6. Layout of CMOS NAND, NOR and complex gates
7. Design and characterization of Transmission gates, Latches and Flip-flops
8. Standard cell generation for inverter using spectre
9. Standard cell generation for basic gates using ELC

Expected Course Outcomes:

After taking up this course, the graduate will be able to:

CO1: Investigate device, circuit & system aspects of digital IC design
CO2: Analyze the functionality of digital integrated circuits & systems
CO3: Design and implement digital integrated circuit & systems
CO4: Evaluate the different performance parameters of a digital integrated circuits & systems

Reference Books:

1.	Jan M.Rabaey, Anantha Chadrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", (2/e), Pearson 2016, ISBN-13: 978-0130909961
2.	Erik Brunvand, "Digital VLSI Chip Design with Cadence and Synopsys CAD Tools", Pearson 2009, ISBN-13: 9780321547743
3.	David A Hodges, Horace G Jackson and Resve A Saleh, "Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology" TMH.2005, ISBN-13: 978-0072283655
4.	Sung MO Kang, Yousuf Leblebici, "CMOS Digital Integrated Circuits"; Tata McGrawHill, (3/e), ISBN: 0-7923-7246-8
5.	Neil H.E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design", Pearson Education, (3/e), 2006,ISBN: 0321149017

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Continuous Internal Evaluation (CIE) for Practical

CIE for the practical courses will be based on the performance of the student in the laboratory, every week. The laboratory records will be evaluated for 40 marks. One test will be conducted for 10 marks. The total marks for CIE (Practical) will be for 50 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Practical

SEE for the practical courses will be based on conducting the experiments and proper results for 40 marks and 10 marks for viva-voce. The total marks for SEE (Practical) will be 50 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H										
CO2	H	H		M	H				M		
CO3	H	H	H	H	H			M	M	M	
CO4	H		H		H				M		M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	M
CO2		H
CO3	M	M
CO4	H	H

Advanced Embedded System Design						
Course Code	**:**	**16MVE13**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:1**	**SEE Marks**	**:**	**100**
Credits	**:**	**5**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

Student shall be able to

1. Understand embedded computing system, design process and basic building blocks of an embedded system.
2. Illustrate how microprocessor, memory, peripheral components and buses build an embedded platform and their interaction.
3. Evaluate how architectural and implementation design decisions influence performance and power dissipation.
4. Assembly and testing the operation of real-time embedded application programs through hands-on experience with a single-board computer.

Unit – I	**10 Hrs**

Introduction to Embedded System Design

Introduction, Characteristics of Embedding Computing Applications, Concept of Real time Systems, Challenges in Embedded System Design, Design Process: Requirements, Specifications, Hardware Software Partitioning, Architecture Design, Designing of Components, System Integration

Embedded System Architecture

Instruction Set Architectures with examples, Memory system Architecture: Von Neumann, Harvard, caches, Virtual Memory, Memory Management, I/O sub system: Busy wait I/O,DMA, Interrupt Driven I/O, Co-Processor & Hardware Accelerators, Processor performance Enhancement: Pipelining, Superscalar Execution, Multi Core CPUs, CPU Power Consumption, Benchmarking Standards: MIPS, MFLOPS, MMACS, Coremark

Unit – II	**10 Hrs**

Designing Embedded System Hardware –I

CPU Bus: Bus Protocols, Bus Organisation, Memory Devices and their Characteristics: RAM, EEPROM, Flash Memory, DRAM; I/O Devices: Timers and Counters, Watchdog Timers, PWM, Interrupt, Controllers, DMA Controllers, A/D and D/A Converters, Displays, Keyboards, Infrared devices

Unit – III	**10 Hrs**

Designing Embedded System Hardware –II

Component Interfacing: Memory interfacing with case study; I/O Device Interfacing with case Study: Programmed IO, Memory Mapped IO, Interfacing Protocols: SPI, I2C, CAN, USB,Reset Circuits, Designing with Processors: System Architecture, FPGA based Design, Processor Selection Criteria

Unit – IV	**10 Hrs**

Designing Embedded System Software –I

Application Software, System Software, Use of High Level Languages: C,C++,Java, Programming & Integrated Development Environment tools: Editor, Compiler, Linker, Automatic Code Generators, Debugger, Board Support Library, Chip Support Library, Analysis and Optimization: Execution Time, Energy & Power, Program Size; Program Validation & Verification, Embedded System Coding Standards: MISRA C 2012/CERT, Standards in Automobiles, Aerospace &Biomedical Applications.

Unit – V	**10 Hrs**

Designing Embedded System Software –II

OS based Design, Real Time Kernel, Process& Thread, Inter Process Communications, Synchronization, Case Study: RTX-ARM, Evaluating and Optimising Operating System Performance: Response time Calculation, Interrupt Latency, Time Loading, Memory Loading, Case Study: Embedded Control Applications-Software Coding of a PID Controller, PID Tuning, IoT based Resource Monitoring

Expected Course Outcomes:

After going through this course the student will be able to:

CO1: Describe hardware & software of an embedded systems for real time applications with suitable processor architecture, memory and communication interface.
CO2: Design embedded software & hardware to meet given constraints with the help of modern engineering tools.
CO3: Demonstrate compliance of prescribed safety norms through implementation of the identified engineering problems pertaining to automobiles, aerospace & biomedical applications.
CO4: Design, implement and demonstrate open ended problem to access their capabilities through assignments.

Reference Books:

1.	James K Peckol, "Embedded Systems – A contemporary Design Tool", John Weily, 2008, ISBN: 0-444-51616-6
2.	Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009, ISBN: 10: 0070678790
3.	David E.Simon, "Embedded Software Primer",Addison Wesley,1999,ISBN-13: 978-0201615692
4.	Barry B.Brey, "The Intel Micro-processors, Architecture, Programming and Interfacing", 6th Edition, Pearson Education, 2008, ISBN 0-13-502645-8

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M		H							H
CO2		H	H		H		H				
CO3							M	H	M	H	
CO4	H	H		H	M	M	M	M	H	M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	M
CO2	M	H
CO3	M	M
CO4	H	M

DIGITAL SYSTEM DESIGN USING VERILOG						
Course Code	**:**	**16MVE14**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

At the end of the course the student shall be able to:

1. Understand the need of HDL for digital system design, and advantages of VERILOG HDL over VHDL in designing digital systems.
2. Explain the underlying basics of number systems, representation and arithmetic based on real and integer numbers; in particular floating point representations.
3. Explain the implementation basics of combinational sub-systems, sequential sub-systems and implementation fabrics such as FPGAs, CPLDs, etc and their use in high end system designs.
4. Gain knowledge of complete system design using VERILOG HDL, the design methodology and Interfacing concepts.

Unit – I	**10 Hrs**

Introduction to System Design, Verilog and System Verilog: Introduction: Digital Systems and Embedded Systems, Real-world circuits. Design Methodology: Design flow-Architecture, Functional design and verification, Synthesis, Physical design. Design optimization-Area, Timing and Power, Design for Test-Fault models and simulation, Scan design and boundary scan, BIST.

Introduction to Verilog : Verilog and its IEEE standards, Application Areas and Abstraction levels, Need of verification of HDL design, Simulation and Synthesis, Test-benches, Basics; Keywords, Identifiers, Numbers representation, data types, Nets, Registers, Arrays, Vectors, Operators, delays, Verilog Value Set. Introduction to Gate Level Modelling, Data flow modelling and Behavioral Level modeling.

Unit – II	**10 Hrs**

Design of Combinational Systems: Number Basics: Unsigned and Signed Integers, Fixed-point and Floating-point Numbers. Boolean Functions and Boolean Algebra, Verilog models for Boolean switching function, Binary Coding.

Combinational Components and Circuits: Design of gate primitives, Gate level modelling of Arithmetic circuits, Multiplexers, Encoders and Decoders, Data flow modelling of Arithmetic circuits, Multiplexers, Encoders and Decoders, Behavioral Level modelling of Arithmetic circuits, Multiplexers, Encoders and Decoders, Verification of Combinational Circuits.

Unit – III	**10 Hrs**

Design of Sequential Systems: Storage elements: Latches and Flip-Flops, Registers and shift registers. Counters: Asynchronous and synchronous, Sequential Data-paths and Control: FSMs, Clocked Synchronous Timing Methodology: Asynchronous inputs, Verification of Sequential Circuits, Asynchronous timing methodologies.

Unit – IV	**10 Hrs**

Processor Design and System Development: Embedded Computer Organization, Instruction and Data, Memory Interfacing.I/O Interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.

Unit – V	**10 Hrs**

System Accelerators, Implementation Fabrics and UDPs

System Accelerators: Concepts, Case study: Video Edge detection, Verification of accelerators. Implementation Fabrics, Memories: Concepts, Memory Types, Error Detection and Correction. ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity, User-Defined Primitives: Combinational Primitives: Basic Features of User-Defined Primitives, Describing Combinational Logic Circuits. Sequential Primitives: Level-Sensitive Primitives, Edge-Sensitive Primitives.

Expected Course Outcomes:

After taking up this course, the graduate will be able to:

CO1: Understand the digital system designs skills using VERILOG HDL based on IEEE-1364 standards and managed by Open Verilog International (OVI).

CO2: Demonstrate the skill on cost-effective system designs through proper selection of implementation fabrics for the desired application.

CO3: Analyze complete systems and build small scale applications using Interfacing concepts.

CO4: Design and implement complete digital systems using VERILOG HDL and demonstrate the innovation skills.

Reference Books:

1.	Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elsevier,2015, ISBN: 978-0-12-369527-7
2.	Charles Roth, Lizy K. John, Byeong Kil Lee, "Digital Systems Design Using Verilog," Cengage Learning, 2015, *ISBN*-10: 1285051076
3.	Thomas & Moorby, "The Verilog H D L," 5E, Kluwer Academic Publishers, New York, USA, 2002, ISBN: 1-4020-7089-6
4.	Navabi, "Verilog digital systems design," McGraw Hill,2005, ISBN: 0-07-047164-9.

Scheme of Continuous Internal Evaluation (CIE) for Theory

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Scheme of Semester End Examination (SEE) for Theory

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Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	L	M	M	L	H	L	L	L			
CO2	H	L	L	L	M	L	M		L		L
CO3	H	H	H	H	M	L	L		M	M	L
CO4	M	L	H	M	H	L	M	L	L	M	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	H
CO2	H	H
CO3	M	M
CO4	H	H

ADVANCED EMBEDDED PROCESSORS						
Course Code	**:**	**16MVE151**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Prerequisites :

Fundamentals of digital Electronics, Embedded Processor

Course Learning Objectives (CLOs):

Student shall be able to

1. Understand the architecture of different processors suitable for embedded system.
2. To gain knowledge on ARM cortex-M series CPU architecture, instruction set, exceptions, memory & special OS features.
3. Identify the design issues ARM based embedded system with the basic knowledge of firmware, embedded OS & ARM architectures.
4. Analyse the execution of instructions/program knowing the basic principles of ARM architecture and assembly language & the special features of Cortex-M3/M4 to realize signal processing applications.

Unit – I	**10 Hrs**

Introduction

Embedded Processor Selection, PowerPC,ARM Cortex, SoC, Digital Signal Processors

ARM Cortex-M Series Technical Overview

Cortex-M Processor Family, Product Portfolio, Advantages, Applications, Cortex Microcontroller Software Interface Standard (CMSIS), General Information, Features

Unit – II	**10 Hrs**

Architecture of ARM Cortex-M Processor

Programmer's Model, Application Program Status Register (APSR), Memory System, Exceptions & Interrupts, System Control Block, Debug, Reset & Reset Sequence

Instruction Set-I

Assembly Language Syntax, Suffixes for Assembly Instructions, Unified Assembly Language, Assembly Instructions

Unit – III	**10 Hrs**

Instruction Set-II

Cortex-M4/M7 Specific Instructions, Barrel Shifter

Memory System

Memory Map, Connecting Cortex-M3/M4 with Memory & Peripherals, Endianness, Data Alignment & Unaligned Data Access Support, Bit Band Operations, Memory Access Attributes, Exclusive Access, Memory Barriers, Memory System in a MCU.

Unit – IV	**10 Hrs**

Exceptions & Interrupts

Overview of Exceptions and Interrupts, Exception Types, Interrupt Management, Vector Table & Vector Table Relocation, Interrupts Inputs & Pending Behaviours, Exceptions Sequence

Overview, Details pf NVIC Registers for Interrupt Control, SCB Registers for Exceptions & Interrupt Control, Special Registers for Exceptions Masking, Procedures in Setting up Interrupts, Software Interrupts. Exception Handler in C, Stack Frames, Exception Sequences.

Unit – V	**10 Hrs**

Low Power and System Control Features

Low Power Designs, Low Power Features, Using WFI & WFE Instructions in for Programming, Developing Low Power Applications, The SysTick Timer, Self-Reset, CPU ID Base Register, Configuration Control Register, Auxiliary Control Registers, Co-Processor Access Control Register.

OS Support Features

Shadowed Stack Pointer, SVC Exception, PendSV Exception, Context Switching in Action, Exclusive Accesses.

Expected Course Outcomes:

After going through this course the student will be able to:

CO1. Understand the architecture, instruction set, memory organization and addressing modes of the embedded processors.

CO2. Realize real time signal processing applications & primitive OS operations on different ARM architectures by making use of software libraries.

CO3. Perform market survey of available embedded processors & arrive at the required processor for solving the given problem statement.

CO4. Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments.

Reference Books:

1.	Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3& M4 Processors", 3rd Edition, Newnes (Elsevier), 2014, ISBN:978-93-5107-175-4
2.	Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publishers, 2008, ISBN-13:9788181476463
3.	Steve Furber, "ARM System on Chip Architecture", Pearson Education Limited, 2nd Edition,2000, ISBN-13:9780201675191
4.	Technical reference manual for ARM processor cores, including Cortex M3, M4, M7 processor families.

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	H									
CO2	M	H	H	H							
CO3				H			M	M			M
CO4	M	H	M	M	H		M	H	H	M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	H
CO2	H	M
CO3	M	M
CO4	H	H

ASIC DESIGN						
Course Code	**:**	**16 MVE152**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

Student shall be able to

1. Understand the fundamentals of ASIC and its design methods
2. Differentiate between ASICs and FPGAs, standard cells, cell libraries, IPs.
3. Gain knowledge on programmable architectures for ASICs and explain the physical design of ASIC including floor planning, placement and Routing.
4. Design a core from specs to GDSII.

Unit – I **10 Hrs**

Introduction to ASICs

Types of ASICs: Full Custom ASIC, Semi-custom based ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channelless gate array, Structured gate array, Programmable logic devices, FPGA.

Design flow.

Unit – II **10 Hrs**

CMOS Logic

Combinational logic cells Sequential logic cells: Latch, flipflop, clocked inverter**.**

Data logic cells: Data Path Elements, Adders, Multipliers, Arithmetic operator.(Practical approach).

I/O Cell, Cell Compilers

Unit – III **10 Hrs**

ASIC Library Design

Logical effort: predicting delay, logical area and logical efficiency, logical paths, multi stage cells, optimum delay, optimum no. of stages.

Library cell design.

Programmable ASICS: The Antifuse, Static RAM, EPROM and EEPROM technology.

Unit – IV **10 Hrs**

Programmable ASICs logic cells

Actel ACT: ACT1 logic module, Shannon's expansion theorem, Multiplexer logic as function generators, Timing models and critical path, speed gating, worst case timing.

Programmable ASIC Design Software: Design System, logic synthesis**,** Introduction to Synthesis and Simulation. (Practical analysis of the design parameters for speed, area & power optimization).

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation.

Unit – V **10 Hrs**

ASIC Construction Floor Planning and Placement & Routing

Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative

placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

Expected Course Outcomes:

After taking up this course, the graduate will be able to:

CO1: Investigate the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test.
CO2: Apply & analyze the design parameters for speed, area & power optimization.
CO3: Develop the algorithms required for the design of ASIC.
CO4: Apply the back-end physical design flow, including floorplanning, placement, and routing techniques

Reference Books:

1.	M.J.S .Smith, - "Application - Specific Integrated Circuits" – Pearson Education, 2003, ISBN:978-817758-408-0
2.	H. Bhatnagar, - "Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime", 2nd edition, 2001, ISBN:0792385373
3.	Farzad Nekoogar Farak Nekooga From ASICs-to-SOCs: A Practical Approach, PHI,2003 ISBN: 0-13-033857-5.
4.	P. Kurup, T. Abbasi, "Logic Synthesis Using Synopsys",Springer, 1995,ISBN 0-7923-9582-4

Scheme of Continuous Internal Evaluation (CIE) for Theory

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Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	M	H	M	L	H	L	M	M	H		
CO2	H	M	H	L	H	M	M	H	M		
CO3	M	M	M	L	H	M	H	M	M	M	M
CO4	H	M	H	L	H	H	M	H	M	H	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	M
CO2	H	H
CO3	M	H
CO4	H	H

PROFESSIONAL SKILL DEVELOPMENT						
Course Code	**:**	**16HSS16**		**CIE Marks**	**:**	**50**
Hrs/Week	**:**	**L:T:P:S**	**0:0:4:0**	**Credits**	**:**	**02**

Course Learning Objectives:

Students are able to

1. Understand the importance of verbal and written communication
2. Improve qualitative and quantitative problem solving skills
3. Apply critical and logical think process to specific problems
4. Manage stress by applying stress management skills

UNIT 1	5 Hours

Communication Skills: Basics of Communication, Personal Skills & Presentation Skills, Attitudinal Development, Self Confidence, SWOC analysis.

Resume Writing: Understanding the basic essentials for a resume, Resume writing tips Guidelines for better presentation of facts.

UNIT 2	6 Hours

Quantitative Aptitude and Data Analysis*:* Number Systems, Math Vocabulary, fraction decimals, digit places etc. Reasoning and Logical Aptitude, - Introduction to puzzle and games organizing information, parts of an argument, common flaws, arguments and assumptions. Verbal Analogies – introduction to different question types – analogies, sentence completions, sentence corrections, antonyms/synonyms, vocabulary building etc. Reading Comprehension, Problem Solving

UNIT 3	4 Hours

Interview Skills: Questions asked & how to handle them, Body language in interview, Etiquette, Dress code in interview, Behavioral and technical interviews, Mock interviews - Mock interviews with different Panels. Practice on Stress Interviews, Technical Interviews, General HR interviews

UNIT 4	5 Hours

Interpersonal and Managerial Skills: Optimal co-existence, cultural sensitivity, gender sensitivity; capability and maturity model, decision making ability and analysis for brain storming; Group discussion and presentation skills;

UNIT 5	4 Hours

Motivation and Stress Management: Self motivation, group motivation, leadership abilities Stress clauses and stress busters to handle stress and de-stress; professional ethics, values to be practiced, standards and codes to be adopted as professional engineers in the society for various projects**.**

Note: The respective departments should discuss case studies and standards pertaining to their domain

Course Outcome:

After going through this course the students will be able to

CO1: Develop professional skill to suit the industry requirement

CO2: Analyze problems using quantitative and reasoning skills

CO3: Develop leadership and interpersonal working skills

CO4: Demonstrate verbal communication skills with appropriate body language.

References

1. Stephen R Covey, "The 7 Habits of Highly Effective People", Free Press, 2004 Edition, ISBN: 0743272455
2. Dale Carnegie, "How to win friends and influence people", General Press, 1st Edition, 2016, ISBN: 9789380914787
3. Kerry Patterson, Joseph Grenny, Ron Mcmillan, "Crucial Conversation: Tools for Talking When Stakes are High", McGraw-Hill Publication, 2012 Edition, ISBN: 9780071772204
4. Ethnus, "Aptimithra: Best Aptitude Book", Tata McGraw Hill, 2014 Edition, ISBN: 9781259058738

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in TWO Phases.

Phase	Activity	Weightage
I	After 7 weeks - Unit 1, 2 & Part of Unit 3	50%
II	After 12 weeks – Unit 3, 4, 5	50%

CIE Evaluation shall be done with weightage as follows:

Writing skills	10%
Logical Thinking	25%
Verbal Communication & Body Language	35%
Leadership and Interpersonal Skills	30%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	---	L	---	----	H	----	H	H	H	M
CO2	H	M	H	---	---	---	-----	---	M	H	M
CO3	---	---	L	---	---	H	---	H	H	H	H
CO4	---	---	H	---	----	H	L	H	H	H	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2	PSO3
CO1			
CO2			
CO3		H	H
CO4			

SECOND SEMESTER

PROJECT MANAGEMENT

Course Code	**:**	**16MEM2IP**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L: T: P: S**	**3:2:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

Students are able to

1. Understand the principles and components of project management.
2. Appreciate the integrated approach to managing projects.
3. Elaborate the processes of managing project cost and project procurements.
4. Apply the project management tools and techniques.

Unit – I **7 Hours**

Introduction: Project, Project management, relationships among portfolio management, program management, project management, and organizational project management, relationship between project management, operations management and organizational strategy, business value, role of the project manager, project management body of knowledge.

Unit – II **8 Hours**

Generation and Screening of Project Ideas: Generation of ideas, monitoring the environment, corporate appraisal, scouting for project ideas, preliminary screening, project rating index, sources of positive net present value. Project costing,

Project Scope Management: Project scope management, collect requirements define scope, create WBS, validate scope, control scope.

Organizational influences & Project life cycle: Organizational influences on project management, project state holders & governance, project team, project life cycle.

Unit – III **7 Hours**

Project Integration Management: Develop project charter, develop project management plan, direct & manage project work, monitor & control project work, perform integrated change control, close project or phase.

Project Quality management: Plan quality management, perform quality assurance, control quality.

Unit – IV **7 Hours**

Project Risk Management: Plan risk management, identify risks, perform qualitative risk analysis, perform quantitative risk analysis, plan risk resources, control risk.

Project Scheduling: Project implementation scheduling, Effective time management, Different scheduling techniques, Resources allocation method, PLM concepts. Project life cycle costing.

Unit-V **7 Hours**

Tools & Techniques of Project Management: Bar (GANTT) chart, bar chart for combined activities, logic diagrams and networks, Project evaluation and review Techniques (PERT) Planning, Computerized project management.

Syllabus includes tutorials for two hour per week:

- Case discussions on project management
- Numerical problems on PERT & CPM
- Computerized project management exercises using M S Project Software

Course Outcomes:

After going through this course the student will be able to

CO1: Explain the process of project management and its application in delivering successful projects.

CO2: Illustrate project management process groups for various project / functional applications.

CO3: Appraise various knowledge areas in the project management framework.

CO4: Develop project plans and apply techniques to monitor, review and evaluate progress for different types of projects.

Reference Books:

1. Project Management Institute, "A Guide to the Project Management Body of Knowledge (PMBOK Guide)", 5th Edition, 2013, ISBN: 978-1-935589-67-9
2. Harold Kerzner, "Project Management A System approach to Planning Scheduling & Controlling", John Wiley & Sons Inc., 11th Edition, 2013, ISBN 978-1-118-02227-6.
3. Prasanna Chandra, "Project Planning Analysis Selection Financing Implementation & Review", Tata McGraw Hill Publication, 7th Edition, 2010, ISBN 0-07-007793-2.
4. Rory Burke, "Project Management – Planning and Controlling Techniques", John Wiley & Sons, 4th Edition, 2004, ISBN: 9812-53-121-1

Scheme of Continuous Internal Evaluation (CIE)

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE)

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	----	M	H	H	H	----	H	----
CO2	----	M	----	-----	M	H	H	H	L	H	----
CO3	---	M	H	---	M	H	H	H	H	H	M
CO4	M	H	M	L	H	H	H	H	----	H	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2	PSO3
CO1			
CO2		L	
CO3			M
CO4	M		M

ANALOG IC DESIGN (Theory & Practice)					
Course Code	**:**	**16MVE22**	**CIE Marks**	**:**	**100+50**
Hrs/Week	**:**	**L:T:P:S:4:0:2:0**	**SEE Marks**	**:**	**100+50**
Credits	**:**	**5**	**SEE Duration**	**:**	**3 Hrs + 3Hrs**

Course Learning Objectives (CLOs):

Student shall be able to

1. Understand basic amplifiers, differential pair and its offsets and common-mode rejection.
2. Estimate dominant pole frequencies using pole splitting Miller effect. Extend the concepts to understand the frequency response of operational amplifiers.
3. Identify circuit noise sources from devices and handle noise power spectral density
4. Design high-performance opamps with high slew rates and understand other variations and evaluate the different performance parameters of analog systems like BGR, PLL.

Unit – I	**10 Hrs**

MOS transistors: Components available in a CMOS process, MOS small signal models, concept of $f_{T,}$ noise model.

Single stage Amplifiers: Basic concepts, dc analysis, small signal analysis and noise analysis of common source and common gate stage, power, bandwidth, impedance and frequency scaling of circuits, Frequency response of CS amplifier, Cascode stage- Folded Cascode.

Current Mirror: Basic Current Mirrors, Cascode current Mirrors, amplifiers biased at constant currents.

Unit – II	**10 Hrs**

Differential Amplifiers: Single ended and differential operation, Common mode response, differential pair with active loads, Gilbert cell

Operational Amplifier: One stage op-amp, two stage op-amp, Telescopic Cascode opamp, Telescopic Cascode opamp frequency response, Folded Cascode opamp-dc gain, Telescopic and folded Cascode opamp-noise, mismatch, slew rate, Two stage opamp-topology, frequency response, gain boosting, common mode feedback.

Unit – III	**10 Hrs**

Noise: Resistors, MOSFET, Input and output referred noise, noise scaling, basic amplifier stages – CS and CG stage

Feedback: Non-idealities- finite dc gain, effect of additional poles & zeros, feedback topologies, sense and return mechanisms, effect of loading, effect of feedback on noise, feedback circuit analysis using return ratio – closed loop gain and impedance using return ratio

Unit – IV	**10 Hrs**

Stability analysis and Frequency compensation: Stability of Feedback: Basic Concepts, Instability and the Nyquist Criterion. Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation

Band gap reference: Band gap reference, Constant current and constant gm bias generators, reducing supply sensitivity

Low dropout regulators: Basic requirements and constraints

Unit – V	**10 Hrs**

Phase Locked Loops : Simple Phase locked loop, Charge pump PLL, Non-ideal effects - Jitter & Phase noise, Applications

Analog Layout techniques: General layout considerations – design rules, antenna effect, layout techniques for multi finger transistors, symmetry, reference distribution, passive devices, interconnects, Electro static discharge (ESD) protection, substrate coupling

Lab Component

1. Study of DC and small signal models of a MOS Transistor
2. Design of MOS current sources and mirrors
3. Design of single stage amplifiers (CS, CG and CD)
4. Design of a MOS Differential amplifier with an active load
5. Design of a cascode amplifier with current mirror
6. Post-layout simulation of MOS current mirrors
7. Post-layout simulation of single stage amplifiers
8. Post-layout simulation of Differential amplifiers
9. Analysis and design of a 2-stage CMOS Op-Amp

Expected Course Outcomes:

After going through this course the student will be able to:

CO1: Investigate device, circuit & system aspects of analog IC design

CO2: Analyze the functionality of analog circuits & systems

CO3: Design and implement analog integrated circuits & systems

CO4: Evaluate the different performance parameters of analog integrated circuits & systems using CAD tools.

Reference Books:

1.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Mc GrawHill Edition, 2002, ISBN: 0-07-238032-2
2.	R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout and Simulation", IEEE Press, 2002, ISBN: 81-203-1682-7
3.	Gray, Hurst, Lewis, and Meyer: "Analysis and design of Analog Integrated Circuits", (4/e), John Wiley & Sons, *ISBN*-10: 0470245999
4.	Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", (2/e) Oxford University Press, February 2002, *ISBN*: 9780199765072
5.	David Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons, Inc.,1997, *ISBN*-10: 0470770104

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Continuous Internal Evaluation (CIE) for Practical

CIE for the practical courses will be based on the performance of the student in the laboratory, every week. The laboratory records will be evaluated for 40 marks. One test will be conducted for 10 marks. The total marks for CIE (Practical) will be for 50 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Practical

SEE for the practical courses will be based on conducting the experiments and proper results for 40 marks and 10 marks for viva-voce. The total marks for SEE (Practical) will be 50 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H										
CO2	H	H		M	H				M		
CO3	H	H	H	H	H			M	M	M	
CO4	H		H		H				M		M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	H
CO2	H	M
CO3	M	M
CO4	H	H

CAD TOOLS FOR VLSI					
Course Code	**:**	**16MVE231**	**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S:4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**	**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

Graduate shall be able to

1. Understand the concept of digital systems, how they can be optimized for area, power and cost, why it is advantageous to use physical design tools.
2. Implement the concept of the physical design cycle and develop algorithms (tools)for each design cycle step and optimize the digital system at architectural level.
3. Synthesize a given system starting with problem requirements, identifying and designing the building blocks, and then integrating blocks designed earlier
4. Develop their own platform (tool) for specific application.

Unit – I	**10 Hrs**

High Level Synthesis: Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations. **VLSI Simulation:** Gate-level modelling and simulation - Switch-level modelling and simulation - Combinational Logic Synthesis - Binary Decision Diagram.

Unit – II	**10 Hrs**

Data Structure and Basic Algorithms : Basic Terminology, Graph Search Algorithms Computational Geometry Algorithms.

VLSI partitioning& floor planning: Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms. Problem formulation, classification, Constraint based, Integer programming based, rectangular dualization, simulated evolution floor planning algorithms.

Unit – III	**10 Hrs**

Placement and Routing : Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms. **Global Routing :**Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path based Algorithms, Steiner tree based Algorithms **Detailed Routing:** Problem formulation, Classification single Layer routing, General river routing, Single row routing.

Unit – IV	**10 Hrs**

Clock and Power Routing : Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms. **Compaction:** Classification of Compaction Algorithms, One-Dimensional &Two-Dimensional Compaction, Hierarchical Compaction.

Unit – V	**10 Hrs**

Genetic algorithm and its application in VLSI physical design: Terminologies – Simple Genetic algorithms ,steady state algorithm – Genetic operators-types of GA-Genetic algorithms vs Conventional algorithms – GA example – GA for VLSI design. Genetic algorithm in partioning , placement and routing.

Expected Course Outcomes:	
After taking up this course, the graduate will be able to: CO1. Analyse each stage of VLSI design flow. CO2. Apply design knowledge to develop algorithms for VLSI design automation. CO3. Investigate the algorithms for optimizing VLSI design with respect to speed, power and area. CO4. Design an optimized VLSI cell using various algorithms.	
Reference Books:	
1.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 1998, ISBN: 978-0-471-98489-4
2.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002, ISBN: 0-7923-8393-1
3.	Pinaki mazumder and Elizabeth M Rudnick, "Genetic algorithms for VLSI design layout and test automation", Pearson Edition, 2011.

Scheme of Continuous Internal Evaluation (CIE) for Theory

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Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	H	L						
CO2	H	M	H	M	H	L				L	
CO3	H	H	H	H	H			M	L		M
CO4	H	H	H	H	H	L		M	L	L	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	H
CO2	H	M
CO3	M	M
CO4	H	M

REAL TIME EMBEDDED SYSTEMS						
Course Code	**:**	**16MVE232**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

Graduate shall be able to

1. Understand functional differences between different real time systems.
2. Examine and evaluate the hardware functionality required by embedded system to achieve real-time operation.
3. Analyse, evaluate and implement task control and real-time scheduling algorithms required to perform multitasking.
4. Demonstrate the concept of real-time programming using tasks and gain knowledge and skills necessary to design and develop embedded applications by means of real-time operating systems.

Unit – I	**10Hrs**

Introduction

Overview, Architecture Real Time Systems, Real Time Services, Real Time Standards,

System Resources

Resource Analysis, Real Time Service Utility, Cyclic Executives

Basics of RTOS

Kernel Features, Real-time Kernels: Polled Loops System, Co-routines, Interrupt-driven System, Multi-rate System; Processes, Threads, Tasks, States, Context Switching: Cooperative Multi-tasking, Pre-emptive Multi-tasking

Unit – II	**10Hrs**

Processing

Scheduling Classes, Scheduler Concepts, Pre-emptive Fixed Priority Policy, Feasibility, Rate Monotonic LUB, Necessary & Sufficient Feasibility, Dead Line Monotonic, Dynamic Priority Policies

I/O Resources

WCET, Intermediate I/O, Execution Efficiency

Memory

Physical Hierarchy, Cache, Set Associative & Direct Mapping Cache, Memory Planning, ECC Memory

Unit – III	**10Hrs**

RTOS Services

Task Creation, Inter Task Communication: Pipes, Message Queues, Mail Box, Memory Mapped Objects; Critical Section, Shared Data Problem, Synchronization: Signals, Semaphores Mutex; Remote Procedure and Sockets, Real Time Memory Management: Process Stack Management, Dynamic Allocation

Unit – IV	**10Hrs**

Timer & Timer Services
Real Time Clocks & System Clocks, Programmable Interval Timers, Timer Interrupt Service Routine, Soft-timer Handling, Soft Timers elated
Task Synchronization Issues
Resource Classification, Racing, Deadlock, Live lock, Starvation, Priority Inversion, Priority Ceiling & Inheritance,

Unit – V	**10 rs**

Examples of Real Time OS
Vx-Works, RT-Linux, RTX-ARM: Task Management, Scheduling, Primitive Kernel Services, Application Program development using APIs

Expected Course Outcomes:

After going through this course the student will be able to:

CO1. Understand the fundamental concepts of real-time system and real time operating system.
CO2. Analyse given requirements & design hardware & software of real time systems.
CO3. Apply modern engineering tools for real time firmware development & performance analysis.
CO4. Verify the specifications of various real time operating systems used for meeting timing constraints of given problem.

Reference Books:

1.	Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007, *ISBN:* 9788131502532
2.	Krishna CM and Kang Singh G, "Real time systems", Tata McGraw Hill, 2003, ISBN: 0-07-114243-64
3.	Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems", CMP Books, 2003, ISBN:1578201241
4.	Jane W. S. Liu, "Real Time Systems",Prentice Hall, 2000, ISBN:0130996513

Scheme of Continuous Internal Evaluation (CIE) for Theory
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Scheme of Semester End Examination (SEE) for Theory
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Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H										
CO2	M	H	H	H							
CO3	H	H	M	H	H		M	M	H	M	
CO4				L				M	H	M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	M
CO2	H	H
CO3	M	M
CO4	H	H

LOW POWER VLSI DESIGN						
Course Code	**:**	**16MVE241**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S:**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

The Graduate shall be able to

1. Explain the need for low power VLSI chips, Sources of power dissipation and the emerging Low power approaches.
2. Analyze the impact of Device Technology (Physics of power dissipation in CMOS devices) on device Power consumption.
3. Use simulation based power analysis techniques, probabilistic based power analysis techniques to evaluate at power at various levels of abstraction.
4. Apply circuit level techniques, logic level techniques, Algorithm & Architectural Level Methodologies to optimize the power dissipation of the system designs such as low power SRAM, CPUs, etc.
5. Design and implement the power aware clock distribution system for the system under design.

Unit – I	**10 Hrs**

Introduction and Algorithm Level Low power Methods:

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Algorithm Level low power Methods: Introduction, design flow, Algorithmic level analysis & optimization.

Unit – II	**10 Hrs**

Device & Technology Impact on Low Power:

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Unit – III	**10 Hrs**

Power estimation methods

Simulation Power analysis:

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis:

Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Unit – IV	**10 Hrs**

Low Power Design at Circuit level and Logic Level:

Low Power Design at Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.

Low Power Design at Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Unit – V	**10 Hrs**

Low power Design at Architecture/System Level and Clock distribution:

Low power Architecture & Systems: Architectural level estimation & synthesis, Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

Course Outcomes:

After going through this course the student will be able to:

CO1: Apply the knowledge of the device physics, principles of analysis tools, circuits levels, logic levels and clock distribution techniques for low power designs.

CO2: Identify, formulate, and solve engineering system design problems using low power VLSI design approaches and engineering tools.

CO3: Use the techniques and skills in system designing through modern engineering tools such as logic works SPICE and description languages such as VHDL and Verilog.

CO4: Design digital systems, components or processes to meet desired low power needs within realistic constraints and create a research oriented platform in thrust areas such as Energy recovery, Quantum computation, Adiabatic computation, etc.

Reference Books:

1.	Jan M. Rabaey and MassoudPedram, "Low Power Design Methodologies" Kluwer Academic Publishers, 5th reprint, ISBN 978-1-46 13-5975-3, 2002.
2.	Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, ISBN 978-1-4613-7778-8, 2002.
3.	Kaushik Roy and Sharat Prasad, "Low-Power CMOS VLSI Circuit Design", John Wiley, 2000. ISBN 13 9788126520237
4.	A. P. Chandraksan& R. W. Broderson: "Low power digital CMOS design", KAP, 1996, *ISBN:* 978-0-7803-3429-8

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Scheme of Semester End Examination (SEE) for Theory

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Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	L	M	M	L	H	L	L	L		M	L
CO2	M	L	L	L	M	L	M			M	L
CO3	H	H	H	H	H	M	L	L	M	H	M

CO4	H	L	H	H	H	M	M		L	H	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	M
CO2	H	H
CO3	M	M
CO4	M	H

ADVANCED EMBEDDED PROGRAMMING						
Course Code	**:**	**16MVE242**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

Graduate shall be able to

1. Understand the difference between embedded C & ANSI C.
2. Analyse & identify the complexity of given algorithm.
3. Demonstrate the use of standard data structures using relevant applications.
4. Analyse the advanced features and limits of the compilers to generate optimized program.
5. Understand different methods of optimization applicable to embedded system design & development.

Unit – I **10 Hrs**

Recap of basic C concepts, C pre-processing, Macros, compilation, Conditional Compilation, linking, Locator, makefiles, advanced pointer concepts and operations, Recursive Functions, Re-entrant Functions, Function pointers, bitwise operations, structures, Structure Padding, unions, Bit fields, type casting, aliasing, Dynamic memory allocation, Storage classes, Volatile Pointers

Unit – II **10 Hrs**

Asymptotic Notation

Introduction, Asymptotic Notation, Asymptotic Matematics, Complexity Analysis, Practical Complexities.

Data Structures-I

Data sorting, Arrays, Singly linked list &Doubly linked list, Circular list and Header Nodes.

Unit – III **10 Hrs**

Data Structures-II

Stacks & Queues using linked list, Binary Trees, Binary Search Trees, Hashing, Priority Queues, CRC Checksums.

Unit – IV **10 Hrs**

Intrinsic Functions, Inline Assembler, Embedded Assembler, Profiling and optimization of C programs, defensive programming for C, debugging C programs, linting and static code checking, C portability issues in embedded systems.

Unit – V **10 Hrs**

Embedded C Application Developmenton Cortex M3/M4

Writing Interrupt Service Routines, Writing LCD drives, Writing LED drivers, writing device driver for serial port communication, I2C interfacing with serial EEPROM using special ISRs,Writing Device Driver for DMA Transfer, Driver for Real Time Signal Interfacing**.**

Expected Course Outcomes:

After going through this course the student will be able to:

CO1. Explain the basic constructs of embedded programming.
CO2. Select & realize suitable data structures to meet given constraints.
CO3. Analyse the complexity of an application & apply optimization to meet the constraints specified & real time performance.

CO4. Formulate, design, implement, demonstrate & analyze an application realized on Cortex M3/M4 architecture.	
Reference Books:	
1.	K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009, ISBN: 10: 0070678790
2.	Seymour Lipschutz,"Data Structures With C", Shaum's Series,Tata McGraw Hill, ISBN13: 9780070701984
3.	Sartaj Sahni, "Data Structures, Algorithms and Applications in C++", McGraw Hill, 2000, ISBN: 10: 007236226X.
4.	Technical reference manuals & application development notes of Cortex M3/M4**.**

Scheme of Continuous Internal Evaluation (CIE) for Theory

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Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	M										
CO2	H	H	M	M							
CO3	H	H	H	H	H						
CO4	M	M	M	M	H		M	M	H	H	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	H
CO2	H	H
CO3	M	M
CO4	M	H

HIGH SPEED VLSI DESIGN

Course Code	**:**	**16MVE251**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

Graduate shall be able to

1. Understand analog circuit principles relevant to high speed digital design.
2. Analyze power distribution and noise in Power supply network and signaling over transmission lines.
3. Demonstrate the functionality of different clocked and non clocked digital circuits and memory elements.
4. Analyze the performance of clocked, non clocked and latching circuits.

Unit – I **10 Hrs**

Introduction to high speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

Unit – II **10 Hrs**

Power distribution and Noise: Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference. Power distribution on chips.

Unit – III **10 Hrs**

Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

Unit – IV **10 Hrs**

Clocked & non clocked Logics:

Non clocked Logic Styles: Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families

Clocked Logic Styles:Single-Rail Domino Logic, Dual-Rail Domino Structures

Unit – V **10 Hrs**

Latching Strategies:

Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques, DDR memories.

Expected Course Outcomes:

After taking up this course, the graduate will be able to:

CO1: Analyse the special requirements that are imposed on high speed digital design.

CO2: Analyze the characteristics of transmission lines, Power supply network and Noise sources in digital systems.

CO3: Apply different Clocked & non clocked digital Logics in designs

CO4: Evaluate the performance of various transmission lines and digital circuits.	
Reference Books:	
1.	William S. Dally & John W. Poulton, "Digital Systems Engineering", Cambridge University Press, 1998. ISBN 0-521-59292-5
2.	Kerry Bernstein, Keith M. Carrig, Christopher M. Durham, Patrick R. Hansen, David Hogenmiller, Edward J. Nowak, Norman J. Rohrer., "High Speed CMOS Design Styles", Kluwer Academic Publishers in 1999, ISBN 978-1-4613-7549-4.
3.	Masakazu Shoji, "High Speed Digital Circuits", Addison Wesley Publishing Company, 1996. *ISBN* 978-0201634839.
4.	Howard Johnson & Martin Graham, "High Speed Digital Design" A Handbook of Black Magic, Prentice Hall PTR, 1993.
5.	Jan M.Rabaey, Anantha Chadrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", (2/e), Pearson 2016, ISBN-13: 978-0130909961.

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Scheme of Semester End Examination (SEE) for Theory

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit. The total marks for SEE (Theory) will be 100 marks.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	M	M	M	M	L	L	M	M	M	L	M
CO2	M	M	M	H	L	L	M	M	M	L	M
CO3	M	M	M	H	M	L	M	M	M	L	M
CO4	M	M	H	H	M	L	M	M	M	L	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	H
CO2	H	M
CO3	M	M
CO4	M	H

MEMS AND SMART SYSTEMS						
Course Code	**:**	**16MVE252**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

Graduate shall be able to

1. Apply concepts of a micro- and smart systems into a real device considering the scaling laws and boundary conditions involved.
2. Integrate the knowledge of semiconductors and solid mechanics to fabricate MEMS devices.
3. Design the micro devices, micro systems using the MEMS fabrication process
4. Interpret the concepts involved in the design of microfluidic systems

Unit – I **10 Hrs**

Introduction to MEMS and principle of operation.

Introduction, History of evolution, Definition of MEMS in a broader sense. Components of a smart system. Commercial products. Microsystems and Miniaturization. Evolution of micro-manufacturing. Design Aspects. Application and future scope of MEMS devices, Market trends.

Definitions and salient features of sensors, actuators and systems. Working principles of Microsystems.Sensors: silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, Actuators: silicon micro-mirror arrays, piezo-electric based inkjet printhead, electrostatic comb-drive and micromotor, magnetic micro relay.

Unit – II **10 Hrs**

Micro and Smart Devices and Systems: Materials and Processing

Materials

Introduction, Substrates and Wafers, Active substrate materials, Si as a substrate material, Si compounds, Si Piezoresistors, Gallium Arsenide, Quartz, Piezoelectric Crystals and Polymers.

Processing

Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization, Silicon micromachining: surface and bulk, bonding based process flows. Thick-film processing: Smart material processing, Emerging trends.

Unit – III **10 Hrs**

Mechanical modelling and Scaling laws in Microsystems Modelling

Simplest deformable element: a bar, Transversely deformable element: a beam, Bimorph effect, Mechanical vibration: general formulation, Resonant Vibration, Design theory of accelerometers and damping coefficients. Basics of fluid mechanics in macro and mesoscales, Capillary effect, electro-phoresis and Dielectrophoresis.

Scaling laws in Miniaturization

Importance of scaling in MEMS- Scaling in geometry, Scaling in rigid body dynamics, scaling in electrostatic forces, scaling in electromagnetic forces, scaling in electricity, scaling in fluid dynamics. scaling effects in the optical domain, scaling in biochemical phenomena.

Unit – IV **10 Hrs**

RF MEMS

Introduction to RF MEMS, Static Analysis of RF MEMS devices: Spring Constant of Low-k Beams, Spring Constant of Cantilever Beams, Spring Constant of Circular Diaphragms, Beam Curvature due to Stress Gradients. Electrostatic Actuation, Shape of the Deformed Beam Under Electrostatic Actuation, DC Hold-Down Voltage of MEMS Beams and Cantilevers, Forces on MEMS Beams, Self-Actuation of MEMS Capacitive Switches, RF Hold-Down Voltage of MEMS Capacitive Switches.

Unit – V	**10 Hrs**

Case study of devices: Pressure sensors, accelerometers, micro pump, micro heater. Introduction to CAD tool for simulation of devices.

Packaging : Integration of Microsystems and microelectronics, Packaging Introduction, Micro Systems Packaging, Objectives, Issues in packaging, Special issues in micro system packaging, Types of Microsystem Packages, Packaging Technologies.

Expected Course Outcomes:

After going through this course the student will be able to:

CO1 :Explain the technology to fabricate advanced micro- and smart systems
CO2: Analyse different methods to fabricate MEMS devices.
CO3: Apply the basics of implementation of MEMS into products.
CO4: Discuss and anlyze principles and processes involved in the implementation of MEMS devices.

Reference Books:

1.	Dr. A.K.Aatre, Ananth Suresh, K.J.Vinoy, S. Gopala krishna, K.N.Bhat., "Micro and Smart Systems", John Wiley Publications, 2002, ISBN: 1118213904, 9781118213902
2.	Tai-Ran Tsu, "MEMS & Microsystems: Design and Manufacture", Tata Mc-Graw-Hill.2002.8th reprint, ISBN-13:978-0-07-048709-3. ISBN-10:0-07-048709-X
3.	RF MEMS Theory, Design and Technology GABRIEL M. REBEIZ. 2003A JOHN WILEY & SONS PUBLICATION. ISBN: 978-0-471-20169-4
4.	S. D. Senturia, "Microsystems Design", Kluwer Academic Publishers, Boston, USA, 2001, ISBN 0-7923-7246-8

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Mapping of Course Outcomes (CO) to Program Outcomes (PO)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	L	H		H					

CO2	M	L	L		M	H					
CO3					M	M	H			H	
CO4		L	H	H							

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	**PSO2**
CO1	H	H
CO2	H	M
CO3	M	M
CO4	M	H

MINOR PROJECT						
Course Code	**:**	**16MDC26**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**0:0:10:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**05**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

Students are able to

1. Understand the method of applying engineering knowledge to solve specific problems.
2. Apply engineering and management principles while executing the project
3. Demonstrate the skills for good presentation and technical report writing skills.
4. Identify and solve complex engineering problems using professionally prescribed standards.

GUIDELINES

1. Each project group will consist of maximum of two students.
2. Each student / group has to select a contemporary topic that will use the technical knowledge of their program of study after intensive literature survey.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The number of projects that a faculty can guide would be limited to four.
5. The minor project would be performed in-house.
6. The implementation of the project must be preferably carried out using the resources available in the department/college.

Course Outcomes:

After going through this course the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.

CO2: Communicate the solutions through presentations and technical reports.

CO3: Apply resource managements skills for projects

CO4: Synthesize self-learning, team work and ethics.

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in THREE Phases. The evaluation committee will comprise of FOUR members : guide, two senior faculty members and Head of the Department.

Phase	Activity	Weightage
I	Synopsis submission, Preliminary seminar for the approval of selected topic and Objectives formulation	20%
II	Mid-term seminar to review the progress of the work and documentation	40%
III	Oral presentation, demonstration and submission of project report	40%

****Phase wise rubrics to be prepared by the respective departments**

CIE Evaluation shall be done with weightage / distribution as follows:

- Selection of the topic & formulation of objectives 10%
- Design and simulation/ algorithm development/experimental setup 25%
- Conducting experiments / implementation / testing 25%
- Demonstration & Presentation 15%
- Report writing 25%

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

1. Brief write-up about the project 5%
2. Presentation / Demonstration of the project 20%
3. Methodology and Experimental Results & Discussion 25%
4. Report 20%
5. Viva Voce 30%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	M	M	H	H	H	---	---	M	---	H	H
CO2	----	---	----	---	H	----	---	H	H	H	----
CO3	H	H	M	---	M	M	H	H	---	M	H
CO4	---	H	----	---	----	H	M	M	M	H	---

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1		
CO2		
CO3		
CO4		

THIRD SEMESTER

SystemVerilog for Design and Verification of Digital Systems						
Course Code	**:**	**16MVE31**		**CIE Marks**	**:**	**100 +50**
Hrs/Week	**:**	**L:T:P:S:3:0:1:0**		**SEE Marks**	**:**	**100 +50**
Credits	**:**	**5**		**SEE Duration**	**:**	**3 Hrs +3Hrs**

Course Prerequisites:

The graduate is expected to possess the following pre-requisites

1. Concept of digital system design.
2. Concept of system design using Verilog.

Course Learning Objectives (CLO):

At the end of the course the student should be able to:

5. Write efficient SystemVerilog reference models for system design and verification.
6. Understand the important new SystemVerilog data types and capabilities; new SystemVerilog RTL and abstraction capabilities
7. Write complex self-checking testbenches - includes the use of new SystemVerilog Hardware Verification Language (HVL)capabilities.
8. Understand the object-oriented stimulus generation using classes, constrained random stimulus generation and functional coverage capabilities.
9. Write efficient synthesizable SystemVerilog RTL models - includes new SystemVerilog data types and capabilities, RTL and abstraction capabilities.
10. Gain the knowledge of complete digital system design and verification using SystemVerilog to be an industry ready engineer.

Unit – I	**10 Hrs**

Introduction to SystemVerilog:

SystemVerilog standards, Key SystemVerilog enhancements for hardware design.Advantages of System Verilog over Verilog, Data Types: Verilog data types, System Verilog data types, 2 - State Data types, Bit, byte, shortint, int, longint. 4 - State data types. Logic, Enumerated data types, User Defined data types, Struct data types, Strings, Packages, Type Conversion: Dynamic casting, Static Casting, Memories: Arrays, Dynamic Arrays, Multidimensional Arrays, Packed Arrays, Associative Arrays, Queues, Array Methods, Tasks and Functions: Verilog Tasks and Functions, Enhancements in S.V, Void Functions, Return Statement, Passing Arguments, Arguments Passing by Name, Default Arguments, Passing Arguments by Value, Passing Arguments by Reference.

Unit – II	**10 Hrs**

Connecting the Testbench and Design:

Verilog interface signals - Limitations of Verilog interface signals, SystemVerilog interfaces, SystemVerilog port connections, Interface instantiation 2.4. Interfaces Arguments, Interface Modports, Interface References, Tasks and functions in interface, Verilog Event Scheduler, SystemVerilog Event Scheduler, Clocking Block, Input and Output Skews, Typical Testbench Environment, Verification plan

Unit – III	10 Hrs

OOPs Basics and Advanced OOPs concepts:

Basic OOP Concepts

Overview of Classes, Properties and Methods in the Classes, Instance/Object Creation, New Constructor, Null Object handles, Accessing Members, this Keyword, Creating an Object, Objects Assignments, Copying an Object: Shallow Copy, Deep Copy

Advanced OOP Concepts

Inheritance: Concept of Inheritance, Super Keyword, Static properties**,** Overriding Methods**,** Polymorphism - $cast**,** Virtual Classes**,** Parameterized Classes

Unit – IV	10 Hrs

Constrained Randomization, Threads and Inter-process Communication:

Constrained Randomization

Random Variables - rand and randc, Randomize( ) Method - Pre/Post Randomize( ) methods, Constraints in the class, Rand_mode and constraint_mode, Constraint and Inheritance, Constraint Overriding, Set Membership, Distribution Constraints, Conditional Constraints - .implication (->), . if/else, Inline Constraints

Threads and Inter-process Communication

Threads, Fork-Join/Join_any/Join_none, Communication – Mailbox, Semaphore, Events, BuildingaTestbenchwithThreadsandIPC

Unit – V	10 Hrs

Functional Coverage andAssertion Based Verification:

Functional Coverage

Coverage Definition, Code Coverage, Functional Coverage: Cover Group, Creating Cover Group Instances, Coverpoints, Bins - . implicit bins, . Explicit bins, Bin creation, Vector and Scalar bins, Cross products, Intersect, Select Expressions, Conditional Expression (iff), Illegal bins, Ignore bins, Coverage Analysis, Covergroup Built-in Methods - . Sample(), . get_coverage(), .get_instance_coverage(), .set_instance_name(string), .start(), . stop()

Assertion Based Verification

Introduction, Types of Assertions - . Immediate, . Concurrent, Assertion Properties- . Writing Properties, Sequences- . Sequence Composition, . and, or, intersect, Advanced SVA Features - . Expect, Binding, Assertion Coverage

Laboratory exercises:

1. Data Types, Interfaces and OOPs

Experiments to understand the usage of

(a) the SystemVerilog data types such as associative arrays and interfaces constructs

(b) the OOP basics such as class, assignment handling, deep copy, inheritance, virtual functions (polymorphism)

2. Randomization, Threads, Mailbox and Semaphores

Experiments to understand the usage of

(a) the SystemVerilog Random variables and constraints

(b) the SystemVerilog threads, mailbox and Semaphores

3. Transactions and Transactors

Experiments to understand the usage of

(a) the SystemVerilog transaction and create transaction

(b) the SystemVerilog Transactors such as generator, driver, monitor, and reference models

4. Scoreboard

Experiments to understand the usage of Scoreboard

5. Environment

Experiments to understand the usage of Environment

Expected Course Outcomes:

After taking up this course, the graduate will be able to:

CO1: Demonstrate the use SystemVerilog data types for digital system design and functional verification.

CO2: Demonstrate the skill on writing test-benches for design digital systemsand connecting them with the design.

CO3: Verify and Analyze the complete systems through robust verification methodsuch as assertion based verification.

CO4: Design and verify the digital systems such as FIFOs, memories, ATM interfaces, etc. using the learnt methods and demonstrate the skills.

Reference Books:

5.	Stuart Sutherland, Simon Davidmann and Peter Flake, "*SystemVerilog for Design - A Guide to Using SystemVerilog for Hardware Design and Modeling*," 2E, Springer Science, ISBN-13: 978-0387-3339-91, 2006.
6.	C Spear, "*SystemVerilog for Verification-A Guide to Learning the Testbench Language Features*," Springer Science, IEEE press, ISBN-13: 978-0387-2703-64,2006.
7.	Doulos, "*SystemVerilog golden reference guide*-A concise guide to SystemVerilog IEEE Standard-1800-2009," Version 5.0,ISBN: 0-9547345-9-9, 2012.
8.	Sasan Iman, "*Step-by-Step Functional Verification with SystemVerilog and OVM*," Hansen Brown Publishing Company,ISBN-13: 978-0-9816-5621-2, 2008.
9.	IEEE Computer Society, "*IEEE Standard for SystemVerilog-Unified Hardware Design, Specification and Verification*," IEEE Press, ISBN: 978-0-7381-6129-7, 2009

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Continuous Internal Evaluation (CIE) for Practical

CIE for the practical courses will be based on the performance of the student in the laboratory, every week. The laboratory records will be evaluated for 40 marks. One test will be conducted for 10 marks. The total marks for CIE (Practical) will be for 50 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Scheme of Semester End Examination (SEE) for Practical

SEE for the practical courses is based on conducting the experiment and proper results (for 40 marks) and viva-voce (for 10 marks). The total marks for SEE (Practical) is 50.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	H	H	H	-	M	H	-	L
CO2	H	H	H	H	H	M	L	-	H	-	H
CO3	H	H	H	H	H	H	-	L	H	M	H
CO4	H	H	H	H	H	H	L	M	H	H	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	M	H
CO2	H	M
CO3	M	H
CO4	H	H

Embedded System for Networking						
Course Code	**:**	**16MVE321**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**4:0:0:0**		**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Prerequisites :

Fundamentals of digital electronics, Embedded Processors and Computer Networks

Course Learning Objectives (CLOs):

Graduate shall be able to

5. Understand requirements of an embedded system for networking application and the issues pertaining to such embedded computing system design.
6. Illustrate how microprocessor, memory, peripheral components and buses build an embedded platform and their interaction for implementation of networking protocols.
7. Evaluate how architectural and implementation design decisions influence performance and scaling
8. Building, testing the operation of real-time IoT application protocol through hands-on experience with a single-board computer.

Unit – I	**09 Hrs**

EMBEDDED PROCESSOR FOR NETWORK PROTOCOL PROCESSING

Introduction and overview, basic terminology and example systems, review of protocols and packet format, Conventional computer hardware architecture, basic packet processing, packet processing functions, protocol software on a conventional processor, hardware architecture for protocol processing, classification and forwarding, switching fabrics, Hardware/Software Traffic management implementation.

Unit – II	**09 Hrs**

INTRODUCTION TO ADVANCED ARCHITECTURE: NETWORK PROCESSOR

Network processors, the complexity of network processor design, network processor architectural Overview and comparison of commercial network processors: the Intel network processor, RISC processor, packet processor hardware.

Unit – III	**10 Hrs**

SCALING IN NETWORK PROCESSORS

Scalability with Parallelism And Pipelining - issues in scaling a network processor- Complexity Of Network Processor Design (packet processing, ingress & egress processing, Macroscopic Data Pipelining And Heterogeneity etc) - Network Processor fun : Packet Flow, Clock Rates, software architecture, Assigning Functionality To The Processor Hierarchy

Unit – IV	**10 Hrs**

CLASSIFICATION OF NETWORK PROCESSORS

Basis in Classification of network processors- Multichip pipeline, configurable instruction set processors, packet processor, Augmented RISC Processor, Embedded Processor Plus Coprocessors- Design Tradeoff s and consequences (Programmability Vs. Processing Speed , speed vs functionality. etc)

Unit – V	**10 Hrs**

INTERNET OF THINGS

Introduction to IoT, Attributes of Processors for IoT, memory for IoT, Introduction to IoT protocols: MQTT, 6LoWPAN, Programming for IoT (C, Node.js)
Implementation of MQTT on various platforms (RASBERRY PI).

Expected Course Outcomes:

After going through this course the student will be able to:

CO1: Describe the architecture of embedded system with functional requirements for hardware and software components to realize networking applications.

CO2: Analyze the architecture of network processor to support complex data processing operations.

CO3: Design firmware for networking embedded systems by utilizing advanced hardware features.

CO4: Demonstrate an ability to read, critically evaluate, analyze and present (verbally or in written form) the content and implications of research articles in the area.

Reference Books:

5.	Douglas E. Comer ”Network System Desi gn using Network Processors” Prentice Hall , 2006.
6.	Jorgen Staunstrup, Wayne Wolf, “Harware/Software Co-Design:Principles and Practice”, Kluwer Academic Pub, 1997
7.	Patrick Crowley, M A Franklin, H Hadimioglu, PZ Onufryk, “Network Processor Design, Issues and Practices Vol – I , 2, Morgan Kauffman, E l s e v i e r 2011
8.	Deepankar Medhi , Karthikeyan Ramasamy, “Network Routing : Algorithms, Protocols, andArchitecture”, El sevier, 2007

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	H	M	M	L	L	-	M	H	-	L
CO2	H	H	M	M	L	M	-	M	H	-	M
CO3	H	H	H	H	M	H	-	H	H	-	H
CO4	H	H	H	M	M	H	-	H	H	M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	L
CO2	H	L
CO3	H	M
CO4	H	H

Radio Frequency IC Design						
Course Code	**:**	**16MVE322**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

Students shall be able to

1. Apply the knowledge of radio frequency circuits in IC design.
2. Analyze the functionality and design issues of RF circuits and systems.
3. Design and implement RF transceiver/ related circuitry
4. Evaluate the different performance parameters used in RF design.

Unit – I **10 Hrs**

Basic concepts in RF design - Nonlinearity and Time Variance, Effects of nonlinearity – harmonic distortion, gain compression, desensitization, cross modulation, intermodulation, cascaded nonlinear stages – level diagram. Noise in RF circuits – Noise figure, Noise figure of cascaded and lossy circuits, Sensitivity and dynamic range.

Unit – II **10 Hrs**

RF Systems Design - Receiver architectures - Heterodyne - dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, Image Reject – Hartley architecture, Transmitter architectures - Direct conversion and two-step transmitters.

RF Circuits Design (MOSFET circuits only)

Low noise Amplifier - Performance parameters, Problem of Input matching, LNA topologies – Variants of common source only, design examples.

Unit – III **10 Hrs**

Mixer - Mixer fundamentals, Performance parameters, Nonlinear systems as linear mixers, two port example –square law mixers, multiplier based mixers – Single balanced and double balanced (active and passive) - working and implementation, (MOSFET circuits only).

Oscillator - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, VCO characteristics, Phase noise – basic concepts and effects of phase noise (no analysis).

Unit – IV **9 Hrs**

Phase Locked Loop Design - Type-II PLL: design equations, phase margin, and closed-loop PLL response, Design methodology for a Type-II 3rd –order PLL, charge pump design issues, Charge Pump design techniques: charge-injection, clock feed-through. Current steering CP design, replica biasing, professional charge pump, Charge pump non-idealities and their mitigation: Dead zone, current mismatch, charge sharing, PLL Noise Analysis.

Unit – V **9 Hrs**

Frequency Synthesizers: General considerations, Basic Integer N synthesizer, settling behavior, spur reduction techniques, PLL based modulation, Divider design – Pulse swallow divider, dual modulus divider, divider logic styles – current steering, CML latch, true single phase clocking. Fractional N synthesizers- basic concepts only.

Expected Course Outcomes:

After going through this course the student will be able to:

1. Apply the knowledge of RF circuits & systems in IC design
2. Analyze CMOS circuits and its impact on Radio frequency IC design.
3. Design and implement RF transceiver chain with specification.

4. Evaluate the different performance parameters used in RF design using CAD tools.	
Reference Books:	
1.	Behzad Razavi, "RF Microelectronics ", 2nd Edition Pearson Education, 2012
2.	John Rogers ,Calvin Plett, "Radio Frequency Integrated Circuits Design", Artech House, 2003
3.	Thomas H Lee , "The Design of CMOS Radio Frequency Integrated Circuits",2nd Edition, Cambridge University Press, 2004
4.	Bosco Leung, "VLSI for Wireless Communications", Pearson Education, 2004

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	H	H	H	-	-	M	-	M
CO2	H	H	H	H	H	H	-	-	M	-	M
CO3	H	H	H	H	H	H	-	-	M	-	M
CO4	H	H	H	H	H	H	-	-	M	-	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1		H
CO2	H	
CO3		M
CO4	H	H

ARM PROGRAMMING AND OPTIMIZATION						
Course Code	**:**	**16MVE331**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

The student will be able to

1. Discuss the basic principles of ARM system design.
2. Identify the major hardware components ARM data path architecture.
3. Identify the design issues ARM based embedded system with the basic knowledge of firmware, embedded OS & ARM architectures.
4. Analyze the execution of instructions/program knowing the basic principles of ARM architecture and assembly language.
5. Compare programs written in C & assembly to execute on ARM platform.

Unit – I **9 Hrs**

Introduction, Data Path Architecture, Registers, Modes, Exceptions

Programming in C for ARM

Overview of C Compilers and optimization, basic C data types, C looping structures, register allocation, function calls, pointer aliasing, structure arrangement, bit fields, unaligned Data and Endianess, division, floating point, inline functions and inline assembly, portability issues.

Unit – II **9 Hrs**

Writing and Optimizing ARM Assembly Code

Writing assembly code, profiling and cycle counting, instruction scheduling, register allocation, conditional execution, looping constructs, Bit manipulation, efficient switches. Handling unaligned data.

Unit – III **10 Hrs**

Digital Signal Processing on ARM

Representing a digital signal, Introduction to DSP on the ARM, FIR filters: Realization of filters on ARM7 and Cortex M3, IIR Filters: Realization of filters on ARM7 and Cortex M3, CMSIS DSP Library.

Unit – IV **10 Hrs**

Firmware

Firmware and Boot loader

Embedded Operating Systems

Fundamental Components, Simple Operating System.

Unit – V **10 Hrs**

Memory Protection Unit

Over view of the MPU's, MPU registers, setting up the MPU, Memory barrier and memory configuration, Using sub-region disable, Consideration when using MPU, Other usages of MPU.

Expected Outcome:

On completion of the course the student will be able to:

CO1. Describe the programmer's model of ARM processor and analyse the instruction set architecture to realize complex operations.

CO2. Apply the optimization methods available for ARM architectures to design embedded software to meet given constraints with the help of modern engineering tools.

CO3. Realize real time signal processing applications & primitive OS operations on different

	ARM architectures by making use of software libraries. CO4. Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments.
Reference Books:	
1.	Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publishers, 2008, ISBN-13:9788181476463
2.	Joseph Yiu, "The definitive Guide to the ARM Cortex- M3 & M4 Processors", 3rd Edition, Newnes (Elsevier), 2014, ISBN: 978-93-5107-175-4
3.	Steve Furber, "ARM System on Chip Architecture", Pearson Education Limited,2nd Edition, ISBN-13:9780201675191
4.	Technical reference manual for ARM processor cores, including Cortex M series, ARM 11, ARM 9 & ARM 7 processor families.
5.	User guides and reference manuals for ARM software development and modeling tools.

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Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	H	H	H	-	M	H	-	L
CO2	H	M	H	M	H	M	-	M	H	-	H
CO3	H	H	H	L	H	H	-	-	H	-	H
CO4	H	H	H	L	H	H	-	-	H	L	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1		H
CO2	H	M
CO3		H
CO4	H	H

VLSI TESTING						
Course Code	**:**	**16MVE332**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

The student will be able to

1. Model and simulate different types of faults in digital circuits.
2. Establish equivalence and dominance relationships of faults in a circuit
3. Critique and compare ATPG algorithms with respect to speed, fault coverage and other criteria.
4. Comprehend the different testing diagnostic & fault simulation techniques

Unit – I	**9 Hrs**

Introduction to Testing: Role of testing VLSI circuits, VLSI trends affecting testing, Physical Faults, Stuck-at Faults, Stuck open Faults, Permanent, Intermittent and Pattern Sensitive Faults, Delay Faults.

Fault Modeling- Functional Testing, Structural Testing, Types of Fault Models, Stuck-at Faults, Bridging Faults, cross point faults, Fault Equivalence, Fault Dominance

Unit – II	**9 Hrs**

Testability Measure – Controllability, Observability, SCOAP measures for combinational and sequential circuits.

ATPG for Combinational Circuits: Path Sensitization Methods, Roth's D- Algorithm, Boolean Difference, PODEM Algorithm. Complexity of Sequential ATPG, Time Frame Expansion.

Unit – III	**10 Hrs**

Design for Testability- Ad-hoc, Structured DFT- Scan method, Scan Design Rules, Overheads of Scan Design, partial scan methods, multiple chain scan methods.

Fault Simulation- Fault Simulation algorithm- Serial, Parallel, Deductive and Concurrent Fault Simulation.

Boundary Scan Standard - TAP Controller, Test Instructions.

Unit – IV	**10 Hrs**

Self test And Test Algorithms

Built-In self-Test, test pattern generation for BIST, response compaction - Parity checking, Ones counting, Transition Count, Signature analyzer.Circular BIST,BIST Architectures.

Testable Memory Design Test Algorithms, Reduced Functional Faults-MARCH and MAT+ algorithm. Test generation for Embedded RAMs.

Unit – V	**10 Hrs**

Fault Diagnosis

Logical Level Diagnosis, Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits, Self-checking design, System Level Diagnosis.

CO1. Acquire knowledge about fault modeling & collapsing.
CO2. Analyse various combinational ATPG techniques
CO3. Evaluate the significance of sequential test pattern generation
CO4. Develop fault simulation techniques & fault diagnosis methods

Reference Books:

Reference Books:

1. Michael L.Bushnell, Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital

	Memory & Mixed Signal VLSI Circuits", Kluwer Academic Publications, 1999.
2.	MironAbramovici, Melvin A. Breuer, Arthur D. Friedman, " Digital Systems Testing and Testable Design", 3rd Edition, Jaico Publishing House, 2004
3.	Hideo Fujiwara, " Logical testing & design for testability", The MIT Press.
4.	Parag.K.Lala "Digital Circuit Testing and Testability" Academic Press.

Scheme of Continuous Internal Evaluation (CIE) for Theory

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Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	H	M	H	H	M	-	M	L	-	L
CO2	M	H	M	H	H	M	-	M	L	-	M
CO3	M	M	M	H	H	M	-	M	L	-	M
CO4	-	M	M	H	H	M	-	M	L	-	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	M
CO2	H	-
CO3	-	H
CO4	H	M

Mixed Signal IC Design						
Course Code	**:**	**16MVE341**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

Students shall be able to

1. Design Sample and Hold circuits.
2. Analyze Switched Capacitor Amplifiers and its non idealities.
3. Design various types of ADC/DAC for a given specification
4. Design oversampling converter considering all the practical issues for the given specification.

Unit – I **10 Hrs**

Sampling

Introduction, sampling, Spectral properties of sampled signals, Oversampling – Anti-alias filter design. Time Interleaved Sampling, Ping-pong Sampling System, Analysis of offset and gain errors in Time Interleaved Sample and Hold. Sampling circuits- Distortion due to switch, Charge injection, Thermal noise in sample and holds, Bottom plate sampling, Gate bootstrapped switch, Nakagome charge pump. Characterizing Sample and hold, Choice of input frequency.

Unit – II **10 Hrs**

Switched Capacitor Amplifiers

Common mode feedback (CMFB) – resistive CM detector, CMFB compensation, single-stage differential opamp. Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers, Non idealities in SC Amplifiers – Finite gain, DC offset, Gain- Bandwidth Product. Fully differential SC circuits, DC negative feedback in SC circuits. Switched-capacitor CMFB: design, analysis

Unit – III **10 Hrs**

Analog to Digital Converter

Static specifications: INL, DNL; Dynamic specifications: SNDR, DR, SFDR, linearity.

Flash ADC, Regenerative latch, Preamp offset correction, Preamp Design, necessity of up-front sample and hold for good dynamic performance.

Unit – IV **10 Hrs**

Digital to Analog Converter

Linearity errors, DAC spectra and pulse shapes. NRZ vs RZ DACs. DAC Architectures: Binary weighted, Thermometer DAC, Current steering DAC – Current cell design in current steering DAC, Charge Scaling DAC

Unit – V **10 Hrs**

Oversampling Converter

Benefits of Oversampling, Oversampling with Noise Shaping, Signal and Noise Transfer Functions, First and Second Order Delta-Sigma Converters. Signal Dependent Stability of Describing Function Method. Introduction to Continuous-time Delta Sigma Modulators, time-scaling, inherent anti-aliasing property, Excess Loop Delay, Time-constant changes, Influence of Op amp nonidealities.

Expected Course Outcomes:

After going through this course the student will be able to:

1. Design Sample and Hold circuits.
2. Analyze Switched Capacitor Amplifiers and its non idealities.
3. Design various types of ADC/DAC for a given specification
4. Evaluate the different performance parameters of ADC/ DAC

Reference Books:	
6.	M. Gustavsson, J. Wikner, and N. Tan, "CMOS Data Converters for Communication" Kluwer Academic Publishers, 2000.
7.	Behzad Razavi, "Principles of Data Conversion System Design" Wiley-IEEE Press, 1994
8.	David A.Johns, Ken Martin, "Analog Integrated Circuit Design" John Wiley & Sons Inc. 1997
9.	R.Jacob Baker, "CMOS Mixed Signal Circuit Design", IEEE Press Series on Microelectronic Systems, 2002.

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Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**
CO1	H	M	M	H	H	H	-	-	M	-	M
CO2	H	H	H	H	H	H	-	-	M	-	M
CO3	H	H	H	H	H	H	-	-	M	-	M
CO4	H	H	H	H	H	H	-	-	M	-	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	**PSO2**
CO1	M	H
CO2	H	M
CO3	M	H
CO4	H	H

Synthesis and Optimization of Digital Circuits						
'Course Code	**:**	16MVE342		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

1. Analyse different levels of abstraction and different types of algorithms for VLSI functional models
2. Draw data flow and sequencing graphs for different types of VLSI models and use compilation and optimization techniques
3. Optimize Sequential circuit using state based models, and using network models
4. Schedule VLSI models with and without resource constraints using different algorithm
5. Analyze simulators for fault, Automatic test pattern generation (ATPG), design for Testability (DFT) Techniques

Unit – I	**9 Hrs**

Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Unit – II	**9 Hrs**

Schedule Algorithms: A model for scheduling problems, Scheduling wither source and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, dataflow and sequencing graphs, compilation and optimization techniques.

Unit – III	**10 Hrs**

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Unit – IV	**10 Hrs**

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Unit – V	**10 Hrs**

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table FPGAs and Anti fuse based FPGAs), rule based library binding.

Expected Course Outcomes:

After going through this course the student will be able to:

1. Understand and apply the various algorithms and graphs to synthesis and optimization of different digital circuit.
2. Analyze the performance of standard algorithm used for synthesis and optimization of two level, multiple level and sequential logic circuits
3. Demonstrate the improvement of optimization techniques used for digital circuits
4. Develop an algorithm for synthesis and optimization

Reference Books:

1.	Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.
2.	SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer, "Logic Synthesis", McGraw-Hill, USA, 1994.
3.	NeilWeste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", 2nd edition, Pearson Education (Asia) Pte.Ltd., 2000.

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	M	H	H	-	M	H	-	L
CO2	H	H	H	M	H	M	-	M	H	-	H
CO3	H	H	H	M	H	H	-	-	H	-	H
CO4	H	H	H	M	H	H	-	-	H	-	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	M	H
CO2	H	M
CO3	M	H
CO4	H	H

INTERNSHIP / INDUSTRIAL TRAINING						
Course Code	**:**	**16MVE35**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**0:0:6:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**3**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES FOR INTERNSHIP

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the process of applying engineering knowledge to produce product and provide services.

(2) Explain the importance of management and resource utilization

(3) Comprehend the importance of team work, protection of environment and sustainable solutions.

(4) Imbibe values, professional ethics for lifelong learning.

1) The duration of the internship shall be for a period of 8 weeks on full time basis between II semester final exams and beginning of III semester.
2) The student must submit letters from the industry clearly specifying his / her name and the duration of the internship on the company letter head with authorized signature.
3) Internship must be related to the field of specialization or the M.Tech program in which the student has enrolled.
4) Students undergoing internship training are advised to use ICT tools such as skype to report their progress and submission of periodic progress reports to the faculty members.
5) Every student has to write and submit his/her own internship report to the designated faculty.
6) Students have to make a presentation on their internship activities in front of the departmental committee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the internship final report. However interim or periodic reports and reports as required by the industry / organization can be submitted as per the format acceptable to the respective industry /organizations.
7) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
8) The broad format of the internship final report shall be as follows
    - Cover Page
    - Certificate from College
    - Certificate from Industry / Organization
    - Acknowledgement
    - Synopsis
    - Table of Contents
    - Chapter 1 - Profile of the Organization – Organizational structure, Products, Services, Business Partners, Financials, Manpower, Societal Concerns, Professional Practices,
    - Chapter 2 - Activities of the Department -

- Chapter 3 – Tasks Performed – summaries the tasks performed during 8 week period
- Chapter 4 – Reflections – Highlight specific technical and soft skills that you acquired during internship
- References & Annexure

Course Outcomes:

After going through the internship the student will be able to:

CO1: Apply engineering and management principles

CO2: Analyze real-time problems and suggest alternate solutions

CO3: Communicate effectively and work in teams

CO4: Imbibe the practice of professional ethics and need for lifelong learning.

Scheme of Continuous Internal Evaluation (CIE):

A committee comprising of the Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation of the application of engineering knowledge in industries 35%

(2) Ability to comprehend the functioning of the organization/ departments 20%

(3) Importance of resource management, environment and sustainability 25%

(4) Presentation Skills and Report 20%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		M	H	M		M				L	
CO2				H	M	M		L			
CO3					L		M	H	H		
CO4					L		H			M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	
CO2	L	L
CO3		M
CO4	M	H

GUIDELINES FOR INDUSTRIAL TRAINING

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the process of applying engineering knowledge to industrial products & processes

(2) Explain the importance of skilling, training and resource management.

(3) Comprehend the importance of team work, communication and sustainable solutions.

(4) Imbibe values, professional ethics for lifelong learning.

1) The duration of industrial training must be for a minimum of 1 week and maximum of 8 weeks on full time basis.
2) Industrial Training in which students pays a fee to the organization / industry will not be considered.
3) He/she can undergo training in one or more industry /organization.
4) The student must submit letters from the industry clearly specifying his / her name and the duration of the training provided by the company with authorized signatures.
5) Industrial training must be related to the field of specialization or the M.Tech program in which the student has enrolled.
6) Students undergoing industrial training are advised to use ICT tools such as skype to report their progress and submission of periodic progress reports to the faculty members.
7) Every student has to write and submit his/her own industrial training report to the designated faculty.
8) Students have to make a presentation on their industrial training in front of the departmental cmmittee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the final report.
9) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
10) The broad format of the industrial training report shall be as follows
    - Cover Page
    - Certificate from College
    - Training Certificate from Industry / Organization
    - Acknowledgement
    - Executive Summary
    - Table of Contents
    - Chapter 1 - Profile of the Organization –Organizational structure, Products, Services, Business Partners, Financials, Manpower, Societal Concerns, Professional Practices
    - Chapter 2 – Details of the Training Modules
    - Chapter 3 – Reflections – Highlight specific technical and soft skills that you acquired References & Annexure

Course Outcomes:

After going through the industrial training the student will be able to:

CO1: Understand the process of applying engineering knowledge to solve industrial problems
CO2: Develop skills through training relevant to industrial requirement
CO3: Communicate effectively and work in teams
CO4: Imbibe ethical practices and develop it as life skill.

Scheme of Continuous Internal Evaluation (CIE):
A committee comprising of Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):
The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation on the application of engineering knowledge 25%

(2) Ability to comprehend the importance of skilling and training 25%

(3) Importance of communication, professional ethics, sustainability 20%

(4) Oral Presentation and Report 30%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**
CO1		M	H	M		M				L	
CO2				H	M	M		L			
CO3					L		M	H	H		
CO4					L		H			M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	**PSO2**
CO1	H	
CO2	L	L
CO3		M
CO4	M	H

GUIDELINES FOR INDUSTRIAL VISITS

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the role of industries and service organization in meeting the demands of the society.

(2) Explain the working of different industries and organizations with an engineering perspective

(3) Comprehend the importance of team work, communication and sustainable solutions.

(4) Imbibe values, professional ethics for lifelong learning.

1) Student must visit a minimum of THREE organizations/industry. The duration of the visit per organization must be for ONE full day, during which he/she must comprehend the importance of organization structure, function of various departments, application of engineering knowledge, resource management, importance to environment and safety, professional ethics.
2) It is mandatory to visit ONE private multi-national company or public sector industry / organization, ONE medium-small enterprise and ONE rural based or NG organization.
3) The student must submit letter from the industry clearly specifying his / her name and the date of visit to the industry with authorized signatures.
4) Industrial visit must be related to the field of specialization or the M.Tech program in which the student has enrolled.
5) Every student has to write and submit his/her own report on each industrial visit and submit the report to the designated faculty advisor for evaluation.
6) A photograph outside the industry with the name and logo of the industry in the background along with the students and faculty members could be included in the report.
7) Students have to make a presentation on their industrial visit in front of the departmental committee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the final report.
8) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
9) The broad format of the industrial visit report shall be as follows
    - Cover Page
    - Certificate from College
    - Acknowledgement
    - Synopsis / Executive Summary
    - Table of Contents
    - Chapter 1 - Profile of the PSU or MNC – must include Organizational structure, Products, Services, Financials, Manpower, Societal Concerns, Professional Practices
    - Chapter 2 – Profile of the SME – must include Organizational structure, Products, Services, Financials, Manpower, Societal Concerns, Professional Practices
    - Chapter 3 - Profile of the NGO – must include Organizational structure, services, Manpower, Societal Concerns, Professional Practices

- Chapter 4 – Comparative Analysis of PSU/MNC – SME – NGO
- References & Annexure (Permission letters from the organizations for the visit & photographs)

Course Outcomes:

After going through this course the student will be able to:

CO1: Classify the role of different industries and organization in addressing the needs of the society.

CO2: Explain the process of applying engineering knowledge in industries and organizations.

CO3: Describe the importance of communication and team work

CO4: Recognize the importance of practicing professional ethics and need for life skills.

Scheme of Continuous Internal Evaluation (CIE):

A committee comprising of Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation of the application of engineering knowledge in industries 25%

(2) Ability to comprehend the functioning of the organization/ departments 30%

(3) Importance of resource management, environment and sustainability 20%

(4) Presentation Skills and Report 25%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		M	H	M		M				L	
CO2				H	M	M		L			
CO3					L		M	H	H		
CO4					L		H			M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	
CO2	L	L
CO3		M
CO4	M	H

TECHNICAL SEMINAR						
Course Code	**:**	**16MVE36**		**CIE Marks**	**:**	**50**
Hrs/Week	**:**	**L:T:P:S**	**0:0:4:0**	**SEE Marks**		**50**
Credits	**:**	**2**		**SEE Duration**		**30 min**

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the technological developments in their chosen field of interest
(2) Explain the scope of work and challenges in the domain area
(3) Analyze these engineering developments in the context of sustainability and societal concerns.
(4) Improve his/her presentation skills and technical report writing skills

GUIDELINES

1) The presentation will have to be done by individual students.
2) The topic of the seminar must be in one of the thrust areas with in-depth review and analysis on a current topic that is relevant to industry or on-going research.
3) The topic could be an extension or complementary to the project
4) The student must be able to highlight or relate these technological developments with sustainability and societal relevance.
5) Each student must submit both hard and soft copies of the presentation.

Course Outcomes:

After going through this course the student will be able to:

CO1:Identify topics that are relevant to the present context of the world
CO2: Perform survey and review relevant information to the field of study.
CO3: Enhance presentation skills and report writing skills.
CO4: Develop alternative solutions which are sustainable

Scheme of Continuous Internal Evaluation (CIE): Evaluation would be carried out in TWO phases. The evaluation committee shall comprise of Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

Rubrics for Evaluation:

1) Topic – Technical Relevance, Sustainability and Societal Concerns 15%
2) Review of literature 25%
3) Presentation Skills 35%
4) Report 25%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		H	M	M	L	H	H	--	---	---	M
CO2	L	M								H	
CO3							L	M	H		
CO4		L	M		H	H					H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	L
CO2	M	H
CO3	M	L
CO4	H	L

MAJOR PROJECT						
Course Code	**:**	**16MVE41**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**0:0:52:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**26**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

The students shall be able to

1. Understand the method of applying engineering knowledge to solve specific problems.
2. Apply engineering and management principles while executing the project
3. Demonstrate good verbal presentation and technical report writing skills.
4. Identify and solve complex engineering problems using professionally prescribed standards.

GUIDELINES

1. Major project will have to be done by only one student in his/her area of interest.
2. Each student has to select a contemporary topic that will use the technical knowledge of their program of specialization.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The number of projects that a faculty can guide would be limited to three.
5. The project can be carried out on-campus or in an industry or an organization with prior approval from the Head of the Department.
6. The standard duration of the project is for 16 weeks, however if the guide and the evaluation committee of the department, after the assessment feel that the work is insufficient and it has to be extended, then the student will have to continue as per the directions of the guide and the committee.
7. It is mandatory for the student to present his/her work in one of the international conferences or publish the research finding in a reputed unpaid journal with impact factor.

Course Outcomes:

After going through this course the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate lifelong learning

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in THREE Phases. The evaluation committee will comprise of: guide, two senior faculty members, one industry member and Head of the Department.

Phase	Activity	Weightage
I 5^{th} week	Synopsis, Preliminary report for the approval of selected topic along with literature survey, objectives and methodology.	20%
II 10^{th} week	Mid-term progress review shall check the compliance with the objectives and methodology presented in Phase I, review the work performed.	40%
III 15^{th} week	Oral presentation, demonstration and submission of project report. After this presentation, the student will have one week time to correct / modify his report to address the issues raised by the	40%

	committee members.	

CIE Evaluation shall be done with marks distribution as follows:

- Selection of the topic & formulation of objectives 10%
- Design and simulation/ algorithm development/experimental setup 25%
- Conducting experiments / implementation / testing / analysis 25%
- Demonstration & Presentation 20%
- Report writing 20%

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

1. Brief write-up about the project 5%
2. Formulation of Project Objectives & Methodology 20%
3. Experiments / Analysis Performed; Results & Discussion 25%
4. Report 20%
5. Viva Voce 30%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**
CO1	H	H	H	M	L	M	L				
CO2				L				M	H		
CO3					L	M	M			H	
CO4					L	M	H	M			H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	**PSO2**
CO1	H	L
CO2	L	H
CO3	M	H
CO4	H	H

SEMINAR						
Course Code	**:**	**16MVE42**		**CIE Marks**	**:**	**50**
Hrs/Week	**:**	**L:T:P:S**	**0:0:4:0**	**SEE Marks**		**50**
Credits	**:**	**2**		**SEE Duration**		**30 min**

Course Learning Objectives (CLO):

The students shall be able to:

1) Understand the technological developments in their chosen field of interest
2) Explain the scope of work and challenges in the domain area
3) Analyze these engineering developments in the context of sustainability, societal concerns and project management.
4) Improve his/her verbal presentation and report writing skills

GUIDELINES

1) The presentation will have to be done by individual students.
2) The topic of the seminar must be in one of the thrust areas with in-depth review and analysis on a current topic that is relevant to industry or on-going research.
3) The topic could be an extension or complementary to the project topic.
4) Topics could be in multidisciplinary areas and strongly address the technical design issues.
5) The student must be able to highlight or relate these technological developments with sustainability and societal relevance.
6) The students must mandatorily address legal, ethical issues as related to the topic of study.
7) The student shall make an attempt to perform financial / cost analysis or apply project management tools as related to his/her topic of study.
8) Each student must submit both hard and soft copies of the presentation.

Course Outcomes:

After going through this course the student will be able to:

CO1: Identify topics that are relevant in the present context of the world and relate it to sustainability and societal relevance.
CO2: Perform literature/market/product survey and analyse information to the field of study.
CO3: Enhance presentation and report writing skills.
CO4: Develop creative thinking abilities.

Scheme of Continuous Internal Evaluation (CIE): Evaluation would be carried out in TWO phases. The evaluation committee shall comprise of TWO senior faculty members. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

Rubrics for Evaluation:

- Topic – Technical Relevance, Sustainability and Societal Concerns 15%
- Literature Review 25%
- Presentation Skills 35%
- Report 25%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		H	M	M	L	H	H	--	---	---	M
CO2	L	M								H	
CO3							L	M	H		
CO4		L	M		H	H					H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	L
CO2	M	H
CO3	M	L
CO4	H	L