RashtreeyaSikshanaSamithi Trust

R.V. College of Engineering

(Autonomous Institution Affiliated to VisvesvarayaTechnologicalUniversity, Belagavi)

Department of Electronics& Communication Engineering

Master of Technology (M. Tech.)

VLSI DESIGN & EMBEDDED SYSTEMS

Scheme and Syllabus of Autonomous System w.e.f 2016

R.V. College of Engineering, Bengaluru – 59

(Autonomous Institution affiliated to VisvesvarayaTechnologicalUniversity, Belagavi)

Department of Electronics & Communication Engineering

Vision:

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering.

Mission:

- To impart quality technical education to produce industry-ready engineers with a research outlook.
- To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.
- To create centers of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.
- To develop entrepreneurial skills among the graduates to create new employment opportunities.

MASTER OF VLSI DESIGN & EMBEDDED SYSTEMS - Program

Program Educational Objectives (PEO)

M. Tech. in VLSI design and Embedded Systems Program, graduates will be able to:

PEO 1. Identify and apply appropriate Electronic Design Automation (EDA) to solve real world problems in VLSI and Embedded Systems domain to create innovative products and systems

PEO 2. Develop managerial skill and apply appropriate approachesinthe domains of VLSI design and Embedded Systems incorporating safety, sustainability and become a successfulprofessional or an Entrepreneur in the domain

PEO 3. Pursue career in research in VLSI Design and Embedded Systems domain through self learning and self directed on cutting edge technologies

Program Outcomes (PO)

M. Tech. in VLSI Design and Embedded Systems Programgraduates will be able to:

PO 1. Scholarship of Knowledge: Acquire in-depth knowledge of VLSI and Embedded systems in wider and global perspective, with an ability to discriminate, evaluate, analyze, synthesize and integrate for enhancement of knowledge.

PO 2. Critical Thinking: Analyze electronics engineering problems critically; applyindependent judgment for synthesizing information to make intellectual and/or creative advances for conducting research.

PO 3. Problem Solving: Think laterally and originally, conceptualize and solve technical problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

PO 4. Research Skill: Extract information through literature survey and experimentspertinent to unfamiliar problems, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze, demonstrate higher order skill, contribute individually/in group(s) to the development of scientific/technological knowledge in techno-managerial systems.

PO 5. Usage of modern tools: Create, select, learn and apply appropriate techniques, resources, and modern engineering and EDA tools including emulators for modeling and prototyping with an understanding of the tools limitations.

PO 6. Collaborative and Multidisciplinary work: Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

PO 7. Project Management and Finance: Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors.

PO 8. Communication: Communicate with the engineering community and society at large confidently and effectively to comprehend and write effective reports/design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

PO 9. Life-long Learning: Recognize the need for, and have the preparation and ability to engage in lifelong learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO 10. Ethical Practices and Social Responsibility: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO 11. Independent and Reflective Learning: Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes with or without depending on external feedback.

Program Specific Criteria (PSC)

Lead Society: Institute of Electrical and Electronics Engineers

1. Curriculum:

The curriculum shall include competency areas in VLSI Design & Embedded Systems including IC designing concepts & Embedded system designing concepts to analyze and design complex systems containing hardware and software components. The curriculum must prepare graduates for design and development of VLSI as well as Embedded Systems for different applications.

2. Faculty

The professional competence of the faculty must be in Analog IC Design, Digital IC Design, Embedded Systems Design and allied areas of VLSI as well as Embedded domains.

Program Specific Outcomes (PSO)

M. Tech. in VLSI Design and Embedded SystemsProgram graduates will be able to:

PSO 1. Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing, Verification and prototype development focusing on applications.

PSO 2. Integrate multiple sub-systems to develop System On Chip, optimize its performance and excel in industry sectors related to VLSI / Embedded domain.

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Department of Electronics & Communication Engineering

M. Tech. VLSI Design & Embedded Systems

FIRST SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MEM11R	Research Methodology	IM	3	1	0	0	4
2	16MVE12	Digital IC Design (Theory and Practice)	EC	4	0	1	0	5
3	16MVE13	Advanced Embedded System Design	EC	4	0	0	1	5
4	16MVE14	Digital System Design using Verilog	EC	4	0	0	0	4
5	16MVE15x	Elective 1	EC	4	0	0	0	4
6	16HSS16	Professional Skill Development	HSS	0	0	2	0	2
		Total		**19**	**1**	**3**	**1**	**24**

Elective-1			
16MVE151	Advanced Embedded Processors	16MVE152	ASIC Design

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Department of Electronics & Communication Engineering

M. Tech. VLSI Design & Embedded Systems

SECOND SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MEM21P	Project Management	IM	3	1	0	0	4
2	16MVE22	Analog IC Design (Theory and Practice)	EC	4	0	1	0	5
3	16MVE23x	Elective-2	EC	4	0	0	0	4
4	16MVE24x	Elective-3	EC	4	0	0	0	4
5	16MVE25x	Elective-4	EC	4	0	0	0	4
6	16MVE26	Minor Project	EC	0	0	5	0	5
		Total		**19**	**1**	**6**	**0**	**26**

Elective-2			
16MVE231	CAD Tools for VLSI	16MVE232	Real Time Embedded Systems
Elective-3			
16MVE241	Low Power VLSI Design	16MVE242	Advanced Embedded Programming
Elective-4			
16MVE251	High Speed VLSI Design	16MVE252	MEMS and Smart Systems

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Department of Electronics & Communication Engineering

M. Tech. VLSI Design & Embedded Systems

THIRD SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MVE31	System Verilog for Design & Verification of Digital Systems(Theory and Practice)	EC	4	0	1	0	5
2	16MVE32x	Elective-5	EC	4	0	0	0	4
3	16MVE33x	Elective-6	EC	4	0	0	0	4
4	16MVE34x	Elective-7	EC	4	0	0	0	4
5	16MVE35	Internship/Industrial Training	EC	0	0	3	0	3
6	16MVE36	Technical Seminar	EC	0	0	2	0	2
		Total		**16**	**0**	**6**	**0**	**22**

Elective-5			
16MVE321	Embedded System for Networking	16MVE322	Radio Frequency IC Design
Elective-6			
16MVE331	ARM programming and optimization	16MVE332	VLSI Testing
Elective-7			
16MVE341	Mixed Signal IC Design	16MVE342	Synthesis & Optimization of Digital Circuits

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M. Tech. VLSI Design & Embedded Systems

FOURTH SEMESTER								
Sl. No	**Course Code**	**Course Title**	**BoS**	**CREDIT ALLOCATION**				**Total Credits**
				Lecture L	**Tutorial T**	**Practical P**	**Self Study S**	
1	16MVE41	Major Project	EC	0	0	26	0	26
2	16MVE42	Seminar	EC	0	0	2	0	2
		Total		**0**	**0**	**28**	**0**	**28**

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THIRD SEMESTER

SystemVerilogfor Design and Verification of Digital Systems						
Course Code	**:**	**16MVE31**		**CIE Marks**	**:**	**100 +50**
Hrs/Week	**:**	**L:T:P:S:3:0:1:0**		**SEE Marks**	**:**	**100 +50**
Credits	**:**	**5**		**SEE Duration**	**:**	**3 Hrs +3Hrs**

Course Prerequisites:

The graduate is expected to possess the following pre-requisites

1. Concept of digital system design.
2. Concept of system design using Verilog.

Course Learning Objectives (CLO):

At the end of the course the student should be able to:

1. Write efficient SystemVerilog reference models for system design and verification.
2. Understand the important new SystemVerilog data types and capabilities; new SystemVerilog RTL and abstraction capabilities
3. Write complex self-checking testbenches - includes the use of new SystemVerilog Hardware Verification Language (HVL)capabilities.
4. Understand the object-oriented stimulus generation using classes, constrained random stimulus generation and functional coverage capabilities.
5. Write efficient synthesizable SystemVerilog RTL models - includes new SystemVerilog data types and capabilities, RTL and abstraction capabilities.
6. Gain the knowledge of complete digital system design and verification using SystemVerilog to be an industry ready engineer.

Unit – I	**10 Hrs**

Introduction to SystemVerilog:

SystemVerilog standards, Key SystemVerilog enhancements for hardware design.Advantages of System Verilog over Verilog, Data Types: Verilog data types, System Verilog data types, 2 - State Data types, Bit, byte, shortint, int, longint. 4 - State data types. Logic, Enumerated data types, User Defined data types, Struct data types, Strings, Packages, Type Conversion: Dynamic casting, Static Casting, Memories: Arrays, Dynamic Arrays, Multidimensional Arrays, Packed Arrays, Associative Arrays, Queues, Array Methods, Tasks and Functions: Verilog Tasks and Functions, Enhancements in S.V, Void Functions, Return Statement, Passing Arguments, Arguments Passing by Name, Default Arguments, Passing Arguments by Value, Passing Arguments by Reference.

Unit – II	**10 Hrs**

Connecting the Testbench and Design:

Verilog interface signals - Limitations of Verilog interface signals, SystemVerilog interfaces, SystemVerilog port connections, Interface instantiation 2.4. Interfaces Arguments, Interface Modports, Interface References, Tasks and functions in interface, Verilog Event Scheduler, SystemVerilog Event Scheduler, Clocking Block, Input and Output Skews, Typical Testbench Environment, Verification plan

Unit – III	10 Hrs

OOPs Basics and Advanced OOPs concepts:

Basic OOP Concepts

Overview of Classes, Properties and Methods in the Classes, Instance/Object Creation, New Constructor, Null Object handles, Accessing Members, this Keyword, Creating an Object, Objects Assignments, Copying an Object: Shallow Copy, Deep Copy

Advanced OOP Concepts

Inheritance: Concept of Inheritance, Super Keyword, Static properties**,** Overriding Methods**,** Polymorphism - $cast**,** Virtual Classes**,** Parameterized Classes

Unit – IV	10 Hrs

Constrained Randomization, Threads and Inter-process Communication:

Constrained Randomization

Random Variables - rand and randc, Randomize( ) Method - Pre/Post Randomize( ) methods, Constraints in the class, Rand_mode and constraint_mode, Constraint and Inheritance, Constraint Overriding, Set Membership, Distribution Constraints, Conditional Constraints - .implication (->), . if/else, Inline Constraints

Threads and Inter-process Communication

Threads, Fork-Join/Join_any/Join_none, Communication – Mailbox, Semaphore, Events, BuildingaTestbenchwithThreadsandIPC

Unit – V	10 Hrs

Functional Coverage andAssertion Based Verification:

Functional Coverage

Coverage Definition, Code Coverage, Functional Coverage: Cover Group, Creating Cover Group Instances, Coverpoints, Bins - . implicit bins, . Explicit bins, Bin creation, Vector and Scalar bins, Cross products, Intersect, Select Expressions, Conditional Expression (iff), Illegal bins, Ignore bins, Coverage Analysis, Covergroup Built-in Methods - . Sample(), . get_coverage(), .get_instance_coverage(), .set_instance_name(string), .start(), . stop()

Assertion Based Verification

Introduction, Types of Assertions - . Immediate, . Concurrent, Assertion Properties- . Writing Properties, Sequences- . Sequence Composition, . and, or, intersect, Advanced SVA Features - . Expect, Binding, Assertion Coverage

Laboratory exercises:

1. Data Types, Interfaces and OOPs

Experiments to understand the usage of

(a) the SystemVerilog data types such as associative arrays and interfaces constructs

(b) the OOP basics such as class, assignment handling, deep copy, inheritance, virtual functions (polymorphism)

2. Randomization, Threads, Mailbox and Semaphores

Experiments to understand the usage of

(a) the SystemVerilog Random variables and constraints

(b) the SystemVerilog threads, mailbox and Semaphores

3. Transactions and Transactors

Experiments to understand the usage of

(a) the SystemVerilog transaction and create transaction

(b) the SystemVerilogTransactors such as generator, driver, monitor, and reference models

4. Scoreboard

Experiments to understand the usage of Scoreboard

5. Environment

Experiments to understand the usage of Environment

Expected Course Outcomes:

After taking up this course, the graduate will be able to:

CO1: Demonstrate the use SystemVerilog data types for digital system design and functional verification.

CO2: Demonstrate the skill on writing test-benches for design digital systemsand connecting them with the design.

CO3: Verify and Analyze the complete systems through robust verification methodsuch as assertion based verification.

CO4: Design and verify the digital systems such as FIFOs, memories, ATM interfaces, etc. using the learnt methods and demonstrate the skills.

Reference Books:

1.	Stuart Sutherland, Simon Davidmann and Peter Flake, "*SystemVerilog for Design - A Guide to Using SystemVerilog for Hardware Design and Modeling*," 2E, Springer Science, ISBN-13: 978-0387-3339-91, 2006.
2.	C Spear, "*SystemVerilog for Verification-A Guide to Learning the Testbench Language Features*," Springer Science, IEEE press, ISBN-13: 978-0387-2703-64,2006.
3.	Doulos, "*SystemVerilog golden reference guide*-A concise guide to SystemVerilog IEEE Standard-1800-2009," Version 5.0,ISBN: 0-9547345-9-9, 2012.
4.	SasanIman, "*Step-by-Step Functional Verification with SystemVerilog and OVM*," Hansen Brown Publishing Company,ISBN-13: 978-0-9816-5621-2, 2008.
5.	IEEE Computer Society, "*IEEE Standard for SystemVerilog-Unified Hardware Design, Specification and Verification*," IEEE Press, ISBN: 978-0-7381-6129-7, 2009

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Continuous Internal Evaluation (CIE) for Practical

CIE for the practical courses will be based on the performance of the student in the laboratory,every week. The laboratory records will be evaluated for 40 marks. One test will be conducted for 10 marks. The total marks for CIE (Practical) will be for 50 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice foreach unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Scheme of Semester End Examination (SEE) for Practical

SEE for the practical courses is based on conducting the experiment and proper results (for 40 marks) and viva-voce (for 10 marks). The total marks for SEE (Practical) is 50.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	H	H	H	-	M	H	-	L
CO2	H	H	H	H	H	M	L	-	H	-	H
CO3	H	H	H	H	H	H	-	L	H	M	H
CO4	H	H	H	H	H	H	L	M	H	H	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	M	H
CO2	H	M
CO3	M	H
CO4	H	H

Embedded System for Networking						
Course Code	**:**	**16MVE321**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**4:0:0:0**		**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Prerequisites :

Fundamentals of digital electronics, Embedded Processors and Computer Networks

Course Learning Objectives (CLOs):

Graduate shall be able to

1. Understand requirements of an embedded system for networking application and the issues pertaining to such embedded computing system design.
2. Illustrate how microprocessor, memory, peripheral components and buses build an embedded platform and their interaction for implementation of networking protocols.
3. Evaluate how architectural and implementation design decisions influence performance and scaling
4. Building, testing the operation of real-timeIoTapplication protocol through hands-on experience with a single-board computer.

Unit – I	**09 Hrs**

EMBEDDED PROCESSOR FOR NETWORK PROTOCOL PROCESSING

Introduction and overview, basic terminology and example systems, review of protocols and packet format, Conventional computer hardware architecture, basic packet processing, packet processing functions, protocol software on a conventional processor, hardware architecture for protocol processing, classification and forwarding, switching fabrics, Hardware/Software Traffic management implementation.

Unit – II	**09 Hrs**

INTRODUCTION TO ADVANCED ARCHITECTURE: NETWORK PROCESSOR

Network processors, the complexity of network processor design, network processor architectural Overview and comparison of commercial network processors: the Intel network processor, RISC processor, packet processor hardware.

Unit – III	**10 Hrs**

SCALING IN NETWORK PROCESSORS

Scalability with Parallelism And Pipelining - issues in scaling a network processor- Complexity Of Network Processor Design (packet processing, ingress & egress processing, Macroscopic Data Pipelining And Heterogeneity etc) - Network Processor fun : Packet Flow, Clock Rates, software architecture, Assigning Functionality To The Processor Hierarchy

Unit – IV	**10 Hrs**

CLASSIFICATION OF NETWORK PROCESSORS

Basis in Classification of network processors- Multichip pipeline, configurable instruction set processors, packet processor, Augmented RISC Processor, Embedded Processor Plus Coprocessors- Design Tradeoff s and consequences (Programmability Vs. Processing Speed , speed vs functionality. etc)

Unit – V	**10 Hrs**

INTERNET OF THINGS

Introduction to IoT, Attributes of Processors for IoT, memory for IoT, Introduction to IoT protocols: MQTT, 6LoWPAN, Programming for IoT (C, Node.js)
Implementation of MQTT on various platforms (RASBERRY PI).

Expected Course Outcomes:

After going through this course the student will be able to:

CO1: Describe the architecture ofembedded system with functional requirements for hardwareand software components to realize networking applications.
CO2: Analyze the architecture of network processor to support complex data processing operations.
CO3: Design firmware for networking embedded systems by utilizing advanced hardware features.
CO4: Demonstrate an ability to read, critically evaluate, analyze and present (verbally or in written form) the content and implications of research articles in the area.

Reference Books:

1.	Douglas E. Comer ”Network System Design using Network Processors” Prentice Hall , 2006.
2.	Jorgen Staunstrup, Wayne Wolf, “Harware/Software Co-Design:Principles and Practice”, Kluwer Academic Pub, 1997
3.	Patrick Crowley, M A Franklin, H Hadimioglu, PZ Onufryk, “Network Processor Design, Issues and Practices Vol – I , 2, Morgan Kauffman, E l s e v i e r 2011
4.	DeepankarMedhi , KarthikeyanRamasamy, “Network Routing : Algorithms, Protocols, andArchitecture”, El sevier, 2007

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Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	H	M	M	L	L	-	M	H	-	L
CO2	H	H	M	M	L	M	-	M	H	-	M
CO3	H	H	H	H	M	H	-	H	H	-	H
CO4	H	H	H	M	M	H	-	H	H	M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	L
CO2	H	L
CO3	H	M
CO4	H	H

Radio Frequency IC Design						
Course Code	**:**	**16MVE322**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

Students shall be able to

1. Apply the knowledge of radio frequency circuits in IC design.
2. Analyze the functionality and design issues of RF circuits and systems.
3. Design and implement RF transceiver/ related circuitry
4. Evaluate the different performance parameters used in RF design.

Unit – I	**10 Hrs**

Basic concepts in RF design - Nonlinearity and Time Variance, Effects of nonlinearity – harmonic distortion, gain compression, desensitization, cross modulation, intermodulation, cascaded nonlinear stages – level diagram. Noise in RF circuits – Noise figure, Noise figure of cascaded and lossy circuits, Sensitivity and dynamic range.

Unit – II	**10 Hrs**

RF Systems Design - Receiver architectures - Heterodyne - dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, Image Reject – Hartley architecture, Transmitter architectures - Direct conversion and two-step transmitters.

RF Circuits Design (MOSFET circuits only)

Low noise Amplifier - Performance parameters, Problem of Input matching, LNA topologies – Variants of common source only, design examples.

Unit – III	**10 Hrs**

Mixer - Mixer fundamentals, Performance parameters, Nonlinear systems as linear mixers, two port example –square law mixers, multiplier based mixers – Single balanced and double balanced (active and passive) - working and implementation, (MOSFET circuits only).

Oscillator - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, VCO characteristics, Phase noise – basic concepts and effects of phase noise (no analysis).

Unit – IV	**9 Hrs**

Phase Locked Loop Design - Type-II PLL: design equations, phase margin, and closed-loop PLL response, Design methodology for a Type-II 3rd –order PLL, charge pump design issues, Charge Pump design techniques: charge-injection, clock feed-through. Current steering CP design, replica biasing, professional charge pump, Charge pump non-idealities and their mitigation: Dead zone, current mismatch, charge sharing, PLL Noise Analysis.

Unit – V	**9 Hrs**

Frequency Synthesizers: General considerations, Basic Integer N synthesizer, settling behavior, spur reduction techniques, PLL based modulation, Divider design – Pulse swallow divider, dual modulus divider, divider logic styles – current steering, CML latch, true single phase clocking. Fractional N synthesizers- basic concepts only.

Expected Course Outcomes:

After going through this course the student will be able to:

1. Apply the knowledge of RF circuits & systems in IC design
2. Analyze CMOS circuits and its impact on Radio frequency IC design.
3. Design and implement RF transceiver chain with specification.

4. Evaluate the different performance parameters used in RF design using CAD tools.	
Reference Books:	
1.	BehzadRazavi, "RF Microelectronics ", 2nd Edition Pearson Education, 2012
2.	John Rogers ,Calvin Plett, "Radio Frequency Integrated Circuits Design", Artech House, 2003
3.	Thomas H Lee , "The Design of CMOS Radio Frequency Integrated Circuits",2nd Edition, Cambridge University Press, 2004
4.	Bosco Leung, "VLSI for Wireless Communications", Pearson Education, 2004

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	H	H	H	-	-	M	-	M
CO2	H	H	H	H	H	H	-	-	M	-	M
CO3	H	H	H	H	H	H	-	-	M	-	M
CO4	H	H	H	H	H	H	-	-	M	-	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1		H
CO2	H	
CO3		M
CO4	H	H

ARM PROGRAMMING AND OPTIMIZATION						
Course Code	**:**	**16MVE331**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

The student will be able to

1. Discuss the basic principles of ARM system design.
2. Identify the major hardware components ARM data path architecture.
3. Identify the design issues ARM based embedded system with the basic knowledge of firmware, embedded OS & ARM architectures.
4. Analyze the execution of instructions/program knowing the basic principles of ARM architecture and assembly language.
5. Compare programs written in C & assembly to execute on ARM platform.

Unit – I	**9Hrs**

Introduction, Data Path Architecture, Registers, Modes, Exceptions

Programming in C for ARM

Overview of C Compilers and optimization, basic C data types, C looping structures, register allocation, function calls, pointer aliasing, structure arrangement, bit fields, unaligned Data and Endianess, division, floating point, inline functions and inline assembly, portability issues.

Unit – II	**9Hrs**

Writing and Optimizing ARM Assembly Code

Writing assembly code, profiling and cycle counting, instruction scheduling, register allocation, conditional execution, looping constructs, Bit manipulation, efficient switches. Handling unaligned data.

Unit – III	**10 Hrs**

Digital Signal Processing on ARM

Representing a digital signal, Introduction to DSP on the ARM, FIR filters: Realization of filters on ARM7 and Cortex M3, IIR Filters: Realization of filters on ARM7 and Cortex M3, CMSIS DSP Library.

Unit – IV	**10Hrs**

Firmware

Firmware and Boot loader

Embedded Operating Systems

Fundamental Components, Simple Operating System.

Unit – V	**10Hrs**

Memory Protection Unit

Over view of the MPU's, MPU registers, setting up the MPU, Memory barrier and memory configuration, Using sub-region disable, Consideration when using MPU, Other usages of MPU.

Expected Outcome:

On completion of the course the student will be able to:

CO1. Describe the programmer's model of ARM processor and analyse the instruction set architecture torealize complex operations.

CO2. Apply the optimization methods available for ARM architectures to design embedded software to meet given constraints with the help of modern engineering tools.

CO3. Realize real time signal processing applications & primitive OS operations on different

	ARM architectures by making use of software libraries. CO4. Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments.
Reference Books:	
1.	Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publishers, 2008, ISBN-13:9788181476463
2.	Joseph Yiu, "The definitive Guide to the ARM Cortex- M3 & M4 Processors", 3rd Edition, Newnes (Elsevier), 2014, ISBN: 978-93-5107-175-4
3.	Steve Furber, "ARM System on Chip Architecture", Pearson Education Limited,2nd Edition, ISBN-13:9780201675191
4.	Technical reference manual for ARM processor cores, including Cortex M series, ARM 11, ARM 9 & ARM 7 processor families.
5.	User guides and reference manuals for ARM software development and modeling tools.

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	H	H	H	-	M	H	-	L
CO2	H	M	H	M	H	M	-	M	H	-	H
CO3	H	H	H	L	H	H	-	-	H	-	H
CO4	H	H	H	L	H	H	-	-	H	L	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1		H
CO2	H	M
CO3		H
CO4	H	H

VLSI TESTING						
Course Code	**:**	**16MVE332**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLOs):

The student will be able to

1. Model and simulate different types of faults in digital circuits.
2. Establish equivalence and dominance relationships of faults in a circuit
3. Critique and compare ATPG algorithms with respect to speed, fault coverage and other criteria.
4. Comprehend the different testing diagnostic & fault simulation techniques

Unit – I	**9 Hrs**

Introduction to Testing: Role of testing VLSI circuits, VLSI trends affecting testing, Physical Faults, Stuck-at Faults, Stuck open Faults, Permanent, Intermittent and Pattern Sensitive Faults, Delay Faults.

Fault Modeling- Functional Testing, Structural Testing, Types of Fault Models, Stuck-at Faults, Bridging Faults, cross point faults, Fault Equivalence, Fault Dominance

Unit – II	**9 Hrs**

Testability Measure – Controllability, Observability, SCOAP measures for combinational and sequential circuits.

ATPG for Combinational Circuits: Path Sensitization Methods, Roth's D- Algorithm, Boolean Difference, PODEM Algorithm.Complexity of Sequential ATPG, Time Frame Expansion.

Unit – III	**10 Hrs**

Design for Testability- Ad-hoc, Structured DFT- Scan method, Scan Design Rules, Overheads of Scan Design, partial scan methods, multiple chain scan methods.

Fault Simulation- Fault Simulation algorithm- Serial, Parallel, Deductive and Concurrent Fault Simulation.

Boundary Scan Standard - TAP Controller, Test Instructions.

Unit – IV	**10 Hrs**

Selftest And Test Algorithms

Built-In self-Test,test pattern generation for BIST, response compaction - Parity checking, Ones counting, Transition Count, Signature analyzer.Circular BIST,BIST Architectures.

Testable Memory Design Test Algorithms, Reduced Functional Faults-MARCH and MAT+ algorithm. Test generation for Embedded RAMs.

Unit – V	**10 Hrs**

Fault Diagnosis

Logical Level Diagnosis,Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits, Self-checking design, System Level Diagnosis.

CO1. Acquire knowledge about fault modeling & collapsing.
CO2. Analyse various combinational ATPG techniques
CO3. Evaluate the significance of sequential test pattern generation
CO4. Develop fault simulation techniques & fault diagnosis methods

Reference Books:

Reference Books:

1. Michael L.Bushnell, Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital

	Memory & Mixed Signal VLSI Circuits", Kluwer Academic Publications, 1999.
2.	MironAbramovici, Melvin A. Breuer, Arthur D. Friedman, " Digital Systems Testing and Testable Design", 3rd Edition, Jaico Publishing House, 2004
3.	Hideo Fujiwara, " Logical testing & design for testability", The MIT Press.
4.	Parag.K.Lala "Digital Circuit Testing and Testability" Academic Press.

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	H	M	H	H	M	-	M	L	-	L
CO2	M	H	M	H	H	M	-	M	L	-	M
CO3	M	M	M	H	H	M	-	M	L	-	M
CO4	-	M	M	H	H	M	-	M	L	-	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	M
CO2	H	-
CO3	-	H
CO4	H	M

Mixed Signal IC Design						
Course Code	**:**	**16MVE341**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

Students shall be able to

1. Design Sample and Hold circuits.
2. Analyze Switched Capacitor Amplifiers and its non idealities.
3. Design various types of ADC/DAC for a given specification
4. Design oversampling converter considering all the practical issues for the given specification.

Unit – I **10Hrs**

Sampling

Introduction, sampling, Spectral properties of sampled signals, Oversampling – Anti-alias filter design. Time Interleaved Sampling, Ping-pong Sampling System, Analysis of offset and gain errors in Time Interleaved Sample and Hold. Sampling circuits- Distortion due to switch, Charge injection, Thermal noise in sample and holds, Bottom plate sampling, Gate bootstrapped switch, Nakagome charge pump. Characterizing Sample and hold, Choice of input frequency.

Unit – II **10Hrs**

Switched Capacitor Amplifiers

Common mode feedback (CMFB) – resistive CM detector, CMFB compensation, single-stage differential opamp. Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers, Non idealities in SC Amplifiers – Finite gain, DC offset, Gain- Bandwidth Product. Fully differential SC circuits, DC negative feedback in SC circuits.Switched-capacitor CMFB: design, analysis

Unit – III **10Hrs**

Analog to Digital Converter

Static specifications: INL, DNL; Dynamic specifications: SNDR, DR, SFDR, linearity.

Flash ADC, Regenerative latch, Preamp offset correction, Preamp Design, necessity of up-front sample and hold for good dynamic performance.

Unit – IV **10Hrs**

Digital to Analog Converter

Linearity errors, DAC spectra and pulse shapes. NRZ vs RZ DACs. DAC Architectures: Binary weighted, Thermometer DAC, Current steering DAC – Current cell design in current steering DAC, Charge Scaling DAC

Unit – V **10Hrs**

Oversampling Converter

Benefits of Oversampling, Oversampling with Noise Shaping, Signal and Noise Transfer Functions, First and Second Order Delta-Sigma Converters. Signal Dependent Stability of Describing Function Method. Introduction to Continuous-time Delta Sigma Modulators, time-scaling, inherent anti-aliasing property, Excess Loop Delay, Time-constant changes, Influence of Op amp nonidealities.

Expected Course Outcomes:

After going through this course the student will be able to:

1. Design Sample and Hold circuits.
2. Analyze Switched Capacitor Amplifiers and its non idealities.
3. Design various types of ADC/DAC for a given specification
4. Evaluate the different performance parameters of ADC/ DAC

Reference Books:	
1.	M. Gustavsson, J. Wikner, and N. Tan, "CMOS Data Converters for Communication" Kluwer Academic Publishers, 2000.
2.	BehzadRazavi, "Principles of Data Conversion System Design" Wiley-IEEE Press, 1994
3.	David A.Johns, Ken Martin, "Analog Integrated Circuit Design" John Wiley & Sons Inc. 1997
4.	R.Jacob Baker, "CMOS Mixed Signal Circuit Design", IEEE Press Series on Microelectronic Systems, 2002.

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Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**
CO1	H	M	M	H	H	H	-	-	M	-	M
CO2	H	H	H	H	H	H	-	-	M	-	M
CO3	H	H	H	H	H	H	-	-	M	-	M
CO4	H	H	H	H	H	H	-	-	M	-	M

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	**PSO2**
CO1	M	H
CO2	H	M
CO3	M	H
CO4	H	H

Synthesis and Optimization of Digital Circuits						
'Course Code	**:**	16MVE342		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

1. Analyse different levels of abstraction and different types of algorithms for VLSI functional models
2. Draw data flow and sequencing graphs for different types of VLSI models and use compilation and optimization techniques
3. Optimize Sequential circuit using state based models, and using network models
4. Schedule VLSI models with and without resource constraints using different algorithm
5. Analyze simulators for fault, Automatic test pattern generation (ATPG), design for Testability (DFT) Techniques

Unit – I	**9 Hrs**

Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Unit – II	**9 Hrs**

Schedule Algorithms: A model for scheduling problems, Scheduling wither source and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, dataflow and sequencing graphs, compilation and optimization techniques.

Unit – III	**10 Hrs**

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Unit – IV	**10 Hrs**

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Unit – V	**10 Hrs**

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table FPGAs and Anti fuse based FPGAs), rule based library binding.

Expected Course Outcomes:

After going through this course the student will be able to:

1. Understand and apply the various algorithms and graphs to synthesis and optimization of different digital circuit.
2. Analyze the performance of standard algorithm used for synthesis and optimization of two level, multiple level and sequential logic circuits
3. Demonstrate the improvement of optimization techniques used for digital circuits
4. Develop an algorithm for synthesis and optimization

Reference Books:

1.	Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.
2.	SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer, "Logic Synthesis", McGraw-Hill, USA, 1994.
3.	NeilWeste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", 2nd edition, Pearson Education (Asia) Pte.Ltd., 2000.

Scheme of Continuous Internal Evaluation (CIE) for Theory

CIE will consist of TWO Tests, TWO Quizzes and ONE assignment. The test will be for 30 marks each and the quiz for 10 marks each. The assignment will be for 20 marks. The total marks for CIE (Theory) will be 100 marks.

Scheme of Semester End Examination (SEE) for Theory

The question paper contains FIVE questions with internal choice for each unit. Each question carries 20 marks. Students have to answer one question from each unit. The total marks for SEE (Theory) is 100.

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	M	M	M	H	H	-	M	H	-	L
CO2	H	H	H	M	H	M	-	M	H	-	H
CO3	H	H	H	M	H	H	-	-	H	-	H
CO4	H	H	H	M	H	H	-	-	H	-	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	M	H
CO2	H	M
CO3	M	H
CO4	H	H

INTERNSHIP / INDUSTRIAL TRAINING						
Course Code	**:**	**16MVE35**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**0:0:6:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**3**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES FOR INTERNSHIP

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the process of applying engineering knowledge to produce product and provide services.

(2) Explain the importance of management and resource utilization

(3) Comprehend the importance of team work, protection of environment and sustainable solutions.

(4) Imbibe values, professional ethics for lifelong learning.

1) The duration of the internship shall be for a period of 8 weeks on full time basis between II semester final exams and beginning of III semester.
2) The student must submit letters from the industry clearly specifying his / her name and the duration of the internship on the company letter head with authorized signature.
3) Internship must be related to the field of specialization or the M.Tech program in which the student has enrolled.
4) Students undergoing internship training are advised to use ICT tools such as skype to report their progress and submission of periodic progress reports to the faculty members.
5) Every student has to write and submit his/her own internship report to the designated faculty.
6) Students have to make a presentation on their internship activities in front of the departmental committee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the internship final report. However interim or periodic reports and reports as required by the industry / organization can be submitted as per the format acceptable to the respective industry /organizations.
7) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
8) The broad format of the internship final report shall be as follows
    - Cover Page
    - Certificate from College
    - Certificate from Industry / Organization
    - Acknowledgement
    - Synopsis
    - Table of Contents
    - Chapter 1 - Profile of the Organization – Organizational structure, Products, Services, Business Partners, Financials, Manpower, Societal Concerns, Professional Practices,
    - Chapter 2 - Activities of the Department -

- Chapter 3 – Tasks Performed – summaries the tasks performed during 8 week period
- Chapter 4 – Reflections – Highlight specific technical and soft skills that you acquired during internship
- References & Annexure

Course Outcomes:

After going through the internship the student will be able to:

CO1: Apply engineering and management principles
CO2: Analyze real-time problems and suggest alternate solutions
CO3: Communicate effectively and work in teams
CO4: Imbibe the practice of professional ethics and need for lifelong learning.

Scheme of Continuous Internal Evaluation (CIE):

A committee comprising of the Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation of the application of engineering knowledge in industries 35%
(2) Ability to comprehend the functioning of the organization/ departments 20%
(3) Importance of resource management, environment and sustainability 25%
(4) Presentation Skills and Report 20%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		M	H	M		M				L	
CO2				H	M	M		L			
CO3					L		M	H	H		
CO4					L		H			M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	
CO2	L	L
CO3		M
CO4	M	H

GUIDELINES FOR INDUSTRIAL TRAINING

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the process of applying engineering knowledge to industrial products & processes
(2) Explain the importance of skilling, training and resource management.
(3) Comprehend the importance of team work, communication and sustainable solutions.
(4) Imbibe values, professional ethics for lifelong learning.

1) The duration of industrial training must be for a minimum of 1 week and maximum of 8 weeks on full time basis.
2) Industrial Training in which students pays a fee to the organization / industry will not be considered.
3) He/she can undergo training in one or more industry /organization.
4) The student must submit letters from the industry clearly specifying his / her name and the duration of the training provided by the company with authorized signatures.
5) Industrial training must be related to the field of specialization or the M.Tech program in which the student has enrolled.
6) Students undergoing industrial training are advised to use ICT tools such as skype to report their progress and submission of periodic progress reports to the faculty members.
7) Every student has to write and submit his/her own industrial training report to the designated faculty.
8) Students have to make a presentation on their industrial training in front of the departmental cmmittee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the final report.
9) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
10) The broad format of the industrial training report shall be as follows
    - Cover Page
    - Certificate from College
    - Training Certificate from Industry / Organization
    - Acknowledgement
    - Executive Summary
    - Table of Contents
    - Chapter 1 - Profile of the Organization –Organizational structure, Products, Services, Business Partners, Financials, Manpower, Societal Concerns, Professional Practices
    - Chapter 2 – Details of the Training Modules
    - Chapter 3 – Reflections – Highlight specific technical and soft skills that you acquired

    References & Annexure

Course Outcomes:

After going through the industrial training the student will be able to:

CO1: Understand the process of applying engineering knowledge to solve industrial problems
CO2: Develop skills through training relevant to industrial requirement
CO3: Communicate effectively and work in teams

CO4: Imbibe ethical practices and develop it as life skill.

Scheme of Continuous Internal Evaluation (CIE):
A committee comprising of Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):
The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation on the application of engineering knowledge 25%
(2) Ability to comprehend the importance of skilling and training 25%
(3) Importance of communication, professional ethics, sustainability 20%
(4) Oral Presentation and Report 30%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		M	H	M		M				L	
CO2				H	M	M		L			
CO3					L		M	H	H		
CO4					L		H			M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	
CO2	L	L
CO3		M
CO4	M	H

GUIDELINES FOR INDUSTRIAL VISITS

Course Learning Objectives (CLO):
The students shall be able to:
(1) Understand the role of industries and service organization in meeting the demands of the society.
(2) Explain the working of different industries and organizations with an engineering perspective
(3) Comprehend the importance of team work, communication and sustainable solutions.

(4) Imbibe values, professional ethics for lifelong learning.

1) Student must visit a minimum of THREE organizations/industry. The duration of the visit per organization must be for ONE full day, during which he/she must comprehend the importance of organization structure, function of various departments, application of engineering knowledge, resource management, importance to environment and safety, professional ethics.
2) It is mandatory to visit ONE private multi-national company or public sector industry / organization, ONE medium-small enterprise and ONE rural based or NG organization.
3) The student must submit letter from the industry clearly specifying his / her name and the date of visit to the industry with authorized signatures.
4) Industrial visit must be related to the field of specialization or the M.Tech program in which the student has enrolled.
5) Every student has to write and submit his/her own report on each industrial visit and submit the report to the designated faculty advisor for evaluation.
6) A photograph outside the industry with the name and logo of the industry in the background along with the students and faculty members could be included in the report.
7) Students have to make a presentation on their industrial visit in front of the departmental committee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the final report.
8) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
9) The broad format of the industrial visit report shall be as follows
    - Cover Page
    - Certificate from College
    - Acknowledgement
    - Synopsis / Executive Summary
    - Table of Contents
    - Chapter 1 - Profile of the PSU or MNC – must include Organizational structure, Products, Services, Financials, Manpower, Societal Concerns, Professional Practices
    - Chapter 2 – Profile of the SME – must include Organizational structure, Products, Services, Financials, Manpower, Societal Concerns, Professional Practices
    - Chapter 3 - Profile of the NGO – must include Organizational structure, services, Manpower, Societal Concerns, Professional Practices
    - Chapter 4 – Comparative Analysis of PSU/MNC – SME – NGO
    - References & Annexure (Permission letters from the organizations for the visit & photographs)

Course Outcomes:

After going through this course the student will be able to:

CO1: Classify the role of different industries and organization in addressing the needs of the society.

CO2: Explain the process of applying engineering knowledge in industries and

organizations.
CO3: Describe the importance of communication and team work
CO4: Recognize the importance of practicing professional ethics and need for life skills.

Scheme of Continuous Internal Evaluation (CIE):

A committee comprising of Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation of the application of engineering knowledge in industries 25%
(2) Ability to comprehend the functioning of the organization/ departments 30%
(3) Importance of resource management, environment and sustainability 20%
(4) Presentation Skills and Report 25%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		M	H	M		M				L	
CO2				H	M	M		L			
CO3					L		M	H	H		
CO4					L		H			M	H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	
CO2	L	L
CO3		M
CO4	M	H

TECHNICAL SEMINAR						
Course Code	**:**	**16MVE36**		**CIE Marks**	**:**	**50**
Hrs/Week	**:**	**L:T:P:S**	**0:0:4:0**	**SEE Marks**		**50**
Credits	**:**	**2**		**SEE Duration**		**30 min**

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the technological developments in their chosen field of interest
(2) Explain the scope of work and challenges in the domain area
(3) Analyze these engineering developments in the context of sustainability and societal concerns.
(4) Improve his/her presentation skills and technical report writing skills

GUIDELINES

1) The presentation will have to be done by individual students.
2) The topic of the seminar must be in one of the thrust areas with in-depth review and analysis on a current topic that is relevant to industry or on-going research.
3) The topic could be an extension or complementary to the project
4) The student must be able to highlight or relate these technological developments with sustainability and societal relevance.
5) Each student must submit both hard and soft copies of the presentation.

Course Outcomes:

After going through this course the student will be able to:
CO1:Identify topics that are relevant to the present context of the world
CO2: Perform survey and review relevant information to the field of study.
CO3: Enhance presentation skills and report writing skills.
CO4: Develop alternative solutions which are sustainable

Scheme of Continuous Internal Evaluation (CIE): Evaluation would be carried out in TWO phases. The evaluation committee shall comprise ofHead of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

Rubrics for Evaluation:

1) Topic – Technical Relevance, Sustainability and Societal Concerns 15%
2) Review of literature 25%
3) Presentation Skills 35%
4) Report 25%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		H	M	M	L	H	H	--	---	---	M
CO2	L	M								H	
CO3							L	M	H		

CO4		L	M		H	H					H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	L
CO2	M	H
CO3	M	L
CO4	H	L

MAJOR PROJECT						
Course Code	**:**	**16MVE41**		**CIE Marks**	**:**	**100**
Hrs/Week	**:**	**L:T:P:S**	**0:0:52:0**	**SEE Marks**	**:**	**100**
Credits	**:**	**26**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

The students shall be able to

1. Understand the method of applying engineering knowledge to solve specific problems.
2. Apply engineering and management principles while executing the project
3. Demonstrate good verbal presentation and technical report writing skills.
4. Identify and solve complex engineering problems using professionally prescribed standards.

GUIDELINES

1. Major project will have to be done by only one student in his/her area of interest.
2. Each student has to select a contemporary topic that will use the technical knowledge of their program of specialization.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The number of projects that a faculty can guide would be limited to three.
5. The project can be carried out on-campus or in an industry or an organization with prior approval from the Head of the Department.
6. The standard duration of the project is for 16 weeks, however if the guide and the evaluation committee of the department, after the assessment feel that the work is insufficient and it has to be extended, then the student will have to continue as per the directions of the guide and the committee.
7. It is mandatory for the student to present his/her work in one of the international conferences or publish the research finding in a reputed unpaid journal with impact factor.

Course Outcomes:

After going through this course the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate lifelong learning

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in THREE Phases. The evaluation committee will comprise of: guide, two senior faculty members, one industry member and Head of the Department.

Phase	Activity	Weightage
I 5th week	Synopsis, Preliminary report for the approval of selected topic along with literature survey, objectives and methodology.	20%
II 10th week	Mid-term progress review shall check the compliance with the objectives and methodology presented in Phase I, review the work performed.	40%
III 15th week	Oral presentation, demonstration and submission of project report. After this presentation, the student will have one week time to correct / modify his report to address the issues raised by the committee members.	40%

CIE Evaluation shall be done with marks distribution as follows:

- Selection of the topic & formulation of objectives 10%
- Design and simulation/ algorithm development/experimental setup 25%

- Conducting experiments / implementation / testing / analysis 25%
- Demonstration & Presentation 20%
- Report writing 20%

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

1. Brief write-up about the project 5%
2. Formulation of Project Objectives & Methodology 20%
3. Experiments / Analysis Performed; Results & Discussion 25%
4. Report 20%
5. Viva Voce 30%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	H	H	H	M	L	M	L				
CO2				L				M	H		
CO3					L	M	M			H	
CO4					L	M	H	M			H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	L
CO2	L	H
CO3	M	H
CO4	H	H

SEMINAR						
Course Code	**:**	**16MVE42**		**CIE Marks**	**:**	**50**
Hrs/Week	**:**	**L:T:P:S**	**0:0:4:0**	**SEE Marks**		**50**
Credits	**:**	**2**		**SEE Duration**		**30 min**

Course Learning Objectives (CLO):

The students shall be able to:

1) Understand the technological developments in their chosen field of interest
2) Explain the scope of work and challenges in the domain area
3) Analyze these engineering developments in the context of sustainability, societal concerns and project management.
4) Improve his/her verbal presentation and report writing skills

GUIDELINES

1) The presentation will have to be done by individual students.
2) The topic of the seminar must be in one of the thrust areas with in-depth review and analysis on a current topic that is relevant to industry or on-going research.
3) The topic could be an extension or complementary to the project topic.
4) Topics could be in multidisciplinary areas and strongly address the technical design issues.
5) The student must be able to highlight or relate these technological developments with sustainability and societal relevance.
6) The students must mandatorily address legal, ethical issues as related to the topic of study.
7) The student shall make an attempt to perform financial / cost analysis or apply project management tools as related to his/her topic of study.
8) Each student must submit both hard and soft copies of the presentation.

Course Outcomes:

After going through this course the student will be able to:

CO1: Identify topics that are relevant in the present context of the world and relate it to sustainability and societal relevance.

CO2: Perform literature/market/product survey and analyse information to the field of study.

CO3: Enhance presentation and report writing skills.

CO4: Develop creative thinking abilities.

Scheme of Continuous Internal Evaluation (CIE): Evaluation would be carried out in TWO phases. The evaluation committee shall comprise of TWO senior faculty members. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

Rubrics for Evaluation:

- Topic – Technical Relevance, Sustainability and Societal Concerns 15%
- Literature Review 25%
- Presentation Skills 35%
- Report 25%

Mapping of Course Outcomes (CO) to Program Outcomes (PO)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1		H	M	M	L	H	H	--	---	---	M
CO2	L	M								H	
CO3							L	M	H		
CO4		L	M		H	H					H

Mapping of Course Outcomes (CO) to Program Specific Outcomes (PSO)

	PSO1	PSO2
CO1	H	L
CO2	M	H
CO3	M	L
CO4	H	L