RV College of Engineering®

Master of Technology (M.Tech)

VLSI DESIGN & EMBEDDED SYSTEM

Scheme And Syllabus Of I & IV Semester
(2024 Scheme)

B.E. Programs : AS, BT, CH, CS, CS - AI, CS - CD, CS - CY, CV, EC, EE, ET, IM, IS, ME.
M. Tech (13) MCA, M.Sc. (Engg.)
Ph.D. Programs : All Departments are recognized as Research Centres by VTU Except AI & AS

2024

Edition

99TH
NIRF RANKING IN ENGINEERING (2024)

1501+
Times Higher Education World University Rankings (2024)

601+
Asia University Ranking 2024

EduFuture Excellence Award
Best Private Engineering University (South)
by Zee Digital

1001+
Subject Ranking (Engineering)

801+
Subject Ranking (Computer Science)

IIRF 2024
Indian Institutional Ranking Framework

NATIONAL RANK - 07
STATE RANK - 02
ZONE RANK - 04

AAA
Rating in NPTEL Local Chapter (Jan - Apr 2024)
State Ranking - 1
National Ranking - 16

CURRICULUM STRUCTURE

07 CREDITS PROFESSIONAL CORE COURSE

04 CREDITS BASIC SCIENCE

16 CREDITS INTEGRATED PROFESSIONAL CORE COURSE

24 CREDITS PROJECT WORK

04 CREDITS AEC

19 CREDITS PROFESSIONAL ELECTIVES

06 CREDITS INTERNSHIP

80 CREDITS TOTAL

*ABILITY ENHANCEMENT COURSES (AEC), UNIVERSAL HUMAN VALUES (UHV), INDIAN KNOWLEDGE SYSTEM (IKS), YOGA

17
Centers of Excellence

11
Centers of Competence

1569
Publications On SCI

440
Publications On Web Of Science

2842
Citations
Last 3 Years

70
Patents Filed

40
Patents Granted
Last 3 Years

61
Published Patents

29
Skill Based Laboratories Across Four Semesters

MOUS: 90+WITH INDUSTRIES / ACADEMIC INSTITUTIONS IN INDIA & ABROAD

₹5 crores
Sponsored Projects

₹14 crores
Consultancy Projects

RV College of Engineering®

Master of Technology (M.Tech)

VLSI DESIGN & EMBEDDED SYSTEM

Scheme And Syllabus Of I & IV Semester
(2024 Scheme)

B.E. Programs : AS, BT, CH, CS, CS - AI, CS - CD, CS - CY, CV, EC, EE, ET, IM, IS, ME.
M. Tech (13) MCA, M.Sc. (Engg.)
Ph.D. Programs : All Departments are recognized as Research Centres by VTU Except AI & AS

2024

Edition

POSTGRADUATE PROGRAMS

Sl. No	Core Department	Program	Code
1.	BT	M. Tech in Biotechnology	MBT
2.	CS	M. Tech in Computer Science & Engineering	MCE
3.	CS	M. Tech in Computer Network Engineering	MCN
4.	CV	M. Tech in Structural Engineering	MST
5.	CV	M. Tech in Highway Technology	MHT
6.	EC	M. Tech in VLSI Design & Embedded Systems	MVE
7.	EC	M. Tech in Communication Systems	MCS
8.	EE	M. Tech in Power Electronics	MPE
9.	ET	M. Tech in Digital Communication	MDC
10.	IS	M. Tech in Software Engineering	MSE
11.	IS	M. Tech in Information Technology	MIT
12.	ME	M. Tech in Product Design & Manufacturing	MPD
13.	ME	M. Tech in Machine Design	MMD
14.	MCA	Master of Computer Applications	MCA

ELECTRONICS & COMMUNICATION ENGINEERING

DEPARTMENT VISION

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering.

DEPARTMENT MISSION

1. To impart quality technical education to produce industry-ready engineers with a research outlook.
2. To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.
3. To create centers of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.
4. To develop entrepreneurial skills among the graduates to create new employment opportunities.

PROGRAMME OUTCOMES (PO)

M. Tech in **VLSI Design and Embedded Systems** graduates will be able to:

PO1: Independently carry out research/investigation and development work to solve the practical problems related to VLSI Design and Embedded Systems.

PO2: Write and present a substantial technical report/document in the field of VLSI Design and Embedded Systems

PO3: Demonstrate a degree of mastery over the area of VLSI Design and Embedded Systems. The mastery should be level higher than the requirements of bachelor's in Electronics & Communication Engineering program.

PO4: Abstract the requirements of modern microelectronics and smart systems to offer innovative solutions with available IPs and interfaces.

PO5: Design and develop VLSI and Embedded modules with good economics to meet Quality of Service.

PO6: Acquire professional and intellectual integrity, research ethics and execute socio-concern projects related to modern VLSI and Embedded Systems.

LEAD SOCIETY

Institute of Electrical and Electronics Engineers (IEEE)

INDEX

I SEMESTER M.TECH VLSI DESIGN & EMBEDDED SYSTEMS												
Sl. No.	**Course Code**	**Course Title**	**Credit Allocation**				**BoS**	**Category**	**CIE Duration (H)**	**Max Marks CIE**	**SEE Duration (H)**	**Max Marks SEE**
			L	**T/ SDA**	**P**	**Total**						
1	MVE311TA	Static Timing Analysis	3	1	0	4	EC	Theory	1.5	100	3	100
2	MVE212IA	Low Power Digital IC Design	3	0	1	4	EC	Theory+Lab	1.5	100+50	3	100+50
3	MVE313IA	Advanced Embedded System Design	3	0	1	4	EC	Theory+Lab	1.5	100+50	3	100+50
4	MXX214AX	Professional Cluster Elective Courses (Group-A)	3	1	0	4	Res BoS	Theory	1.5	100	3	100
5	MVE415DL	Design Thinking Lab	0	0	2	2	EC	Lab	1.5	50	2	50
7	HSS116EL	Technical English	0	0	1	1	HSS	Lab	1.5	50	2	50
Total Credits						**19**						

Professional Cluster Elective Courses (Group-A)			
Sl.No	**BoS**	**Course code**	**Course title**
1	EC	MCS214A1	Programming, Data Structures and Algorithms
2	ET	MDC214A2	Multimedia Communications
3	EE	MPE214A3	Electric and Hybrid Vehicles
4	EC	MVE214A4	Digital System Design with FPGA

II SEMESTER M.Tech VLSI Design & Embedded Systems												
Sl. No.	**Course Code**	**Course Title**	**Credit Allocation**				**BoS**	**Category**	**CIE Duration (H)**	**Max Marks CIE**	**SEE Duration (H)**	**Max Marks SEE**
			L	**T/ SDA**	**P**	**Total**						
1	MVE321IA	Analog IC Design	3	0	1	4	EC	Theory+Lab	1.5	100+50	3	100+50
2	MVE322IA	Physical Design	3	0	1	4	EC	Theory+Lab	1.5	100+50	3	100+50
3	MVE323BX	Program Specific Elective (Group-B)	3	1	0	4	EC	Theory	1.5	100	3	100
4	MXX324CX	Professional Cluster Elective (Group-C)	3	1	0	4	EC	Theory	1.5	100	3	100
5	MXX325DX	Interdisciplinary Courses (Global Electives) (Group-D)	3	0	0	3	EC	Theory	1.5	100	3	100
	MIM426RT	Research Methodology	2	0	0	2	IM	NPTEL	--	---	2	50
6	MVE427SL	Skill Lab	0	0	2	2	EC	Lab	1.5	50	2	50
Total Credits						**23**						

Program Specific Elective (Group-B)			
Sl.No	**BoS**	**Course code**	**Course title**
1	EC	MVE323B1	SystemVerilog for Design and Verification
2	EC	MVE323B2	RFIC Design
3	EC	MVE323B3	Semiconductor Device Modelling
4	EC	MVE323B4	Automotive Embedded Systems

Professional Cluster Elective (Group-C)			
Sl.No	**BoS**	**Course code**	**Course title**
1	EC	MCS324C1	Computer Vision with DL
2	ET	MDC324C2	Adhoc Networks
3	EE	MPE324C3	Intelligent control techniques in Electrical Drives
4	EC	MVE324C4	Semiconductor Manufacturing
Interdisciplinary Courses (Global Electives) (Group-D)			
Sl. No.	**BoS**	**Course code**	**Course title**
1	BT	MBT325DA	Nature Impelled Engineering
2	BT	MBT325DB	Clinical Data Management
3	CS	MCN325DC	Cyber Forensics and Cyber Laws
4	CV	MCV325DD	Industrial Safety and Health
5	CV	MCV325DE	Advanced Technologies for Transportation Systems
6	EC	MEC325DF	Design & Implementation of Human-Machine Interface
7	EE	MEE325DG	Electric Vehicle technology - II
8	ET	MET325DH	Electronic Navigation Systems
9	ET	MET325DJ	Vehicular Communication Ecosystem
10	IM	MIM325DK	Essentials of Project Management
11	IS	MIS325DM	User Interface & User Experience
12	MA	MMA325DN	Mathematical Methods for Data Science
13	ME	MME325DO	Industry 4.0: The Smart Manufacturing
14	ME	MME325DQ	Industrial Internet of Things (IIoT)

III SEMESTER M.Tech VLSI Design & Embedded Systems												
Sl. No.	**Course Code**	**Course Title**	**Credit Allocation**				**BoS**	**Category**	**CIE Duration (H)**	**Max Marks CIE**	**SEE Duration (H)**	**Max Marks SEE**
			L	**T/ SDA**	**P**	**Total**						
1	MVE331TA	Algorithms for VLSI Design and Automation	3	1	0	4	EC	Theory	1.5	100	3	100
2	MVE232EX	Professional Elective Course (Group-E)	2	0	0	2	EC	NPTEL	--	--	2	50
3	MVE433P	Minor Project	0	0	6	6	EC	Project	1.5	50	3	50
4	MVE434N	Internship	0	0	6	6	EC	Internship	1.5	50	3	50
Total Credits						**18**						

Professional Elective Course (Group-E) NPTEL			
Sl.No	**BoS**	**Course Code**	**Course Title**
1	EC	MVE232E1	Digital VLSI Testing
2	EC	MVE232E2	C Based – VLSI Design
3	EC	MVE232E3	VLSI Interconnects
4	EC	MVE232E4	Sensor Technologies: Physics, Fabrication, and Circuits

IV SEMESTER M.Tech VLSI Design & Embedded Systems												
Sl. No.	**Course Code**	**Course Title**	**Credit Allocation**				**BoS**	**Category**	**CIE Duration (H)**	**Max Marks CIE**	**SEE Duration (H)**	**Max Marks SEE**
			L	**T/ SDA**	**P**	**Total**						
1	MVE341FX	Program Specific Courses (Group-F)	2	0	0	2	EC	NPTEL	--	--	2	50
2	MVE442P	Major Project	0	0	18	18	EC	Project	--	100	3	100
Total Credits						**20**						

Program Specific Courses (Group-F) NPTEL			
Sl. No	**BoS**	**Course Code**	**Course Title**
1	EC	MVE341F1	VLSI Design Flow: RTL to GDS
2	EC	MVE341F2	Phase-Locked Loops
3	EC	MVE341F3	VLSI Data Conversion Circuits
4	EC	MVE341F4	Multi-Core Computer Architecture

SEMESTER: I						
STATIC TIMING ANALYSIS **(Professional Core Course)** **(Theory)**						
Course Code	**:**	**MVE311TA**		**CIE Marks**	**:**	**100 Marks**
Credit L:T:P	**:**	**3:1:0**		**SEE Marks**	**:**	**100 Marks**
Hours	**:**	**45 L +30T+45EL**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**09 Hrs**
Introduction: Basics of timing concepts, Propagation delay, slew, timing arcs, min and max timing paths, and clock domains. **Delay Concepts for Digital Designing:** Types of Delays in Digital Circuits, Different Cause for Delay **Timing parameters of digital circuits:** Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design, Clock Concepts **The STA Environment**- timing path groups, modeling of external attributes, virtual clocks, refining the timing analysis, point-to-point specification	
Unit–II	**09 Hrs**
Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitics, Interconnects, Parasitic Extraction Formats, linear v/s. non-linear delay model. **Clock Network Optimization**: Metrics, clock skew-scheduling, handling variability. **Parallel Timing Optimization**: Circuit partitioning for independent timing regions. **Post-Silicon Timing Validation**: Introduction, Sources of Post-silicon timing failure, Post-silicon tuning	
Unit–III	**09 Hrs**
Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design: Cause for Cross talk on Integrated Circuits, Crosstalk Prevention Methods	
Unit–IV	**09 Hrs**
Constraints for STA: Clock Constraints, Other Timing Constraints, External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate.	
Unit–V	**09 Hrs**
Timing Violations and Verification: Slack, Critical Path of Timing Report, Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Recovery and Removal Violation Check, Input/output Timing Path Checks, DRC Violation Check, Multi-Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Set up Violations, Techniques to Fix Hold Violations, Time borrowing.	

Course Outcomes: After completing the course, the students will be able to:

CO1	**Apply** the basic concepts of STA to evaluate the delay of the circuits, **analyze** the generated reports to identify critical issues and bottlenecks for violations, and suggest techniques to make the design meet timing.
CO2	**Analyze** cell delays from a library, calculate output slew degradation, and use wire-load information to determine net delays. Additionally,
CO3	**Design** timing constraints, such as clock constraints, external delays, and timing exceptions, and **create** the STA environment for performing timing analysis using EDA tools.
CO4	**Evaluate** timing analysis reports to detect and resolve issues like setup and hold violations, slack, crosstalk, and noise, ensuring timing closure for digital designs.

Reference Books	
1	Static Timing Analysis for Nanometer Designs: A Practical Approach, J. Bhasker, R. Chadha, 2009, Springer, ISBN:978-0-387-93819-6,978-0-387-93820-2(e-book).
2	Static Timing Analysis for VLSI circuits, R. Jayagowri, Pushpendra S. Yadav, 2nd edition, 2024, MEDTECH,A Division of Scientific International, ISBN: 978-93-87210-06-6.
3	Timing Analysis and Optimization of Sequential Circuits, Naresh Maheshwari and Sachin S.Sapatnekar,1998, SpringerScience+ Business Media, LLC, Library of Congress Cataloging-in-Publication Data, ISBN:978-1-4613-7579-1, 978-1-4615-5637-4(eBook).
4	Constraining Designs for Synthesis and Timing Analysis - A Practical Guide to Synopsys Design Constraints (SDC), Sridhar Gangadharan and Sanjay Churiwala, 2013,Springer Science +Business Media, LLC, Library of CongressCataloging-in-PublicationData, ISBN:978-1-4614-3268-5, 978-1-4614-3269-2 (eBook).

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted &each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO TESTS** will be conducted. Each test will be evaluated for 50 Marks, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. **Phase I (20) & Phase II (20) ADDING UPTO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: I						
LOW POWER DIGITAL IC DESIGN **(Professional Core Course)** **(Theory & Practice)**						
Course Code	**:**	**MVE212IA**		**CIE**	**:**	**100 + 50 Marks**
Credits: L: T: P	**:**	**3:0:1**		**SEE**	**:**	**100 + 50 Marks**
Total Hours	**:**	**45L+30P+45EL**		**SEE Duration**	**:**	**03+ 03 Hrs**

Unit-I	**09 Hrs**
Introduction to CMOS Logic: MOSFET - static & dynamic behavior, CMOS Inverter, static and dynamic behavior, Noise Margin, Components of Energy and Power. CMOS Combinational Logic Circuit Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic. Dynamic CMOS Design, Logical Effort**.** **Introduction to Low Power Design**: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches.	
Unit – II	**09 Hrs**
Arithmetic building blocks design: Data paths in digital processor architectures – Adder, binary adder, static adder, mirror adder, TG-based adder, carry bypass adder, linear and square root carry select adder, **Low Power Design at Circuit & Logic Level**: Low Power Design at Circuit level: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, pre-computation logic, Gate reorganization, signal gating.	
Unit –III	**09 Hrs**
CMOS Sequential Logic Circuit Design: Static Latches and Registers. Dynamic Latches and Registers. Pulse-Based Registers. Sense Amplifier-based registers. Pipelining concepts. **Low Power Sequential Design**: Power estimation of Flip Flops & Latches, logic encoding, state machine encoding, Bus Invert Encoding.	
Unit –IV	**09 Hrs**
Memory & Array structures design: Memory core –ROM, SRAM, DRAM, CAM. **Interconnects:** Interconnect Impact, Resistive, Capacitive and Inductive Parasitics, Crosstalk Control, Timing Issues: Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and Impact on Performance.	
Unit –V	**09 Hrs**
Low Power Design at Architecture & higher-Level Low power Architecture & Systems: Architectural level estimation & synthesis, Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power memory design. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co-design of clock network.	
Practical: 1. Static Characteristics of CMOS Inverter 2. CMOS Full adder Circuit and its analysis. 3. Delay variation of Inverter logic at different process corners. 4. Pre and Post Layout simulation of INVX2 inverter. 5. Pre and Post Layout simulation of NAND2X2 logic gate. 6. Design of DFF using transmission gate. 7. Synthesis of Modified Booth multiplier. 8. Pre and Post synthesis simulation of the 16-bit adder. 9. Performing logic equivalence checking for counter design. 10. Generation of standard delay format (.sdf), Synopsys Design Constraints (.sdc) of digital design.	

Course Outcomes: After completing the course, the students will be able to:	
CO1	Analyze transistor circuits and Low-power concepts of digital IC design.
CO2	Analyze the functionality of digital integrated circuits & systems.
CO3	Design and implement various combinational and sequential circuits of digital systems.
CO4	Evaluate the performance parameters of digital integrated circuits & systems

Reference Books	
1.	Digital Integrated Circuits: A Design Perspective, Jan M.Rabaey, Anantha Chadrakasan, Borivoje Nikolic, (2/e), Pearson 2016, ISBN-13: 978-0130909961
2.	CMOS VLSI Design, Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, 2006, Pearson Education, ISBN: 0321149017
3.	Practical Low Power Digital VLSI Design, Gary K. Yeap, 2009, Kluwer Academic Publishers, ISBN: 978- 1-4613-77778-8.
4.	Low Power Design Methodologies, Jan M. Rabaey and Massoud Pedram, 5th reprint, Kluwer Academic Publishers,2002 ISBN: 978-1-4613-5975-3.

RUBRIC FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video-based seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
4.	**LAB:** Conduction of laboratory exercises, lab report, observation, and analysis **(20 Marks)**, lab test **(10 Marks),** and Innovative Experiment/ Concept Design and Implementation (2**0 Marks)** adding up to 50 Marks.	**50**
	MAXIMUM MARKS FOR THE CIE THEORY	**150**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO Questions of 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

RUBRIC FOR THE SEMESTER END EXAMINATION (LAB)		
Q. NO.	**CONTENTS**	**MARKS**
1	Write Up	10
2	Execution	20
3	Viva	20
	TOTAL	**50**

Semester: I						
ADVANCED EMBEDDED SYSTEM DESIGN (Theory & Practice) (Professional Core Course)						
Course Code	**:**	**MVE313IA**		**CIE**	**:**	**100 + 50 Marks**
Credits: L:T:P	**:**	**3:0:1**		**SEE**	**:**	**100 + 50 Marks**
Total Hours	**:**	**45 L+30P+45EL**		**SEE Duration**	**:**	**03 + 03 Hrs**

Unit-I	**09 Hrs**
Introduction to Embedded System Design Introduction, Characteristics of Embedding Computing Applications, Concept of Real-time Systems, Challenges in Embedded System Design, Design Process: Requirements, Design, Analysis, Hardware Software Partitioning, **Embedded System Architecture** Instruction Set Architectures with examples, Memory system Architecture: Von Neumann, Harvard, caches, Virtual Memory, Memory Management, I/O subsystem: Busy wait I/O, DMA, Interrupt Driven I/O, Processor performance Enhancement: Co-Processor & Hardware Accelerators, Pipelining, Superscalar Execution, Multi-Core CPUs, CPU Power Consumption, Benchmarking Standards: MIPS, MFLOPS, Coremark	
Unit – II	**09 Hrs**
Designing Embedded System Hardware –I CPU Bus: Bus Protocols, Bus Organization, Introduction to PCI and SATA, Memory Devices, and their Characteristics: RAM, EEPROM, Flash Memory, DRAM; I/O Devices: Timers and Counters, Watchdog Timers, Interrupt, Controllers, DMA Controllers, A/D and D/A Converters	
Unit –III	**09 Hrs**
Designing Embedded System Hardware –II Programmed IO, Memory Mapped IO, Component Interfacing with Processor, Wired Interfaces: SPI, I2C, CAN, Wireless Interfaces Reset Circuits, Power Distribution Circuits, Power Budgeting, Processor Selection Criteria, FPGA-based Design, Introduction to SoCs.	
Unit –IV	**09 Hrs**
Designing Embedded System Software –I Application Software, System Software, Cross-Platform Development Process, Board Support Library, Chip Support Library, Overview of Linkers and the Linking Process, Executable and Linking Format, Mapping Executable Images into Target Embedded Systems, Linker Command Files, Secure Boot Analysis and Optimization: Execution Time, Energy & Power, Program Size; Program Validation & Verification, Embedded System Coding Standards: MISRA C 2012, Functional Safety in Automobiles, AUTOSAR	
Unit –V	**09 Hrs**
Designing Embedded System Software –II OS-based Design, Real-Time Kernel, Process& Thread, Inter Process Communications, Synchronization, Case Study: RTX-ARM/FreeRTOS, Evaluating and Optimizing Operating System Performance: Response time Calculation, Interrupt Latency, Time Loading, Memory, Loading, Case Study: Embedded Control Applications-Software Coding of a PID Controller, PID Tuning	

Practical:

Experiments on bare metal programming

1. Write an application program to interface LEDs and push buttons to GPIOs of the LPC 1857cortex M3 evaluation board and demonstrate polling-based IO operation.
2. Write Systick_handler to accurately control the delay between toggling of LEDs to support interrupt-driven IO.

3. Write a driver for ADC0 in LPC 1857 MCU. Display digital value on GLCD and demonstrate analog sensor interface. Write driver functions for ADC initialization, ADC start of conversion, reading digital value output. Develop the main function using APIs of the ADC driver to test the functionality.
4. Write I2C driver for LPC1857. Develop the following APIs to support I2C.
   uint32_t I2C_Init (void);
   uint32_t I2C_Start (void);uint32_t I2C_Stop (void);
   uint32_t I2C_Addr (uint8_t adr, uint8_t dir);uint32_t I2C_Write (uint8_t byte);
   uint32_t I2C_Read (uint32_t ack, uint8_t *byte);
5. Write driver to support LM75a digital temperature sensor through I2C. Make use of APIs developed in experiment 4 to interface LM75a to LPC 1857 MCU. Test the functionality by displaying temperature values on GLCD.
6. Write an application program to realize the FIR filter on the STM32F4 cortex M4 development board.Test the filtering operation on the signal generated from the function generator and interfaced to the STM32F4 development board. Use STM32CubeMX for HAL generation.

Experiments using RTOS

1. Create a multitasking application program to demonstrate the creation of tasks. Task1 isexpected to control the blinking of two LEDs and Task2 is to change the font and color of the textual display on GLCD concurrently. Use APIs of RL-RTX/Freertos real time kernel. Configure systick timer to generate tick interval.
2. Create a multitasking program to demonstrate task synchronization. Task1 is expected to display an LED blinking pattern and Task2 displays a textual message on GLCD. Synchronize the access of GLCD using mutex/semaphore using APIs of RL-RTX/Freertos.
3. Create a multitasking program to demonstrate event flags to synchronize task execution. Create four tasks to simulate the operation of the stepper motor driver. Use four LEDs blinking tosimulate the activation of the four output driver stages. Create another concurrently executing task to display text on GLCD. The stepper motor driver tasks are expected to run sequentially.
4. Create a multitasking program to demonstrate IPC using a mailbox. Create a task to read a digital value from ADC and send to another task executing concurrently through the mailbox. Synchronize the execution of tasks. Use APIs of RL-ARM/FreeRTOS real time kernel.
5. Create a 'Blinky' project using RL-ARM real-time Kernel to simulate the operations of a step-motor driver. Use four LEDs blinking to simulate the activation of the four output driver stages. Create other two tasks executing concurrently and competing for GLCD. The first task displays the status of LEDs blinking on GLCD and the second task displays a string with changing color of font and background. Use suitable mechanisms to protect shared resources.

Course Outcomes: After completing the course, the students will be able to	
CO1	Analyze real-world problems and identify their feasibility for embedded system solutions.
CO2	Identify the role and functionality of microcontrollers, microprocessors, memories, sensors, actuators, communication, and additional hardware & software modules in embedded applications.
CO3	Design embedded hardware to meet constraints pertaining to operational and non-operational attributes.
CO4	Develop software across different layers of the embedded system software stack, considering processor architectures, memory hierarchies, and communication interfaces for optimized performance.

Reference Books	
1.	Embedded Systems – A Contemporary Design Tool, James K Peckol, 2nd Edition, John Weily, 2019, ISBN: 978-0-471-72180-2
2.	Introduction to Embedded Systems, Shibu K V, 1st Edition, Tata McGraw Hill Education Private Limited, 2016, ISBN: 13: 978-0070678798
3.	The Intel Microprocessors, Architecture, Programming and Interfacing, Barry B.Brey, 6th Edition, Pearson Education, 2018, ISBN-10: 8131726223
4.	Technical reference manuals on PCI, SATA, FreeRTOS/RTX ARM, and Coding standards.

RUBRIC FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10),Program-specific requirements (10), Video-based seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
4.	**LAB:** Conduction of laboratory exercises, lab report, observation, and analysis **(20 Marks)**, lab test **(10 Marks),** and Innovative Experiment/ Concept Design and Implementation (2**0 Marks)** adding up to 50 Marks.	**50**
	MAXIMUM MARKS FOR THE CIE THEORY	**150**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO Questions of 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

RUBRIC FOR THE SEMESTER END EXAMINATION (LAB)		
Q. NO.	**CONTENTS**	**MARKS**
1	Write Up	10
2	Execution	20
3	Viva	20
	TOTAL	**50**

Semester: I						
PROGRAMMING, DATA STRUCTURES AND ALGORITHMS (Theory) (Professional Cluster Elective- Group A)						
Course Code	**:**	**MCS214A1**		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**09 Hrs**
Introduction to data structures: Introduction to oops concepts. Introduction to data representation, Linear Lists, Linked Representation **Algorithm Analysis:** Mathematical Background, Model, What to Analyze, Running Time Calculations.	
Unit – II	**09 Hrs**
Stack and queue: Stack and queue implementation using linear list and linked list. Stack application- Parenthesis matching, Queue application-railroad car rearrangement. **Hashing:** Hash table representation- ideal hashing, hashing with linear open addressing, hash tables with chains	
Unit –III	**09 Hrs**
Binary and other Trees: Trees, Binary Trees, Properties and Representation of Binary Trees-Formula Based Representation, Linked Representation, Common Binary Tree Operations. **Binary Search Tree (BST).** Organizing data in a BST. Inserting and deleting items in a BST.	
Unit –IV	**09 Hrs**
Priority Queues (Heaps): Model, Simple Implementations, Binary Heap, Leftist Heaps. **Graph Algorithms:** Definitions, Properties of graphs, Representation of Graphs, Shortest-Path Algorithms, Network Flow Problems, Minimum Spanning Tree, Depth-First Search, Breadth-First Search, Introduction to NP-Completeness	
Unit –V	**09 Hrs**
Searching and Sorting Techniques: Sorting Techniques: Bubble sort, Merge sort, Selection sort', Heap sort, Insertion Sort. Searching Techniques: Sequential Searching, Binary Searching, Search Trees. **Algorithm Design Techniques:** Greedy Algorithms, Divide and Conquer, Dynamic Programming, Randomized Algorithms, Backtracking Algorithms.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Illustrate the fundamental concepts of various technologies in data structures which are used in computer programs
CO2	Derive the solution by applying the acquired knowledge of classic data structures: array lists, linked lists, stacks, queues, heaps, binary trees, hash tables.
CO3	Evaluate the solution of the problems using graph algorithms to the real-world problems arising in many practical situations
CO4	Design and development of various algorithms built using different data structures knowledge to apply and engage in life–long learning.

Reference Books	
1.	Data Structures and Algorithm Analysis in C++, M. A. Weiss. 3rd Edition, Addison-Wesley, ISBN-10: 032144146X & ISBN-13: 9780321441461
2.	Data structures, Algorithms and applications in C++, Sartaj Sahani, 1st Edition, McGraw Hill; 2000, ISBN: 10:007236226X
3.	Data Structures Using C++, D.S. Malik, 2nd Edition, 2009, Cengage Learning, ISBN- 13: 978-0-324-78201-1
4.	Data Structures & Algorithms in Java, Goodrich, Goldwasser, 6th Edition, Wiley Publications , ISBN: 978-1-118-77133-4
5.	Data structures and algorithms in Java, Robert Lafore,2nd Edition, ISBN-13: 978-0672324536, ISBN- 10: 0672324539

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10) Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO Questions of 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: I						
MULTIMEDIA COMMUNICATIONS (Theory) (Professional Cluster Elective- Group A)						
Course Code	**:**	**MDC214A2**		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**09 Hrs**
Multimedia Communications: Multimedia information representation, multimedia networks, multimedia applications, network QoS and application QoS.	
Unit – II	**09 Hrs**
Standards and Protocols: JPEG (image compression) ,JPEG 2000 compression standard – development process, features, architecture, bit stream, Audio coding standards for Multimedia: Dolby, AA3, Vorbis. MPEG – 21 multimedia frame work, Protocols - RTP, RTCP, RTSP, RSVP.	
Unit –III	**09 Hrs**
Video compression: Video compression principles, video compression standards: H.261, H.263, MPEG 1, MPEG 2, and MPEG 4. DivX, Flash Video, Avi, WMV.	
Unit –IV	**09 Hrs**
Multimedia Entertainment Networks: Introduction, Cable TV networks, Satellite TV networks, Terrestrial TVnetworks. High speed PSTN access Technologies.	
Unit –V	**09 Hrs**
Digital Video Broadcasting: DVB Interoperabilities, DVB System,Baseband processing, Digital Television, Services over IP-based networks, Services, Authentication, Authorization. DVB and Internet:IP Multicast,Audio/Video streaming.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain multimedia information representation, networks and compression techniques
CO2	Analyze applications like interpersonal communication, interactive communication over the internet and entertainment networks.
CO3	Apply various coding methods and compression techniques.
CO4	Analyze and explain the various broadcasting systems.

Reference Books	
1.	Multimedia Communications, Fred Halsall, 2001, Pearson education, ISBN: 978-81-317-0994-8.
2.	Introduction to Multimedia Communications, K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, 2014, Wiley, ISBN 13 978-0-471-46742-7.
3.	Multimedia Communication Systems, K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic,, 2004, Pearson education, ISBN: 013031398X.
4.	Data Communications and Networking, Behrouz A Forouzan, 2015, 4 th Edition, McGraw Hill publication, ISBN-13:978-0-07-063414-5.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO Questions of 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: I						
ELECTRIC AND HYBRID VEHICLES (Theory) (Professional Cluster Elective- Group A)						
Course Code	**:**	**MPE214A3**		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**09 Hrs**
Introduction to EV & HEV: History of hybrid and electric vehicles, social and environmental importance of hybrid and electric vehicles, impact of modern drive -trains on energy supplies. **Conventional Vehicles:** Basics of vehicle performance, vehicle power source characterization, transmission characteristics, and mathematical models to describe vehicle performance. **EV & HEV Drive trains:** Basic concepts & components, hybrid drive-train topologies, power flow control in hybrid drive-train topologies, fuel efficiency analysis.	
Unit – II	**09 Hrs**
Electric Traction unit: Introduction to electric components used in hybrid and electric vehicles, Configuration and control of DC Motor drives, Configuration and control of Induction Motor drives, configuration and control of Permanent Magnet Motor drives, Configuration and control of Switch Reluctance Motor drives, drive system efficiency.	
Unit –III	**09 Hrs**
Energy Storage: Introduction to Energy Storage Requirements in Hybrid and Electric Vehicles, Battery based energy storage and its analysis, Fuel Cell based energy storage and its analysis, Super Capacitor based energy storage and its analysis, Flywheel based energy storage and its analysis, Hybridization of different energy storage devices. **Energy Management Strategies:** Introduction to energy management strategies used in hybrid and electric vehicles, classification of different energy management strategies, comparison of different energy management strategies, implementation issues of energy management strategies.	
Unit –IV	**09 Hrs**
Traction Motors: Design, Sizing, Thermal Analysis and Modeling. **Series and Parallel Hybrid Drive Train Design:** Operation Patterns, Control Strategies, Sizing of the Major Components, Power Rating Design of the Traction Motor, Power Rating Design of the Engine/Generator, Design of PPS, Design Example.	
Unit –V	**09 Hrs**
Design of DC-DC Converters for EV-HEV Applications: Multi-input DC-DC Converters, Multi-input converter Using High/Low Voltage Sources, Flux Additive DC-DC Converter, Bidirectional DC-DC Converters. **Case studies:** Typical converters for EV and HEV Applications.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand and explain the configuration and propulsion system of EV and HEV.
CO2	Analyse the performance EV and HEV drive trains.
CO3	Design the structure of EV and HEV.
CO4	Evaluate the PE converters performance to EV and HEV applications.

Reference Books	
1.	Mehrdad Ehsani, Yimin Gao, Sebatien Gay and Ali Emadi, "Modern Electric, Hybrid Electric and Fuel cell vehicles: Fundamentals, Theory and Design", CRC Press, 3rd Edition, 2004, ISBN: 978-1498761772.
2.	Iqbal Husain, "Electric and Hybrid Vehicles- Design Fundamentals" CRC Press, 2nd Edition, 2011, ISBN:978-1439811757.
3.	Zhang Xi , Mi Chris, "Vehicle Power Management Modeling, Control and Optimization" Springer, 1st Edition, 2011, ISBN: 978-0-85729-735-8.
4.	Mi Chris, Masrur A., and Gao D.W.," Hybrid Electric Vehicle: Principles and Applications with Practical Perspectives", Wiley Publisher, 1st Edition, 2011, ISBN:0-824-77653-5.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO Questions of 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: I						
DIGITAL SYSTEM DESIGN WITH FPGA (Theory) (Professional Cluster Elective- Group A)						
Course Code	**:**	**MVE214A4**		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**09 Hrs**
Introduction to Verilog and Design Methodology: Verilog IEEE standards, Verilog Data Types: Net, Register and Constant. Verilog Operators, Number representation and Verilog ports, Simulation and Synthesis, Test-benches. Verilog Primitives. Logic Simulation, Design Verification, and Test Methodology: Four-Value Logic and Signal Resolution in Verilog, Test Methodology Signal Generators for Test benches, Sized Numbers. Introduction to Design Methodology: Digital Systems and Embedded Systems, Real-world circuits. Design Methodology: Design Flow-Architecture.	
Unit – II	**09 Hrs**
Verilog Modelling Styles: Behavioral Modelling: Latches and Level-Sensitive Circuits in Verilog, Cyclic Behavioral Models of Flip-Flops and Latches, Behavioral Models of Multiplexers, Encoders, Decoders and Arithmetic circuits. Dataflow Modelling: Boolean Equation-Based Models of Combinational Logic, Propagation Delay and Continuous Assignments. Linear-Feedback Shift Register. Tasks & Functions. Structural Modelling: Design of Combinational Logic, Verilog Structural Models, Top-Down Design and Nested Modules. (Hands on using Xilinx Vivado tool)	
Unit –III	**09 Hrs**
Synthesis of Digital Sub-systems: Synthesis of Combinational Sub-systems: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Three-state Devices and Bus Interfaces. Synthesis of Sequential Sub-systems: Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines, Registered Logic, State Encoding, Synthesis of Implicit State Machines, Registers and Counters. (Hands on using Xilinx Vivado)	
Unit –IV	**09 Hrs**
System Implementation and Fabrics: CPLD vs FPGA Architecture - Programming Technologies-Chip I/O Programmable Logic Blocks- Fabric and Architecture of FPGA. Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture – ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture, Hardcore and Softcore FPGA. (Examples such as counter, sequence detector, sequence generator etc, implementation on FPGA board)	
Unit –V	**09 Hrs**
Processor Design and System Development: Design of Processor Architectures: Functional Units for Addition, Subtraction and Multiplication (overview). Design: Hierarchical Decomposition STG-Based Controller Design, Efficient STG-Based Sequential Binary Multiplier. Case Studies: Algorithms and Architectures for Digital Processors, Digital Filters and Signal Processors	

Course Outcomes: After completing the course, the students will be able to	
CO1	Identify different modeling styles for the various digital systems.
CO2	Verify the behavior of Digital Circuits Using Simulation and Validation Techniques.
CO3	Analyze Digital Systems and build small-scale applications using Interfacing concepts.
CO4	Demonstrate the skill of cost-effective system designs through proper selection of Implementation Fabric.

Reference Books	
1.	Advanced Digital Design With the Verilog HDL, Michael D. Ciletti, 2nd Edition, 2015, PHI, ISBN: 978–0–07–338054–4.
2.	Digital Systems Design Using Verilog, 1st Edition, 2015, Charles Roth, Lizy K. John, ByeongKil Lee,Cengage Learning, ISBN-10: 1285051076
3.	Digital Design: An Embedded Systems Approach Using VERILOG, Peter J. 1st Edition, 2010, Ashenden, Elsevier, ISBN: 978-0-12-369527-7
4.	IEEE Standard Verilog Hardware Description Language," in IEEE Std 1364-2001 , vol., no., pp.1-792, 2001, ISBN: 978-0-7381-4851-9
5.	Fundamentals of Digital Logic with Verilog Design, Stephen Brown and ZvonkoVranesic, 6th Edition, 2014, McGraw Hill publication, ISBN: 978–0–07–338054–4

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10) Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO Questions of 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: I						
DESIGN THINKING LAB (Lab)						
Course Code	**:**	**MVE415DL**		**CIE**	**:**	**50 Marks**
Credits: L:T:P	**:**	**0:0:2**		**SEE**	**:**	**50 Marks**
Hours/Week	**:**	**15 P**		**SEE Duration**	**:**	**02 Hrs**

Design thinking is a methodology which provides a solution-based approach to solving problems. It is extremely useful when used to tackle complex problems, as it serves to understand the societal needs involved, reframe the problem in human-centric ways, create numerous ideas in brainstorming sessions and adopt a hands-on approach to prototype and testing.

The 5 Stages in the Design Thinking Process:
Stage 1: Empathize—Compile Users' Needs.
Stage 2: Define—State Users' Needs and Problems.
Stage 3: Ideate—Challenge Assumptions and Create Ideas.
Stage 4: Prototype—Start to Create Solutions.
Stage 5: Test—validate the solutions obtained.

The five stages of design thinking will help students to apply the methodology to solve complex problems that occur in product designs. The broad area identified for the specialization **System Design and On-chip variation analysis.** The students are encouraged to apply the 5 stages in the Design Thinking Process to solve the problems in the area identified.

Broader Theme; System Design and On-chip variation analysis

Reference Books

1. https://onlinecourses.nptel.ac.in/noc22_mg32/preview

RUBRIC FOR CONTINUOUS INTERNAL EVALUATION (CIE-Lab)

The evaluation of the work will be carried out by the committee appointed by the Head of the department. Student/team should submit a report on the Case Studies solved under the theme.
Evaluation will be carried out in THREE Phases.

Phase	Activity	MARKS
I	Phase I	10
II	Phase II	15
III	Phase III and Draft report	15
	Final report	10
	MAXIMUM MARKS FOR THE CIE	**50**

RUBRIC FOR SEMESTER END EXAMINATION (SEE-Lab)

The evaluation will be done by Internal and External examiners through Exhibition Mode.
The following weightage would be given for the exhibition:

Q.NO.	CONTENTS	MARKS
1	Presentation through posters	15
2	Demonstration of the Prototype	25
3	Vivavoce	10
	MAXIMUM MARKS FOR THE SEE	**50**

SEMESTER: I						
TECHNICAL ENGLISH (Online English Laboratory Course) Common to all (Humanities and Social Sciences)						
Course Code	**:**	**HSS116EL**		**CIE Marks**	**:**	**50 Marks**
Credits L:T:P	**:**	**0:0:1**		**SEE Marks**	**:**	**50 Marks**
Hours	**:**	**30P**		**SEE Duration**	**:**	**2 Hrs**

Unit – I	**10 Hrs**
The Basics. Business Documents, Questions, and the Technical Pursuit. Engineering Concepts and Complexity; The Future Tense for Technical Work. White Papers; Modifiers and Qualifiers.	
Unit – II	**10 Hrs**
Making Recommendations; Interpreting Data, Ethical Persuasion for Technical Projects; Cause and Effect; Calls for Proposals. Technical Complexity in Communication. Numbers, Plain English, Jargon, and Technical Terms, Active and Passive Structures.	
Unit – III	**10 Hrs**
Organization Needs; Seeing the Big Picture; Negotiating. Audience Needs and Assessment; Standards versus White Papers; Objectivity, Communicating within Expected Genres; Identifying Trustworthy Sources or Bias in. A Review of Major Course Takeaways.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Demonstrate clarity and precision in technical communication by structuring information effectively, balancing technical terms with plain English, and adapting to diverse audiences.
CO2	Analyze and produce professional documents, such as white papers, business proposals, and reports, while applying ethical persuasion, data interpretation, and evidence-based reasoning.
CO3	Evaluate and refine communication strategies by assessing audience needs,recognizing trustworthy sources, and navigating organizational and technical complexities.
CO4	Apply critical thinking and negotiation skills to align communication with organizational goals, anticipate future challenges, and support informed decision- making.

References	
1	IEEE – EBSCO Technical English for Professionals – Online platform
2	Valerie Lambert, Elaine Murray, English for Work – Everyday Technical English, Pearson Education, 2003, ISBN- 0 582 53963-3
3	David Bonamy, Christpher Jacques, Technical English – First Course Book, Pearson Education, 2008
4	S Sumant. Technical English I, The McGraw Hill, 2011, ISBN -978 81 8209 308 9

Assessment and Evaluation Pattern (Online Mode)		
	CIE (Online Mode)	**SEE (Online Mode)**
Weightage	**50%**	**50%**
Test – I	Each test will be conducted for 50 marks adding to 100 marks. Final test marks will be reduced to 40 marks	**Final assessment will be conducted for 50 marks**
Test – II		
Experiential Learning	10 Marks	

Communication Skills- Activity based test – Script writing, Essay Writing, Role plays. Any other activity that enhances the Communication skills. The students will be assigned with a topic by the faculty handling the batch. The students can either prepare a presentation/write essay/role play etc. for the duration (4-5 minutes per student). **Parameters for evaluation of the Presentation** a. Clarity in the presentation/ Speaking/Presentation skills. b. Concept / Subject on which the drama is enacted/ scripted		
Maximum Marks	50 Marks	**50 Marks**
Total marks for the course	**50**	**50**

SEMESTER: II						
ANALOG IC DESIGN (Theory & Practice) (Professional Core Course)						
Course Code	:	**MVE321IA**		**CIE Marks**	:	**100+50 Marks**
Credits L:T:P	:	**3:0:1**		**SEE Marks**	:	**100+50 Marks**
Hours	:	**45L+30P_45EL**		**SEE Duration**	:	**03+03 Hrs**

Unit – I	**09 Hrs**
Single stage Amplifiers: Basic concepts, DC analysis, small signal analysis and noise analysis of common source and common gate stage, power, bandwidth, impedance and frequency scaling of circuits, Frequency response of CS amplifier, Cascode stage- Folded Cascode. **Current Mirror**: Basic Current Mirrors, Cascode current Mirrors, and amplifiers biased at constant currents.	
Unit – II	**09 Hrs**
Differential Amplifiers: Single-ended and differential operation, Common mode response, differential pair with active loads, Gilbert cell **Operational Amplifier:** One-stage op-amp, two-stage op-amp, Telescopic Cascode opamp, Telescopic Cascode opamp frequency response, Folded Cascode op-amp-dc gain, Telescopic and folded Cascode opamp, PSRR, Two stage opamp-topology, Gain boosting, common mode feedback.	
Unit – III	**09 Hrs**
Noise: Resistors, MOSFET, Input and output referred noise, basic amplifier stages – CS and CGstage **Stability analysis and Frequency compensation:** Stability of Feedback: Basic Concepts, Instability and the Nyquist Criterion. Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation.	
Unit – IV	**09 Hrs**
Band gap reference: Band gap reference, Constant current and constant gm bias generators, reducing supply sensitivity **Low dropout regulators:** Basic requirements and constraints. **Phase Locked Loops:** Simple Phase locked loop, Charge pump PLL, Non-ideal effects - Jitter & Phase noise, Applications.	
Unit – V	**09 Hrs**
Digital-to-Analog Converter Specification, Analog-to-Digital Converter Specifications. **DAC Architectures:** Resistor String, R-2R Ladder networks, Current Steering. **ADC Architectures:** Flash ADC, Pipeline ADC, Successive Approximation ADC.	

Practical:

1. Study of DC and small signal models of a MOS Transistor
2. Design of MOS current sources and mirrors
3. Design of single-stage amplifiers – CS Amplifier with different loads
4. Design of a MOS Differential amplifier with an active load
5. Design of a cascode amplifier, double cascode and triple cascode amplifier
6. Design of Telescopic opamp
7. Design of a 2-stage CMOS Op-Amp
8. Design of Band Gap Reference circuit
9. Post-layout simulation of CS Amplifier
10. Post-layout simulation of Differential Amplifier

Course Outcomes: After going through this course the student will be able to	
CO1	Apply the knowledge of MOSFET & amplifiers to investigate various design trends of analog IC design
CO2	Analyze the functionality of analog/mixed-signal circuits & systems
CO3	Design and implement analog integrated circuits & systems
CO4	Evaluate the different performance parameters of analog/mixed-signal integrated circuits

Reference Books	
1.	Design of Analog CMOS Integrated Circuits, Behzad Razavi, McGraw Hill Edition, 2002, ISBN: 0-07-238032-2
2.	CMOS Circuit Design, Layout and Simulation, R. Jacob Baker, Harry W. Li and David E. Boyce, IEEE Press, 2002, ISBN: 81-203-1682-7
3.	Analysis and design of Analog Integrated Circuits, Gray, Hurst, Lewis, and Meyer: 4th Edition, John Wiley & Sons, ISBN-10: 0470245999
4.	CMOS Analog Circuit Design, Phillip E. Allen and Douglas R. Holberg, 2nd Edition Oxford University Press, February 2002, ISBN: 9780199765072

RUBRIC FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video-based seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
4.	**LAB:** Conduction of laboratory exercises, lab report, observation, and analysis **(20 Marks)**, lab test **(10 Marks),** and Innovative Experiment/ Concept Design and Implementation (2**0 Marks)** adding up to 50 Marks.	**50**
	MAXIMUM MARKS FOR THE CIE THEORY	**150**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

RUBRIC FOR THE SEMESTER END EXAMINATION (LAB)		
Q. NO.	**CONTENTS**	**MARKS**
1	Write Up	10
2	Execution	20
3	Viva	20
	TOTAL	**50**

Semester: II						
PHYSICAL DESIGN (Theory & Practice) (Professional Core Course)						
Course Code	**:**	**MVE322IA**		**CIE**	**:**	**100 + 50 Marks**
Credits: L:T:P	**:**	**3:0:1**		**SEE**	**:**	**100+ 50 Marks**
Total Hours	**:**	**45L +30P+45EL**		**SEE Duration**	**:**	**03 + 03 Hrs**

Unit-I	09 Hrs
Introduction Review of Combinational & Sequential Logic circuits, VLSI design Flow, Verilog/VHDL basics, CMOS logic structures. **Sequential Logic Synthesis** Introduction, Basics of FSM concept, Describe logic synthesis process, Explain procedure involved in logic synthesis of combinational and sequential circuits, Classify multilevel logic synthesis and technology mapping, Clocking strategies.	
Unit – II	**09 Hrs**
Floorplan Technology File, Circuit Description, Design Constraints, Design Planning, Power Planning, Macro Placement, Clock Planning **Placement** Global Placement, Detail Placement.	
Unit –III	**09 Hrs**
Clock tree synthesis, Power Analysis. **Routing** Global Routing, Detail Routing **RC Extraction** Resistance extraction, Capacitance extraction, Inductance and impedance (RLC) extraction.	
Unit –IV	**09 Hrs**
UPF fundamentals, concepts of Logic Equivalence Check (LEC) and Design Low Power Checks (CLP). **Static Timing Analysis** Foundry Library; Liberty format, Gates: Propagation Delays, Flops: Propagation Delay, Setup time, hold Time, contamination delay, Recovery time, Removal time, Clock frequency, Jitter, Skew(source & network latency), Timing Paths, Multi-input path, Clock Budget, Multi-Clock, Multi-Cycle Path, False Path, Retiming	
Unit –V	**09 Hrs**
Physical Verification CMOS circuit and layout design , LVS, DRC, lambda based Design Rules, Stick Diagrams, Study of CMOS Technologies and Layout Compaction, Study of Antenna Rules, Layer Density Rules, Resolution Enhancement Rules. **Design For Testing** Introduction to Testing – Fault Modelling and Simulation, Functional Test, Scan Test, Boundary Scan Test (IEEE 1149.1), Parametric Test, Current and Very Low-Level Voltage Test, Wafer Acceptance Test, Memory Built-In -Self-Test (MBIST), Parallel Module Test.	

Practical:

1. Write register transfer logic level code using Verilog for combinational and sequential digital systems.
2. Analyse combinational and sequential logic circuits by simulating.
3. Write Constraints and Perform logic synthesis of Verilog logic designs.
4. Generate the synthesized netlist and analyse critical path delay, area, power, and performance of the digital system.
5. Perform Low Power checks (CLP) & Logic Equivalence Checks (LEC) using the design (RTL/Netlist)
6. Perform physical design flow: Use floorplan, placement, clock tree synthesis and routing steps.
7. Back annotation: Extract resistance, capacitance, inductance and simulate the design.
8. Static timing analysis checks: Setup/Hold/Max_Transition/Max_Cap/Noise/Cross Talk/Min_Pulse_Width
9. Physical Verification checks: DRC/ERC/SOFT/LVS/ANTENNA/DENSITY
10. Design For Test: Scan Insertion, ATPG, MBIST, BSCAN implementation and verification

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply the principles of physical design, including floor planning, placement, and routing, to create efficient and reliable integrated circuits, utilizing industry-standard design tools.
CO2	Analyze the performance of integrated circuits through static timing analysis and RC extraction, identifying and resolving issues related to timing paths, clock skews, and power consumption.
CO3	Create optimized floorplans, placements, and clock distribution networks by leveraging power planning, macro placement, and clock tree synthesis techniques for high-performance designs.
CO4	Evaluate the effectiveness of physical verification techniques such as DRC, LVS, and antenna rule checks, ensuring design integrity and compliance with CMOS technology standards.

Reference Books	
1.	Physical Design Essentials: An ASIC Design Implementation Perspective, Khosrow Golshan, 1st Edition, Springer, ISBN-10: 44194219X, ISBN-13: 978-1441942197.
2.	Static Timing Analysis for Nanometer Designs, J. Bhashkar and Rakesh Chadha, 2009 Edition, Springer-Verlag New York Inc, ISBN-10:0387938192, ISBN-13:978- 0387938196.
3.	CMOS Digital Integrated Circuits Analysis and Design, Sung-Mo Kang and Yusuf Leblebici, 41st Edition, December 2002, McGraw-Hill Higher Education, ISBN-10: 9780071243421 ISBN-13: 978-0071243421.
4.	Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer, and A. D.Friedman, Computer Science Press, 1990, ISBN: 0-7167-8179-4.

RUBRIC FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video-based seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
4.	**LAB:** Conduction of laboratory exercises, lab report, observation, and analysis **(20 Marks)**, lab test **(10 Marks),** and Innovative Experiment/ Concept Design and Implementation (2**0 Marks)** adding up to 50 Marks.	**50**
	MAXIMUM MARKS FOR THE CIE THEORY	**150**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

RUBRIC FOR THE SEMESTER END EXAMINATION (LAB)		
Q. NO.	**CONTENTS**	**MARKS**
1	Write Up	10
2	Execution	20
3	Viva	20
	TOTAL	**50**

Semester: II						
SYSTEMVERILOG FOR DESIGN AND VERIFICATION (Professional Basket course- Group B) (Theory)						
Course Code	**:**	**MVE323B1**		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**09 Hrs**
Introduction to SystemVerilog as a Verification Language: SystemVerilog standards, SystemVerilog key enhancements for hardware design. Advantages of System Verilog over Verilog, System Verilog data types, Integer Data Type: 2 - State Data types, 4 - State data types, Non-Integer Type, Enumerated data types, User Defined data types, Struct data types, Interfaces, Packages. Type Conversion: Dynamic casting, Static Casting, Strings, Memories: Arrays, Dynamic Arrays, Multidimensional Arrays, Packed Arrays, Associative Arrays, Queues, Array Methods, Tasks and Functions: Verilog Tasks and Functions, Enhancements in S.V, Void Functions, Return Statement, Passing Arguments, Arguments Passing by Name, Default Arguments, Passing Arguments by Value, Passing Arguments by Reference.	
Unit – II	**09 Hrs**
OOPs Concepts, Inheritance, Constrained Randomization & Threads and Inter-process Communication: **OOP Concepts:** Overview of Classes, Properties and Methods in the Classes, Instance/Object Creation, New Constructor, Null Object handles, Accessing Members, this Keyword, Creating an Object, Objects Assignments, Copying an Object: Shallow Copy, Deep Copy. **Inheritance:** Concept of Inheritance, Super Keyword, Static properties, Overriding Methods, Polymorphism - $cast, Virtual Classes, Parameterized Classes. **Constrained Randomization:** Random Variables - rand and randc, Randomize( ) Method - Pre/Post Randomize( ) methods, Constraints in the class, Rand_mode and constraint_mode, Constraint and Inheritance, Constraint Overriding, Set Membership, Distribution Constraints, Conditional Constraints - implication (->) if/else, Inline Constraints. **Threads and Inter-process Communication:** Threads, Fork-Join/Join_any/Join_none, Inter Process Communication, Communication Building a Testbench with Threads and IPC.	
Unit –III	**09 Hrs**
Testbench building and Connecting to DUT: Verilog interface signals - Limitations of Verilog interface signals, SystemVerilog interfaces, SystemVerilog port connections, Interface instantiation, Interfaces Arguments, Interface Modports, Interface References, Tasks and functions in interface, Verilog Event Scheduler, SystemVerilog Event Scheduler, Clocking Block, Input and Output Skews, Typical Testbench Environment.	
Unit –IV	**09 Hrs**
SystemVerilog Coverage and Assertions: Cover groups, cover points, cover point bins and labels, cross coverage, cover group options, coverage capabilities. Assertion definition, assertion benefits, system Verilog assertion types, immediate assertions, concurrent assertions, assert and cover properties and labels, overlapping and non-overlapping implications, assertion and coverage examples. Case Studies.	
Unit –V	**09 Hrs**
Universal Verification Methodology: Introduction to Universal Verification Methodology, Overview of UVM Base Classes and Simulation Phases in UVM and UVM macros. UVM environment structure, Connecting DUT and Testbench. Case Studies.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explore the behavior of different digital blocks using SystemVerilog.
CO2	Apply the SystemVerilog verification features for effective and efficient verification.
CO3	Analyze the system through Coverage and Assertion-based verification.
CO4	Develop Verification Environment for Digital System.

Reference Books	
1.	SystemVerilog for Verification-A Guide to Learning the Testbench Language Features, Chris Spear, Greg Tumbush, 3rd edition, 2014, Springer New York, ISBN 978-1-4899-9500-1
2.	RTL Modeling with SystemVerilog for Simulation and Synthesis Using SystemVerilog for ASIC and FPGA, Stuart Sutherland, Sutherland HDL, Incorporated, ISBN-9781546776345, 1546776346, 2017.
3.	IEEE Standard for SystemVerilog--Unified Hardware Design, Specification, and Verification Language, IEEE, vol., no., pp.1-1354, 2024, doi: 10.1109/IEEESTD.2024.10458102.
4.	The UVM Primer-A Step-By-Step Introduction to the Universal Verification Methodology, Ray Salemi, Boston Light Press, 2013, ISBN:9780974164939, 0974164933
5.	System Verilog Functional Verification, Sasan Iman, McGraw-Hill Publishing Co. ISBN-13 :978-00714890

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

Semester: II						
RFIC DESIGN (Professional Basket course- Group B) (Theory)						
Course Code	**:**	**MVE323B2**		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Basic concepts in RF design: Units in RF design, Nonlinearity and Time Variance, Effects of nonlinearity – harmonic distortion, gain compression – 1 dB compression point, desensitization, blocking, cross modulation, intermodulation – third intercept point, cascaded nonlinear stages – IM spectra in a cascade. Noise in RF circuits - Representation of noise in circuits – input-referred noise, Noise figure, Noise figure of cascaded stages, Noise figure of lossy circuits, Sensitivity, dynamic range – spurious free dynamic range (SFDR).	
Unit – II	**09 Hrs**
Transceiver architectures: channel selection and band selection, Heterodyne – constant LO and constant IF down conversion, problem of image, image rejection vs channel selection, dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, issues in homodyne receivers, Image Reject – Hartley & Weaver architecture. Transmitter architectures - Direct conversion and two-step transmitters. Review of two port parameters and their significance.Nanoscale MOSFETs - Parasitic resistances (Rs, Rd, Rg), parasitic capacitances (Cgs, Cgd,), simplified and extrinsic small-signal models. High-frequency figures of merit: f_T and f_{MAX}.	
Unit –III	**09 Hrs**
Matching networks: Passive RLC circuits, impedance transformation – Quality factor, series to parallel conversion, basic matching networks- L, Pi-match networks – design example. Low noise Amplifier - Performance parameters, Problem of Input matching, CS stage with inductive load, Cascode CS stage with inductive degeneration (MOSFET circuits only), Noise figure calculation, Amplifier bandwidth extension techniques, Millimeter Wave LNAs.	
Unit –IV	**09 Hrs**
Mixer: Performance parameters, Mixer noise figures, single-balanced and double-balanced (active and passive) – working (MOSFET circuits only), Millimeter Wave Mixers. Oscillators - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, three-point oscillators, (MOSFET circuits only), Ring oscillators.	
Unit –V	**09 Hrs**
Phase Locked Loops: Basic concepts - Phase detector, Type I PLL, Dynamics of simple PLL, Drawbacks of simple PLL, Type II PLLs - PFD, charge pump, charge pump PLL, PFD/CP Nonidealities (concepts only) – Up and Down Skew and Width Mismatch, Charge Injection and clock feedthrough.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Investigate the functionality of a typical RF system.
CO2	Analyse CMOS circuits and their impact on Radiofrequency and Millimeter Wave IC design.
CO3	Design and implement various circuit blocks for RF transceiver chains with specifications.
CO4	Evaluate the different performance parameters used in RF design using CAD tools.

Reference Books	
1	RF Microelectronics, Behzad Razavi, 2nd Edition Pearson Education, 2012, ISBN: 13: 9780137134731
2	The Design of CMOS Radio Frequency Integrated Circuits, Thomas H Lee, 2nd Edition, Cambridge University Press, 2004, ISBN: 9780511817281
3	Radio Frequency Integrated Circuits Design, John Rogers, Calvin Plett Artech House, 2003, ISBN 1-58053-502-x

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
SEMICONDUCTOR DEVICE MODELLING (Professional Cluster course- Group B) (Theory)						
Course Code	**:**	**MVE323B3**		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Charge Carriers and Transport Modelling Crystal Structure, Semiconductor Models, Carrier Properties, State and Carrier Distributions, Equilibrium Carrier Concentrations, Drift, Diffusion, Recombination-Generation, Equations of State, Modelling & Simulation examples.	
Unit – II	**09 Hrs**
PN Junction Diodes: pn Junction Electrostatics, Preliminaries, Quantitative Electrostatic Relationships, I-V Characteristics, The Ideal Diode Equation, Deviations from the Ideal, Small-Signal Admittance, Reverse-Bias Junction Capacitance, Forward-Bias Diffusion Admittance, MS Contacts and Schottky Diodes, Solar cells and LEDs.	
Unit –III	**09 Hrs**
BJT: Electrostatics, Performance Parameters, Ideal Transistor Analysis, General Solution, Simplified Relationships, Ebers-Moll Equations and Model, Deviations from the Ideal, Modern BJT Structures.	
Unit –IV	**09 Hrs**
MOS: Electrostatics, Capacitance-Voltage Characteristics, Quantitative I_D/V_D Relationships, Square-Law Theory, Bulk-Charge Theory, ac Response, Small-Signal Equivalent Circuits, Cutoff Frequency, Small-Signal Characteristics	
Unit –V	**09 Hrs**
Emerging electron devices (Qualitative approach): Introduction, HEMT, HBT, Fin-FET. Nanowire-FET, quantum and molecular devices, energy storage, and harvesting Electronics devices	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Apply semiconductor models to analyze carrier densities and carrier transport.
CO2:	Analyze basic governing equations to analyze semiconductor devices.
CO3:	Design the p-n junction, Schottky barrier diodes, and emerging semiconductor devices.
CO4:	Model & Simulate microelectronic devices using software tools.

Reference Books	
1	Semiconductor Device Fundamentals, Robert F. Pierret, 2006, Pearson, ISBN 9780201543933
2	Operation and modeling of the MOS Transistor, Y.P. Tsividis, Colin McAndrew, 3rd Edition, 2014, Oxford Univ Press, ISBN:978-0195170153.
3	Fundamentals of Modern VLSI Devices, Yuan Taur ,Tak H. Nin 2nd edition, 2013 Cambridge University Press, ISBN: 978-1107635715.
4	Semiconductor Simulation Tools, "https://nanohub.org/roups/semiconductors"

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester – II						
AUTOMOTIVE EMBEDDED SYSTEM DESIGN (Professional Cluster course- Group B) (Theory)						
Course Code	**:**	**MVE323B4**		**CIE**	**:**	**100 Marks**
Credits: L: T: P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Automotive Systems Overview: Automotive Vehicle Technology, Overview of Vehicle Categories, Various Vehicle Sub Systems like Chassis, Body, Driveline, Engine technology, Fuelling technology, vehicle Emission, Brakes, Suspension, Emission, Doors, Dashboard instruments, Wiring Harness, Safety & Security, Comfort &Infotainment, Communication & Lighting, Future Trends in Automotive Embedded Systems: Hybrid Vehicles, Electric Vehicles.	
Unit – II	**09 Hrs**
Automotive Sensors and Actuators: Automotive Control System Applications of Sensors and Actuators. **Sensors:** Air Flow Sensor, Engine Crankshaft Angular Position Sensor, Throttle Angle Sensor, Temperature Sensor, Sensors for Feedback Control, Sensors for Driver Assistance System: Radar, Lidar, Video Technology. **Actuators:** Solenoids, Piezo Electric Force Generators, Fluid mechanical Actuators, Electric Motors and Switches.	
Unit –III	**09 Hrs**
Automotive Control System Design-I: Digital Engine Control, Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System.	
Unit –IV	**09 Hrs**
Automotive Control System Design-II: Cruise Control System, Cruise Control Electronics, Anti-locking Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering, ADAS Systems, Autonomous Vehicles, Application of IoT in automotive	
Unit –V	**09 Hrs**
Automotive Protocols: LIN, MOST, Flex Ray, Test, Calibration and Diagnostics tools for networking of electronic systems like ECU Software and Testing Tools, ECU Calibration Tools, Vehicle Network Simulation, Advanced Trends in Automotive Electronics: AUTOSAR Architecture.	

Course Outcomes (CO): After completing the course, the students will be able to	
CO1	Understand the fundamentals of different Automotive Systems.
CO2	Integrate various sensors and actuators into automotive systems, and understand their functionalities in vehicle control and monitoring.
CO3	Design control systems specifically applied to automotive engineering, including engine control, transmission control, chassis control, and vehicle dynamics control.
CO4	Provide technical embedded solutions for the development of automotive Systems.

Reference Books	
1.	Understanding Automotive Electronics-An Engineering Perspective, William B. Ribbens, 7th Edition, Butterworth-Heinemann Publications.
2.	Automotive Electronics Handbook, Robert Bosch, 2004, John Wiley and Sons, ISBN-0471288357
3.	Automotive Control Systems for Engine Driveline and Vehicle, Kiencke, Uwe, Nielsen, Lars, 2nd Edition, Springer Publication.
4.	Vehicle Safety Communications: Protocols, Security and Privacy, Tao Zhang, Luca Delgrossi, Wiley Publication.
5.	Automobile Electrical and Electronic Systems, Tom Denton, 4th Edition, Routledge, 2012.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10) Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
COMPUTER VISION WITH DL **(Professional Cluster Course- Group C)** **(Theory)**						
Course Code	**:**	**MCS324C1**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Image Formation Models: Introduction: Overview and Applications. Image formation: Digital images for representing 2D, 3D, and moving objects. The human eye and digital camera models.Photometric information: Colour: Physics of Colour, human perception of Colour, Colour models (RGB, HSI).Geometric-information: Representing points, lines, planes, surfaces, and shapes in 3D, nature and structure of medical images. Two-dimensional and three-dimensional geometric transformations of images and 3D scenes	
Unit – II	**09 Hrs**
Image Processing: Image Processing: Point operators, Linear filtering, Fourier Transform, Geometric transformation. Image filtering: Gray-level transformations, histograms, convolution, noise reduction, spatial and Fourier domain filtering and convolution, Gaussian filtering, and image resolution pyramids. Using Open CV: Smoothing Images, Median Filter, Gaussian Filter, Bilateral Filter, Changing the Shape of Images, Thresholding, Calculating Gradients, Performing Histogram Equalization	
Unit –III	**09 Hrs**
Features Detection and Classification: Feature detection and matching: gradient vector, Canny's edge detection, Harris-corner detector. Contours: Model fitting, Total LSE, Least Median Square Error. RANSAC, Hough transform. Image stitching, clustering techniques, K-mean clustering, PCA**,** Using Open CV: RANSAC Algorithm, SIFT Algorithm	
Unit –IV	**09 Hrs**
Image-based rendering: Image classification using Artificial Neural Networks and CNN, View- dependent texture maps, Application: Photo Tourism. Video-based rendering, Video-based animation, Video textures Application: Animating pictures	
Unit –V	**09 Hrs**
Real time use cases: Computer Vision Methods for Video Content Analysis: Object detection, Face detection, Pedestrian detection, Face recognition, Eigenfaces, Active appearance and 3D shape models, Application: Personal photo collections. Instance recognition, Geometric alignment, Large databases**,** Application: Location recognition, Recognition databases and test sets	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explore and acquire knowledge on fundamentals of Computer Vision concepts.
CO2	Analyze and interpret the inherent difficulties encountered in Computer Vision.
CO3	Apply Computer Vision techniques to solve problems in the visible world around us.
CO4	Evaluate and draw inferences by processing Images in real-time applications.

Reference Books	
1.	Computer Vision: Algorithms and Applications, Richard Szeliski, Springer Verlag, 2013 Edition, ISBN-13: 978-1848829343, ebook:http://szeliski.org/Book/
2.	Practical Machine Learning and Image Processing: For Facial Recognition, Object Detection, and Pattern Recognition Using Python, Himanshu Singh, 1st Edition, Apress, ISBN:978-1-4842- 4149-3
3.	Computer Vision: A Modern Approach, David Forsyth and Jean Ponce, 2nd edition, 2015, Pearson Education India, ISBN-10: 9332550115, ISBN-13: 978-9332550117
4.	Introductory Computer Vision, Imaging Techniques and Solutions, Adrian Low, 2nd Edition, 2010, BS Publications, ISBN-13 9788178001977.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10) Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
ADHOC NETWORKS **(Professional Cluster Course- Group C)** **(Theory)**						
Course Code	**:**	**MDC324C2**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Introduction: Introduction to Cellular and Ad hoc wireless networks, Applications of ad hoc networks, Issues in ad hoc wireless networks, Medium access scheme, Routing, Multicasting, Transport layer protocols, Pricing scheme, Quality of Service provisioning, Self-organization, Security, Address and security discovery, Energy management, Scalability.	
Unit – II	**09 Hrs**
MAC Protocols: Issues in designing a MAC Protocol for ad hoc wireless networks, design goalsof a MAC Protocol for Ad Hoc Wireless Networks, Classification of MAC Protocols, Contention based Protocols, Contention based Protocols with Reservation mechanism, Contention Based MAC Protocols with Scheduling Mechanisms	
Unit –III	**09 Hrs**
Routing Protocols: Design issues and classification, Table-driven, On-demand and Hybrid routing protocols, Routing protocols with efficient flooding mechanisms, Hierarchical and Power-aware routing protocol.	
Unit –IV	**09 Hrs**
Multicast Routing Protocols : Design issues and operation, Architecture reference model, Classification, Tree-based and Mesh based protocols, Energy-Efficient multicasting, Multicastingwith Quality-of-Service guarantee, Application dependent multicast routing.	
Unit –V	**09 Hrs**
Quality of Service and Security Issues : Issues and challenges in providing QoS, Classification ofQoS solutions, MAC layer solutions, Network layer solutions, QoS frameworks, Network security issues. Energy Management: Need, Classification of battery management schemes, Transmission power management schemes, System power management schemes.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the fundamental of ad hoc wireless networks and cellular networks.
CO2	Analyze contention-based MAC protocols and routing protocols for ad hoc networks
CO3	Analyze the design aspects and the limitation of the Multicast routing Protocols
CO4	Evaluate the performance of ad hoc networks using quality of service and Energy management

Reference Books	
1.	C. Siva Ram Murthy, B. S. Manoj, Ad-Hoc Wireless Networks: Architectures and Protocols, 2012,1st Edition, Prentice Hall, New Jersey. ISBN- 978-81-26547-86-9.
2.	C-K. Toh, AdHoc Mobile Wireless Networks: Protocols and Systems, 2011, 1st Edition, PrenticeHall, New Jersey. ISBN- 978-01-30078-17-9
3.	Mohammad Ilyas, The Handbook of AdHoc Wireless Networks, 2012, 1st Edition, CRC press,Florida. ISBN -978-03-67248-26-0
4.	Minoru Etoh, Next Generation Mobile Systems 3G and Beyond, 2011, 1st Edition, WileyPublications, NewJersey. ISBN: 978-04-70091-51-7

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
INTELLIGENT CONTROL TECHNIQUE IN ELECTRICAL DRIVES (Professional Cluster Course- Group C) (Theory)						
Course Code	**:**	**MPE324C3**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Fuzzy Logic Systems: Introduction to fuzzy logic, fuzzy Vs crisp set, linguistic variables, membership functions, fuzzy sets and operations on crisp sets and fuzzy sets, Fuzzy relations, operations on fuzzy relation, Cartesian Product of Relation. linguistic variables, fuzzy if then rules, compositional rule of inference, Fuzzy Rule Base and Approximate Reasoning	
Unit – II	**09 Hrs**
Fuzzy Logic Control: Basic concept of fuzzy logic control, relationship to PI, PD and PID control, design of FLC: determination of linguistic values, construction of knowledge base, inference engine, tuning, fuzzification, De-fuzzification methods. Fuzzy Inference Systems (FIS), Construction and Working Principle of FIS, Mamdani FIS models, Takagi-Sugeno-Kang (TSK) fuzzy models and concept of Adaptive Fuzzy control, Examples applicable to Drives.	
Unit –III	**09 Hrs**
Neural network: Fundamental Concept, history and development of neural network principles, Biological Neural Network, Comparison Between Biological Neuron and Artificial Neuron, Important Terminologies of ANN. Basic Models and Advantages of Neural Networks. **Learning methods:** types of learning, supervised, unsupervised, reinforced learning, knowledge representation and acquisition **Theory, architecture and learning algorithm of neural network models:** McCulloc model, Hopfield model, Perceptron Network, Back propagation network.	
Unit –IV	**09 Hrs**
Neural Networks for feedback Control: Identification of system models using neural networks, Model predictive control, feedback linearization and model reference control using neural networks, Neural Network Reinforcement Learning Controller, Radial basis function neural networks, Basic learning laws in REF nets, Recurrent back propagation, CMAC networks and ART networks, Kmeans clustering algorithm. Kohnen's feature maps, pattern recognition & mapping, Examples applicable to Drives.	
Unit –V	**09 Hrs**
Hybrid algorithms: Neuro-fuzzy systems, ANFIS and extreme-ANFIS, derivative free optimization methods. **Genetic algorithms:** introduction, principle of natural selection, Flow chart of simple genetic algorithm, GA operators and parameters. Particle swarm optimization, Solution of typical control problems. Case studies on Application to Electrical Drives.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the concepts ANN and Fuzzy Logic.
CO2	Analyze the techniques involved in ANN and fuzzy logic applications.
CO3	Design and model hybrid system with ANN and FL or independent system.
CO4	Apply techniques in modern industrial drives and power electronics system.

Reference Books	
1.	Dr. S. N. Sivanandam and Dr. S. N. Deepa, "Principles of Soft Computing", WILEY publication, 2nd Edition, 2008, ISBN: 9788126527410.
2.	John Yen and Reza Langari, "Fuzzy Logic – Intelligence, Control and Information", Pearson Education Inc, 3rd Edition, 2009, ISBN 978-81-317-0534-6.
3.	Simon Haykin, "Neural Networks – A Comprehensive Foundation", PH Publisher, 2nd Edition, 1998, ISBN:978-81-203-2373-5.
4.	Timothy J. Ross., "Fuzzy Logic with Engineering Applications", John Wiley and Sons, 3rd Edition, 2011, ISBN: 978-0-470-74376-8.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10) Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
SEMICONDUCOR MANUFACTURING (Professional Cluster Course- Group C) (Theory)						
Course Code	**:**	**MVE324C4**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
An Introduction to Microelectronic Fabrication: Semiconductor Substrates, Crystallography and Crystal Structure, Crystal Defects, Czochralski Growth, Bridgman Growth of GaAs, Float Zone Growth, Wafer Preparation and Specifications	
Unit – II	**09 Hrs**
Hot Processing and Ion Implantation: Diffusion, Fick's Diffusion Equation in One Dimension, Atomistic Models of Diffusion, Analytic Solutions of Fick's Law, Diffusion Coefficients for Common Dopants, Analysis of Diffused Profiles, Diffusion in SiO2, Simulations of Diffusion Profiles	
Unit –III	**09 Hrs**
Thermal Oxidation: The Deal–Grove Model of Oxidation, The Linear and Parabolic Rate Coefficients, The Initial Oxidation Regime, The Structure of SiO2, Oxide Characterization, The Effects of Dopants During Oxidation and Polysilicon Oxidation, Silicon Oxynitrides, Alternative Gate Insulators, Oxidation Systems, Numeric Oxidations	
Unit –IV	**09 Hrs**
Resistivity: Two-Point Versus Four-Point Probe, Wafer Mapping, Resistivity Profiling, Contactless Methods, Conductivity Type,Contact Resistance and Schottky Barriers, Metal-Semiconductor Contacts, Contact Resistance, Measurement Techniques, Schottky Barrier Height,Comparison of Methods	
Unit –V	**09 Hrs**
Statistical Process Control: Statistics Review: Distributions & Estimation, Hypothesis Tests and Control Chart, Control Charts, Advanced Control Charts, Nested Variance, Experimental Design	

Course Outcomes: After completing the course, the students will be able to	
CO1	Acquire the concepts of fabrication process and characterization techniques of IC technology.
CO2	Analysis of different process parameters in IC fabrications.
CO3	Define different standard operating procedure in IC fabrication.
CO4	Evaluate different analytic techniques in fabrication process.

Reference Books	
1.	Stephen A. Campbell, "Fabrication Engineering at the Micro and Nanoscale", Third Edition, University of Minnesota, Oxford University Press, 2008.
2.	Dieter K. Schroder, "Semiconductor Material and Device Characterization", Wiley - IEEE, 2006.
3.	Yuan Taur, Tak H. Ning, "Fundamentals of Modern VLSI Devices", 2nd edition , 2013 Cambridge University Press, ISBN: 978-1107635715.
4.	Richard Jaeger, "Introduction to Microelectronic Fabrication": Volume 5, Modular Series on Solid State Deviced, 13 November 2001.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
NATURE IMPELLED ENGINEERING (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MBT325DA**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Bio-Inspired designs-biomimetics: Termites; Sustainable buildings, Insect foot adaptations for adhesion. Bees and Honeycomb Structure. Namib Desert Beetle; Harvesting desert fog- Nature's water filter. Biopolymers, Bio-steel, Bio-composites, multi-functional biological materials. Antireflection and photo-thermal biomaterials, Invasive and non-invasive thermal detection inspired by skin	
Unit – II	**09 Hrs**
Plant inspired Technologies: Photosynthesis and Photovoltaic cells, Bionic/Artificial leaf. Lotus leaf effect for super hydrophobic surfaces. Flectofin®, a new façade-shading system inspired by flower of the Bird-of-Paradise (Strelitzia reginae). Robotic Solutions Inspired by Plant Root	
Unit –III	**09 Hrs**
Bio-Inspired technologies for medical applications: Organ system- Circulatory- artificial blood, artificial heart, pacemaker. Respiratory- artificial lungs. Excretory- Artificial kidney and skin. Artificial Support and replacement of human organs: artificial liver and pancreas. Total joint replacements- artificial limbs. Visual prosthesis -artificial / bionic eye.	
Unit –IV	**09 Hrs**
Bio-Inspired driven technologies for industrial applications: Biosensors: Artificial tongue and nose. Biomimetic echolation. Insect foot adaptations for adhesion. Thermal insulation and storage materials. Bio-robotics.	
Unit –V	**09 Hrs**
Bio-inspired computing: Cellular automata, neural networks, evolutionary computing, swarm intelligence, artificial life, and complex networks. Genetic Algorithms, Artificial Neural Networks. Artificial intelligence and MEMS.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Contemplate a deep understanding of biological systems, mimetics structures, and functions that inspire engineering innovations for adaptability and sustainability.
CO2	Endeavor biological principles from nature driven techniques to design engineering systems for solving real-world challenges
CO3	Appraise the bioinspired materials for their advanced applications in the domain of health, energy and environmental sustainability.
CO4	Paraphrase biomimicry and ethics in bioinspired engineering designs, ensuring that their solutions are environmentally responsible and socially conscious

Reference Books	
1.	Yoseph Bar-Cohen. Biomimetics: Biologically Inspired Technologies D. Floreano and C. Mattiussi, "Bio-Inspired Artificial Intelligence", CRC Press, 2018. ISBN: 1420037714, 9781420037715.
2.	Guang Yang, Lin Xiao, and Lallepak Lamboni. Bioinspired Materials Science and Engineering. John Wiley, 2018. ISBN: 978-1-119-390336.
3.	M.A. Meyers and P.Y. Chen. Biological Materials, Bioinspired Materials, and Biomaterials Cambridge University Press, 2014 ISBN 978-1-107-01045.
4.	Tao Deng. Bioinspired Engineering of Thermal Materials. Wiley-VCH Press, 2018. ISBN: 978-3-527-33834-4.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
CLINICAL DATA MANAGEMENT (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MBT325DB**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Fundamentals of Healthcare Data and Analytics: Overview, importance, and evolution of health informatics in the digital age, Healthcare Data Types: Structured vs. unstructured data, clinical vs. operational data, and sources of healthcare data, Data Conversion and Integration: Data standardization, integration into clinical data warehouses, and data cleaning. Data Analytics: Introduction to descriptive, predictive, and prescriptive analytics in healthcare. Use of AI and machine learning for improved outcomes, Challenges and Future Trends: Data privacy, interoperability issues, the role of informatics in personalized medicine, and the future of digital health.	
Unit – II	**09 Hrs**
Electronic Health Records (EHRs) and Digital Health: Overview of EHRs: Key components, data capture mechanisms, and the shift towards integrated EHR systems. Scope and Adoption: Role of EHRs in enhancing patient care, interoperability, and data sharing between healthcare providers. Implementation Process: Steps for selecting, deploying, and optimizing EHR systems, including vendor selection and compliance with healthcare regulations. Challenges in EHRs: Usability issues, data quality, resistance to adoption, and strategies for overcoming these barriers. Digital Health Innovations: Impact of telemedicine, remote patient monitoring, and digital therapeutics on EHR integration.	
Unit –III	**09 Hrs**
Data Standards, Interoperability, and Medical Coding: Introduction to Standards: Need for data standards in health informatics, and their role in ensuring interoperability. Terminology and Content Standards: Deep dive into ICD, SNOMED CT, LOINC, and HL7 FHIR. Data Exchange and Transport Standards: HL7, DICOM, CDA, and emerging standards for seamless data exchange. Medical Coding Systems: Role of medical coding in billing, clinical documentation, and outcome measurement. Overview of CPT, ICD-10, and DRG codes. Emerging Trends: Role of AI in medical coding and billing, and the shift towards real-time data standardization.	
Unit –IV	**09 Hrs**
Health Informatics Ecosystem: Introduction to the ecosystem, including hospitals, clinics, insurance providers, and regulatory bodies. Key Players and Stakeholders: Role of informatics professionals, data scientists, clinicians, and IT staff in healthcare. Challenges and Barriers: Addressing technical, organizational, and regulatory challenges in health informatics. Career Opportunities: Overview of roles like clinical informatics specialist, health data analyst, and telehealth coordinator. Resources and Professional Development: Important certifications, online resources, and organizations (e.g., HIMSS, AMIA).	
Unit –V	**09 Hrs**
Health Information Privacy, Security, and Ethics: Introduction to Privacy and Security: Core principles of data privacy, HIPAA, and GDPR in healthcare. Security Principles: Confidentiality, integrity, availability, encryption methods, and access control mechanisms. Authentication and Identity Management: Role of biometric authentication, two-factor authentication, and secure access protocols. Data Security in the Cloud: Cloud computing in healthcare, managing risks in cloud-based data storage, and hybrid cloud models. Ethics in the use of AI in healthcare, managing bias in algorithms, and ensuring equitable access to digital health technologies.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the key principles and challenges of health informatics, and apply them to real-world scenarios.
CO2	Effectively manage the process of data capture, conversion, and analysis to generate actionable insights.
CO3	Apply knowledge of medical coding, data standards, and interoperability to improve data sharing and clinical workflows.
CO4	Implement robust security measures to protect patient data, and navigate ethical issues in health informatics.

Reference Books	
1.	Robert E. Hoyt Ann K. Yoshihashi, Health Informatics, Practical guide for Healthcare and Information Technology Professionals, 6th edition , Informatics, 2014, ISBN: 978-0-9887529-2-4
2.	Kathryn J. Hannah Marion J. Ball, Health Informatics, Springer Series edition, Springer, 2005, ISBN: 1-85233-826-1
3.	William R Hersh, Health Informatics, a Practical guide, 8th edition. 2022, ISBN 978-1-387-85475-2
4.	Pentti Nieminen. Medical informatics and data analysis 1st edition, MDPI AG, 2021, ISBN-13 : 978-3036500980

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**

7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
CYBER FORENSICS AND CYBER LAWS **(Professional Basket Course- Group D)** **(Theory)**						
Course Code	**:**	**MCN325DC**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Computer Forensics in Today's World Introduction to Computer Forensics and Digital Evidence, the Role of the Forensic Investigator, Understanding Forensic Readiness. Legal Issues and Considerations, Types of Computer Forensic Investigations, Forensic Investigation Process.	
Unit – II	**09 Hrs**
Investigation Process Computer Forensics Investigation Methodology, Handling Digital Evidence, Chain of Custody and Documentation, Evidence Preservation: Hashing and Imaging, Investigation Planning and Legal Approval, Searching and Seizing Computers: Search and Seizure Procedures, Obtaining a Search Warrant, Securing the Crime Scene	
Unit –III	**09 Hrs**
Digital Evidence Types of Digital Evidence (Physical, Logical, Latent), Collecting and Preserving Digital Evidence, Writing Reports on Digital Evidence, Identifying Evidence Sources: Hard Drives, Network Logs, Databases, Evidence Recovery Techniques, First Responder Procedures: First Responder Role in Digital Investigations, Protecting and Securing Evidence, Best Practices for Incident Response	
Unit –IV	**09 Hrs**
Jurisdiction of Cyberspace: Information Technology Law Literature and Glossary, Information Technology Law Concepts, Jurisdictional Issues in Cyber Space, scope of I.T. laws, **Law and the Internet:** Domain issues in Internet, Regulatory body, ICANN regulations	
Unit –V	**09 Hrs**
Security Governance Objectives – Security Architecture, Risk Management Objective, Developing A Security Strategy, Sample Strategy Development	

Course Outcomes: After completing the course, the students will be able to	
CO1	Gain a comprehensive understanding of Cyberfornsic and Investigation
CO2	Apply cyber forensics measures, tools, and techniques to protect systems, networks, and information.
CO3	Analyse the Legal Frameworks governing the internet
CO4	Exploration of Security Frameworks in the Cyber space.

Reference Books	
1.	EC-Council CHFI Course Outline: https://www.eccouncil.org/programs/computer-hacking-forensic-investigator-chfi/
2.	Guide to Computer Forensics and Investigations" by Bill Nelson, Amelia Phillips, and Christopher Steuart, 6th Edition (latest), Cengage Learning, February 15, 2018, 978-1337568944
3.	The Basics of Digital Forensics: The Primer for Getting Started in Digital Forensics" by John Sammons, Edition: 2nd Edition (latest) Syngress (an imprint of Elsevier), June 30, 2014, ISBN-10: 0128016353

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	20
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	40
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	40
	MAXIMUM MARKS FOR THE CIE THEORY	100

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	CONTENTS	MARKS
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
INDUSTRIAL SAFETY AND HEALTH (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MCV325DD**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure. National Policy and Legislations on EHS in India - Regulations and Codes of Practice - Role of trade union safety representatives. Occupational health and safety: Introduction: Health, Occupational health: definition, Interaction between work and health, Health hazards, workplace, economy and sustainable development. Development of accident prevention programs and development of safety organizations.	
Unit – II	**09 Hrs**
Work as a factor in health promotion. Potential health hazards: Air contaminants, Chemical hazards, Biological hazards, Physical hazards, Ergonomic hazards, Psychosocial factors, Evaluation of health hazards: Exposure measurement techniques, Interpretation of findings, recommended exposure limits. Controlling hazards: Engineering controls, Work practice controls, Administrative controls. Occupational diseases: Definition, Characteristics of occupational diseases, Prevention of occupational diseases.	
Unit –III	**09 Hrs**
Hazardous Materials characteristics and effects on health: Introduction, Chemical Agents, Organic Liquids, Gases, Metals and Metallic Compounds, Particulates and Fibers, Alkalies and Oxidizers, General Manufacturing Materials, Chemical Substitutes, Allergens, Carcinogens, Mutagens, Reproductive Hazards, Sensitizers and Teratogens, Recommended Chemical Exposure Limits. Physical Agents, Noise and Vibration, Temperature and Pressure, Carcinogenicity, Mutagenicity and Teratogenicity. Ergonomic Stresses: Stress-Related Health Incidents, Eyestrain, Repetitive Motion, Lower Back Pain, Video Display Terminals.	
Unit –IV	**09 Hrs**
Occupational safety and Health act. Occupational Safety and Health Administration, right to know Laws, Accident Causation, Correcting Missing Skills, Investigator Tendencies and Characteristics, Theories of accident causation: Domino theory, Human Factors theory, Accident/Incident theory, Epidemiological theory and systems theory of accident causation.GD	
Unit –V	**09 Hrs**
Environmental Health And Safety Management : Concept of Environmental Health and Safety Management – Elements of Environmental Health and Safety Management Policy and implementation and review – ISO 45001-Strucure and Clauses-Case Studies. Occupational Health and Safety Considerations: Water and wastewater treatment plants, Construction material manufacturing industries like cement plants, RMC Plants, precast plants and construction sites, Municipal solid waste management	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the Industrial and Occupational health and safety and its importance.
CO2	Demonstrate the exposure of different materials, occupational environment to which the employee can expose in the industries.
CO3	Exposure to the onset of regulatory acts and accident causation models.

CO4	Demonstrate the significance of safety policy, models and safety management practices.

Reference Books	
1.	Industrial Health and Safety Acts and Amendments, by Ministry of Labor and Employment, Government of India.
2.	Fundamentals of Industrial Safety and Health by Dr.K.U.Mistry, Siddharth Prakashan, 2012.
3.	Goetsch, D. L. (2011). Occupational Safety and Health for Technologists, Engineers and Managers 3rd edition. Prentice hall.
4.	David. A. Calling - Industrial Safety Management and Technology, Prentice Hall, New Delhi.
5.	5. Environmental and Health and Safety Management by Nicholas P. Cheremisinoff and Madelyn L. Graffia, William Andrew Inc. NY, 1995.
6.	6. ISO 45001:2018 Occupational health and safety management systems – Requirements with guidance for use, International Organisation for Standardisation, 2018.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
ADVANCED TECHNOLOGIES FOR TRANSPORTATION SYSTEMS (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MCV325DE**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Introduction to Intelligent Transportation Systems (ITS): Definition, objectives, Historical Background, Benefits of ITS –ITS. ITS User Services. ITS Applications. Strategic Needs Assessment and Deployment. Regional ITS Architecture Development Process. ITS Standards. ITS Evaluation. ITS Challenges and Opportunities.	
Unit – II	**09 Hrs**
Data collection techniques – Detectors, Automatic Vehicle Location (AVL), Automatic Vehicle Identification (AVI), Geographic Information Systems (GIS), video data collection. **Telecommunications in ITS:** Information Management, Traffic Management Centres (TMC). Application of sensors to Traffic management; Traffic flow sensor technologies; Transponders and Communication systems; Data fusion at traffic management centres; Sensor plan and specification requirements; Elements of Vehicle Location and Route Navigation and Guidance concepts.	
Unit –III	**09 Hrs**
Traffic Engineering - Fundamental relations of traffic flow, Traffic Stream models - , Shock wave, Car following models, Lane changing models, Vehicle arrival models, PCU values, Interrupted and Uninterrupted flow. Signalized intersection design and Analysis based on IRC, HCM and Indo –HCM. Numerical Problems. Traffic Simulation. Numerical Problems. Application of IOT, Machine learning in traffic management.	
Unit –IV	**09 Hrs**
Transportation Network Analysis – Basic Introduction to Travel demand modelling, Trip generation, Distribution, Modal Split and Trip Assignment. Transit Capacity, ITS functional areas: Advanced Traffic Management Systems (ATMS), Advanced Traveler Information Systems (ATIS), Commercial Vehicle Operations (CVO), Advanced Vehicle Control Systems (AVCS), Advanced Public Transportation Systems (APTS), Advanced Rural Transportation Systems (ARTS)	
Unit –V	**09 Hrs**
ITS applications: Traffic and incident management systems; ITS and sustainable mobility, travel demand management, electronic toll collection, ITS and road-pricing. Parking Management; Transportation network operations; commercial vehicle operations; public transportation applications; Automated Highway Systems- Vehicles in Platoons –ITS in World – Overview of ITS implementations in developed countries, ITS in developing countries. Case Studies	

Course Outcomes: After completing the course, the students will be able to	
CO1	Identify and apply ITS applications at different levels
CO2	Illustrate ITS architecture for planning process
CO3	Examine the significance of ITS for various levels
CO4	Compose the importance of ITS in implementations

Reference Books	
1.	Pradip Kumar Sarkar and Amit Kumar Jain, "Intelligent Transport Systems", PHI Learning Private Limited, Delhi,2018, ISBN-9789387472068
2.	Choudury M A and Sadek A, "Fundamentals of Intelligent Transportation Systems Planning" Artech House publishers (31 March 2003); ISBN-10: 1580531601
3.	Bob Williams, "Intelligent transportation systems standards", Artech House, London, 2008. ISBN-13: 978-1-59693-291-3
4.	Asier Perallos, Unai Hernandez-Jayo, Enrique Onieva, Ignacio Julio García Zuazola "Intelligent Transport Systems: Technologies and Applications" Wiley Publishing ©2015, ISBN:1118894782 9781118894781

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
DESIGN AND IMPLEMENTATION OF HUMAN-MACHINE INTERFACE (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MEC325DF**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
FOUNDATIONS OF HMI: The Human: History of User Interface Designing, I/O channels, Hardware, Software and Operating environments, The Psychopathology of everyday Things, Psychology of everyday actions, Reasoning and problem solving. The computer: Devices, Memory, processing and networks. Interaction: Models, frameworks, Ergonomics, styles, elements, interactivity, Paradigms. **Introduction to HMI and domains**: Automotive, Industrial, CE, Medical, ECUs within car and their functionalities. Interaction between ECUs. Communication protocols for ECUs(CAN, LIN, Most, FlexRay, Ethernet etc)	
Unit – II	**09 Hrs**
Automotive Human-Machine Interfaces: Automotive infotainment system - Evolution road map, Feature sets, System architecture, Trends, Human factors and ergonomics in automotive design, Automotive User Experience (UX) Design Principles, In-Vehicle Information Systems (IVIS), Driver-Assistance Systems (DAS) Interfaces, HMI design for adaptive cruise control, Voice and Gesture Recognition in Automotive HMIs, Touchscreen Interfaces and Controls, Usability Testing and Evaluation in Automotive HMIs, Safety Considerations and Regulations in Automotive HMIs, Emerging Technologies in Automotive HMIs, Human-Machine Interfaces for Autonomous Vehicles	
Unit –III	**09 Hrs**
UX and Guidelines: Introduction to UX design - stages, theory, Design thinking, UX Study, Interaction concepts, Graphic design tools - Adobe Photoshop, Adobe XD, Blender, GIMP, Asset Design - Overview , Guidelines and norms, 2D/3D rendering, OpenGL, OSG.	
Unit –IV	**09 Hrs**
HMI User Interface: User-centered HMI development process, Basics of Web-Server. Web-based HMI: Basics of TwinCAT and HTML, CSS, JavaScript. **HMI on Mobile**: Four Principles of Mobile UI Design, Benefits of Mobile HMIs, Mobile HMI Development Suites.	
Unit –V	**09 Hrs**
HMI Control Systems: Introduction to Voice-Based HMI, Gesture-Based HMI, Sensor-Based UI controls. **Haptics in Automotive HMI**: Kinesthetic Feedback Systems, Tactile Feedback Systems, Haptics in Multimodal HMI, Automotive Use-Cases **HMI Testing**: Limitations of Traditional Test Solutions, Case - Study: Bosch's HMI validation tool - Graphics Test Systems (GTS). **UI analytics**: Usage patterns, Debugging, Performance Profiling, Use Cases	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understanding the application of HMIs in various domain.
CO2	Comparison of various communication protocols used in HMI development
CO3	Apply and analyse the car multimedia system free software and hardware evolution.

CO4	Design and evaluate the graphic tools and advanced techniques for creating car dashboard multimedia systems.

Reference Books	
1.	Shuo gao, Shuo Yan, Hang Zhao, Arokia Nathan " Touch based HMI; Principles and Applications" Springer Nature Switzerland AG, 1st Edition.
2.	Robert Wells, " Unity 2020 by Example: A Project based guide to building 2D, 3D augumented reality and Virtual reality games from sratch" Packt Publishing ltd , edition 2020
3.	Ryan Cohen, Tao Wang, "GUI Design and Android Apps" Apress, Berkley, CA,2014

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
ELECTRIC VEHICLE TECHNOLOGY **(Professional Basket Course- Group D)** **(Theory)**						
Course Code	**:**	**MEE325DG**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

UNIT – I	**09 Hours**
History, Basics of Electric Vehicles, Components of Electric Vehicle, General Layout of EV, EV classification: Battery Electric Vehicles (BEVs), Hybrid Electric Vehicle (HEV), Fuel-Cell Electric Vehicles (FCEVs) Comparison with Internal Combustion Engine: Technology, Advantages & Disadvantages of EV, National Policy for adoption of EVs.	
UNIT – II	**09 Hours**
Electric Drive-Trains: Introduction to various electric drive-train topologies in EV and HEV, Power flow control in electric drive-train topologies, classification of electric machines used in automobile drivetrains. **E-Motor Drives Configuration(Control Block diagrams):** Induction Motor Drive, Permanent Magnet (PM) motor Drive & Switched Reluctance Motor (SRM) Drive.	
UNIT – III	**09 Hours**
Battery Energy Storage: Types of Battery, Introduction to Electrochemical Battery, Electrochemical Reactions, Battery Parameters: Battery Capacity, Discharge Rate, Charging Rate, SOC, SOD, SOH, DOD, Specific Energy, Specific Power, Energy Efficiency, **Battery Management Systems (BMS):** Introduction to BMS, Objectives of the BMS: Discharging control, Charging control, Cell Balancing; BMS topologies: Distributed Topology, Modular Topology and Centralized Topology.	
UNIT – IV	**09 Hours**
Energy Storage: Introduction to Energy Storage Requirements in Hybrid and Electric Vehicles, Battery based energy storage, Fuel Cell based energy storage, Super Capacitor based energy storage, Hybridization of different energy storage devices. Introduction to BMS and its topologies. **Energy Management Strategies**: Introduction to energy management strategies used in hybrid and electric vehicles, Classification of different energy management strategies, Comparison of different energy management strategies and implementation issues of energy management strategies.	
UNIT – V	**09 Hours**
Charging Infrastructure: Basic Requirements for Charging System, Charger Architectures, Grid Voltages, Frequencies, and Wiring, Charging Standards and Technologies, SAE J1772. On-board chargers and Off-board chargers, Topologies and Standards, Types of Charging Station Charging Station Placement for Electric Vehicles: A Case Study.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Analyse the basics of electric and hybrid electric vehicles, their architecture, technologies and modelling.
CO2	Analyze various electric drives suitable for electric vehicles.
CO3	Discuss and implement different energy storage technologies used for electric vehicles and their management system.
CO4	Analyse various charging methods, requirements, standards and types of charging for EV and HEV.

Reference Books	
1.	Modern Electric Vehicle Technology C.C. Chan and K.T. Chau, 1st Edition, 2001, Oxford university press, ISBN 0 19 850416 0.
2.	Battery Management system for large Lithium Battery Packs, Davide Andrea, 1st Edition, 2010, ARTECH HOUSE, ISBN-13 978-1-60807-104-3.
3.	Electric Powertrain: Energy Systems, Power Electronics and Drives for Hybrid, Electric and Fuel Cell Vehicles, John G. Hayes, G. Abas Goodarzi, 1st Edition, 2018, Wiley, ISBN 9781119063667.
4.	Hybrid Vehicles from Components to System, F. BADIN, Ed, 1st Edition, 2013, Editions Technip, Paris, ISBN 978-2-7108-0994-4.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
ELECTRONIC NAVIGATION SYSTEMS (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MET325DH**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:1:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**9 Hrs**
An Introduction to Radar: Basic Radar, The simple form of the Radar Equation, Radar Block Diagram, Radar Frequencies, Application of radar, Types of Radars. Detection of signals in Noise, Receiver Noise and the Signal-to Noise Ratio, Probability of Detection and False alarm, Introduction to Doppler, MTI, UWB Radars	
Unit – II	**09 Hrs**
Terrestrial Network based positioning and navigation: General Issues of wireless positions location, Fundamentals, positioning in cellular networks, positioning in WLANs, Positioning in Wireless sensor networks.	
Unit –III	**09 Hrs**
Satellite-based navigation systems: Global Navigation satellite systems (GNSS), GNSS receivers.	
Unit –IV	**09 Hrs**
LiDAR: Introduction to LiDAR, context and conceptual discussion of LiDAR, Types of LiDARS, LiDARS Detection modes, Flash LiDAR versus Scanning LiDAR, Monostatic versus Bistatic LiDAR, Major Devices in a LiDAR, LiDAR remote sensing, Basic components and physical principles of LiDAR, LiDAR accuracy and data formats	
Unit –V	**09 Hrs**
SONAR: Underwater acoustics, applications, comparison with radar, submarine detection and warfare, overcoming the effects of the ocean, sonar and information processing.Transmission of the acoustic signal: Introduction, detection contrast and detection index, transmission equation, equation of passive and active sonar.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the concepts of Radar, LiDAR, Sonar, terrestrial and satellite based navigation system.
CO2	Apply the concepts of radars, LiDAR, Sonar, cellular networks, WLAN, sensor networks and satellites in determining the user position and navigation.
CO3	Analyze the different parameters of satellite and terrestrial networks for navigation systems.
CO4	Evaluate the Radar, LiDAR, Sonar systems and satellite and terrestrial network based navigation and tracking systems.

Reference Books	
1.	M. L Skolnik,Introduction to RADAR Systems,3rd edition, 2017,TATA Mcgraw-Hill, ISBN: 978-0070445338
2.	Mark A Richards, James A Scheer, William A Holam,Principles of Modern Radar Basic Principles, 2010, 1st edition,SciTech Publishing Inc, ISBN:978-1891121524 .
3.	Davide dardari, Emanuela Falletti, Marco Luise, Satellite and Terrestrial Radio Positioning techniques- A signal processing perspective, 1st Edition, 2012, Elsevier Academic Press, ISBN: 978-0-12-382084-6.
4.	Paul McManamon,LiDAR Technologies and Systems, SPIE press, 2019.
5.	Pinliang Dong and Qi Chen,LiDAR Remote Sensing and Applications, CRC Press, 2018, ISBN: 978-1-4822-4301-7
6.	Jean-Paul Marage, Yvon Mori, Sonar and Underwater Acoustics, Wiley, 2013, ISBN: 9781118600658

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10) Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
VEHICULAR COMMUNICATION ECOSYSTEM (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MET325DJ**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Introduction: Basic Principles and Challenges, Past and Ongoing VANET Activities **Standards and Regulations of DSRC** Introduction, Layered Architecture for VANETs, DSRC Regulations, DSRC Physical Layer Standard, DSRC Data Link Layer Standard (MAC and LLC), DSRC Middle Layers.	
Unit – II	**09 Hrs**
Physical Layer Considerations for Vehicular Communications: Standards Overview, Wireless Propagation Theory, Channel Metrics, Measurement Theory, Empirical Channel Characterization at 5.9 GHz. **MAC Layer and Scalability Aspects of Vehicular Communication Networks:** Challenges and Requirements. MAC Approaches for VANETs, Communication Based on IEEE 802.11p.	
Unit –III	**09 Hrs**
MAC Layer and Scalability Aspects of Vehicular Communication Networks Performance Evaluation and Modeling, Aspects of congestion control. **Data Security in Vehicular Communication Networks**: Challenges of Data Security in Vehicular Networks, Network, Applications, and Adversarial Model, Security Infrastructure, Cryptographic Protocols.	
Unit –IV	**09 Hrs**
Intra-vehicle communication:-In-vehicle networks, Automotive bus systems, In-vehicle Ethernet, Wireless in-vehicle networks **Inter-vehicle communication**: Applications, Requirements and components, Concepts for inter-vehicle communication, Fundamental limi	
Unit –V	**09 Hrs**
Cooperative Vehicular Safety Applications: Introduction, Enabling technologies, Cooperative system architecture, Mapping for safety applications. **VANET-enabled Active Safety Applications:** Infrastructure-to-vehicle applications, Vehicle-to-vehicle applications, Pedestrian-to-vehicle applications.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Illustrate fundamentals of wireless vehicular networks.
CO2	Design of Physical & MAC layer and routing protocols for vehicular networks.
CO3	Analyse the security issues and energy management in vehicular networks.
CO4	Evaluate the performance of vehicular networks in different use cases.

Reference Books	
1.	Hannes Hartenstein and Kenneth Laberteaux (eds.), VANET Vehicular Applications and Inter-networking Technologies, John Wiley & Sons, 2009
2.	Christophe Sommer and Falko Dressler, Vehicular Networking, Cambridge University Press, 2014.
3.	Claudia Campolo, AntonellaMolinaro and Riccardo Scopigno, Vehicular ad hoc Networks: Standards, Solutions, and Research, Springer, 2015.
4.	Andrea Goldsmith, Wireless Communications, Cambridge University Press, 2005.
5.	Hannes Hartenstein and Kenneth Laberteaux (eds.), VANET Vehicular Applications and Inter-networking Technologies, John Wiley & Sons, 2009.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
ESSENTIALS OF PROJECT MANAGEMENT (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MIM325DK**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Introduction: Project Planning, Need of Project Planning, Project Life Cycle, Roles, Responsibility and Team Work, Project Planning Process, Work Breakdown Structure (WBS), Introduction to Agile Methodology.	
Unit – II	**09 Hrs**
Capital Budgeting: Capital Investments: Importance and Difficulties, phases of capital budgeting, levels of decision making, facets of project analysis, feasibility study – a schematic diagram, objectives of capital budgeting	
Unit –III	**09 Hrs**
Project Costing: Cost of Project, Means of Finance, Cost of Production, Working Capital Requirement and its Financing, Profitability Projections, Projected Cash Flow Statement, Projected Balance Sheet, Multi-year Projections, Financial Modeling, Social Cost Benefit Analysis	
Unit –IV	**09 Hrs**
Tools & Techniques of Project Management: Bar (GANTT) chart, bar chart for combined activities, logic diagrams and networks, Project evaluation and review Techniques (PERT) Critical Path Method (CPM), Computerized project management.	
Unit –V	**09 Hrs**
Project Management and Certification: An introduction to SEI, CMMI and project management institute USA – importance of the same for the industry and practitioners. PMBOK 6 - Introduction to Agile Methodology, hemes / Epics / Stories, Implementing Agile. Domain Specific Case Studies on Project Management: Case studies covering project planning, scheduling, use of tools & techniques, performance measurement.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain project planning activities that accurately forecast project costs, timelines, and quality.
CO2	Evaluate the budget and cost analysis of project feasibility.
CO3	Analyze the concepts, tools and techniques for managing projects.
CO4	Illustrate project management practices to meet the needs of Domain specific stakeholders from multiple sectors of the economy (i.e. consulting, government, arts, media, and charity organizations).

Reference Books	
1.	Prasanna Chandra, Project Planning Analysis Selection Financing Implementation & Review, Tata McGraw Hill Publication, 9th Edition, 2017, ISBN: 978-9332902572.
2.	Project Management Institute, A Guide to the Project Management Body of Knowledge (PMBOK Guide), 5th Edition, 2013, ISBN: 978-1-935589-67-9
3.	Harold Kerzner, Project Management A System approach to Planning Scheduling & Controlling, John Wiley & Sons Inc., 11th Edition, 2013, ISBN 978-1-118-02227-6.
4.	Rory Burke, Project Management – Planning and Controlling Techniques, John Wiley & Sons, 4th Edition, 2004, ISBN: 978-0470851241

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
USER INTERFACE AND USER EXPERIENCE (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MIS325DM**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
What's a UI Pattern?: How Users Interact With Design Patterns, Following Universal Design Conventions, Applying Empathy to UI Design Patterns. Why Use UI Patterns?: Why Patterns Work, Expectations Reinforce Themselves, Deadline-Busting Communication, Why not use patterns?. The Importance of Prototyping First: Got a Pattern? Plan it Out, Thinking Through the Process, Patterns Take Guesswork Off of Developers' Plates.	
Unit – II	**09 Hrs**
User Testing: Insights You Can't Ignore. Prototyping UI Patterns: Explaining the Gray Box, Pattern Libraries Are Prototyping Shortcuts, Reusable elements, Patterns and Prototypes Work Together, Applying UI Design Patterns: Building a Pattern Library, Riffing on Design Patterns, Tweaking Pattern Styles, Going forward, Useful UI Pattern Examples, Formatting Data, Getting input, Navigation, Teasers.	
Unit –III	**09 Hrs**
Design for Usefulness: Painkillers & Vitamins, Embracing Goal-Centered Design, Test for Relevancy With an MVP, A Quick MVP Case Study: Buffer. Designing for Usability: Forgiving, Satisfying, The 6-Step Process to Improve Usability. Designing for Desirability: Desirable Products Are More Usable, Desire Is Relative to Users, Elements of Desirable Design.	
Unit –IV	**09 Hrs**
Designing for Findability: Building the Right Information Architecture, 5 IA Layouts for the Web, 5 Navigational Menu Patterns, Testing Findability. Designing for Accessibility: Universal Design, What Accessibility Means for UX Design, Benefits of Accessibility, Accessibility Best Practices	
Unit –V	**09 Hrs**
The Core of Desirable Design: The Habit Loop, A Quick Case Study, Quick Case Study: Apple.com. Designing for Credibility: First Impressions Matter, Quick Case Study: Chase, Building a Credible Product Interface, Selling the Product Through Social Proof, Persuading Through Transparency.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply the concept of User Interface and User Experience to increase look and feel various applications.
CO2	Analyse the usability, accesssibility, availability and other factors of User Interface design patterns.
CO3	Design and implement techniques of implementing design patterns.
CO4	Evaluate the design patetrns and elements of user experience.

Reference Books	
1.	Ben Gremillion, Jerry Cao, Kamil, Tactical UI Design Patterns, The Handbook to faster Design, UXPin Inc., 2015.
2.	Jerry Cao, Kamil, Matt Ellis, The Elements of Successful UX Design, Best Practices of Meaningful products, UXPin Inc., 2015.
3.	User Friendly- How the Hidden Rules of Design Are Changing the Way We Live, Work, and Play, Cliff Kuang, Picador Paper; Reprint edition, 2020, ISBN: 1250758203
4.	Jenifer Tidwel, Designing Interfaces: Patterns for Effective Interaction Design, 3rd Edition, O'Reilly, 2020, ISBN: 1492051969

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
MATHEMATICAL METHODS FOR DATA SCIENCE (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MMA325DN**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Parameter Estimation: Introduction to probability models of univariate random variables, Discrete distribution (Bernoulli, Binomial, Poisson), Continuous distributions (Uniform, Exponential, Normal), Estimation - Criteria for good estimates - unbiasedness, consistency, efficiency and sufficiency, Variance of a point estimator, Parameter estimation via maximum likelihood, Method of moments, Bayesian estimation of parameters.	
Unit – II	**09 Hrs**
Optimization I: Introduction and formulation, Optimality conditions, Review of local maxima, and local minima along with first and second order conditions. Taylor series and local function approximation, automatic differentiation, One dimensional Search Methods - Sequential search method, Fibonacci search method, Golden section search method.	
Unit –III	**09 Hrs**
Optimization II: Constrained and Unconstrained optimization, Gradient vector, Hessian matrix, optimization using Hessian matrix, Gradient descent method, Step size selection and convergence, Newton method, Stochastic gradient descent (SGD), Convex optimization, Duality - weak and strong duality, Optimization using duality.	
Unit –IV	**09 Hrs**
Fuzzy Optimization: Basic concepts of fuzzy sets - Operations on fuzzy sets, Fuzzy relation equations, Fuzzy logic control, Fuzzification, Defuzzification, Decision making logic, Membership functions. **Artificial Neural Networks:** Introduction - Neuron model, Multilayer perceptions - Back propagation algorithm and its variants, Loss functions in artificial neural networks.	
Unit –V	**09 Hrs**
Machine Learning Algorithms: Unsupervised learning, Supervised learning, Linear regression, Multiple Linear Regression, Overfitting, Naïve Bayes classifier. Clustering methods, k-means clustering, Linear support vector machine, Kernel functions and Nonlinear support vector machine.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explore fundamental concepts of estimation, optimization, and machine learning applied in various branches of engineering.
CO2	Apply theoretical concepts of estimation and optimization to model problems using a machine learning approach on model requirements and to evaluate solutions within given constraints effectively.
CO3	Analyze and solve the modern engineering problems using appropriate techniques of statistical and mathematical learning to the real-world problems arising in many practical situations.
CO4	Develop and implement algorithms for constrained and unconstrained optimization, utilizing estimation techniques to classify, predict, and optimize solutions for practical applications, emphasizing model accuracy and performance and also engage in lifelong learning.

Reference Books	
1.	Jorge Nocedal Stephen J. Wright, Numerical Optimization, Springer, 2nd Edition, 2006, ISBN-10: 0-387-30303-0 ISBN-13: 978-0387-30303-1.
2.	Mykel J. Kochenderfer, Tim A. Wheeler, Algorithms for Optimization, MIT Press, Illustrated Edition, 2019, ISBN-13 978-0262039420.
3.	Christopher M. Bishop, Pattern Recognition and Machine Learning, Springer, 1st Edition, 2006, ISBN-10: 0-387-31073-8 ISBN-13: 978-0387-31073-2.
4.	Shai Shalev-Shwartz and Shai Ben-David "Understanding Machine Learning: From Theory to Algorithms", 1st Edition, Cambridge University Press, 2014, ISBN: 978-1-107-05713-5.
5.	George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic: Theory and Applications, 1st Edition, Prentice Hall PTR, 1995, ISBN 0-13-101171-5.

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10) Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
INDUSTRY 4.0: THE SMART MANUFACTURING (Professional Basket Course- Group D) (Theory)						
Course Code	**:**	**MME325DO**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Fundamentals of Industry 4.0-Introduction, Key Components of Industry 4.0, RAMI 4.0, Cyber-Physical Systems. **Servitization and Product-Service Systems** - Integrated Overview, Examples Across Sectors. Industry 4.0 Across Sectors- Introduction, Smart Manufacturing, Transportation 4.0, Multimodal Transportation Systems, Rail 4.0, Logistics 4.0 and Implications. **Future Trends and Challenges**- Emerging Applications, Risks and Barriers to Implementation	
Unit – II	**09 Hrs**
The Concept of IIoT- Introduction to IIoT, Key Features and Applications **Modern Communication Protocols**- Overview, TCP/IP, Wireless Communication, Technologies. **API**- A Technical Perspective, Importance in IIoT, Examples Applications, **Middleware Architecture**- Role in IIoT, Integration and Data Flow Management. **Emerging Trends in IIoT**- Industrial IoT Standards and Frameworks, Edge Computing in IIoT.	
Unit –III	**09 Hrs**
Data Analytics in Manufacturing: Energy Efficiency in Manufacturing, Anomaly Detection in Air Conditioning Systems, Smart Remote Machinery Maintenance Systems with Komatsu, Quality Prediction in Steel Manufacturing, Predictive Maintenance with Data Analytics **Internet of Things and New Value Proposition**: IoT in Manufacturing, Value Creation Barriers: Standards, security, and privacy concerns. **Advances in Robotics in the Era of Industry 4.0**: Recent Technological Components of Robots, Advanced Sensor Technologies, Artificial Intelligence in Robotics, Collaborative Robots, Internet of Robotic Things, Cloud Robotics, Digital Twin Technology	
Unit –IV	**09 Hrs**
Additive Manufacturing Technologies and Applications: Additive Manufacturing Technologies Overview, Stereo lithography, 3D Printing, Fused Deposition Modeling, Selective Laser Sintering, Laser Engineered Net Shaping, Manufacturing in Industry 4.0, Hybrid Manufacturing Processes. **Advances in Virtual Factory Research and Applications**: The State of Art, The Virtual Factory Software	
Unit –V	**09 Hrs**
Cybersecurity and Resilience in Industry 4.0: Introduction to Cybersecurity in Industry 4.0, Industrial IoT security, Edge and Cloud Security, Digital Twin Security, AI and Machine Learning for Cybersecurity, Standards and Frameworks for Industry 4.0 Cybersecurity, Resilience Strategies for Industry 4.0, Future Trends in Cybersecurity for Industry 4.0	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the opportunities, challenges brought about by Industry 4.0 for benefits of organizations and individuals
CO2	Analyze the effectiveness of Smart Factories, Smart cities, Smart products and Smart services
CO3	Apply the Industrial 4.0 concepts in a manufacturing plant to improve productivity and profits
CO4	Evaluate the effectiveness of Cloud Computing in a networked economy

Reference Books	
1.	Alasdair Gilchrist, Industry 4.0 The Industrial Internet Of Things, Apress Publisher, ISBN-13 (pbk): 978-1-4842-2046-7
2.	Alp Ustundag, Emre Cevikcan, Industry 4.0: Managing The Digital Transformation, Springer, 2018 ISBN 978-3-319-57869-9
3.	Ovidiu Vermesan and Peer Friess, Designing the industry - Internet of things connecting the physical, digital and virtual worlds, Rivers Publishers, 2016 ISBN 978-87-93379-81-7
4.	Christoph Jan Bartodziej, The concept Industry 4.0- An Empirical Analysis of Technologies and Applications in Production Logistics, Springer Gabler, 2017 ISBN 978-3-6581-6502-4

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

Semester: II						
INDUSTRIAL INTERNET OF THINGS (IIOT) **(Professional Basket Course- Group D)** **(Theory)**						
Course Code	**:**	**MME325DQ**		**CIE**	**:**	**100Marks**
Credits: L:T:P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Total Hours	**:**	**45L+45EL**		**SEE Duration**	**:**	**03 Hours**

Unit-I	**09 Hrs**
Introduction: IoT vs IIoT, challenges in deployment, building blocks of business model and architecture, layers, sensing for manufacturing process, processing, communication and networking. Applications – Factories and assembly lines, inventory management and quality control, facility management. **Industrial Control Systems** Process Industries versus Discrete Manufacturing Industries – Levels, variables and parameters, Continuous Control Systems, Discrete Control Systems, Computer Process Control - Control Requirements, Capabilities of Computer Control, Forms of Computer Process Control.	
Unit – II	**09 Hrs**
Sensors in IIoT applications Temperature sensor interfacing, accelerometer sensor interfacing, MoS Gas sensor, magneto strictive sensors, speed sensor, ultrasonic sensor, smart sensors. **Automatic identification and data Capture** Overview Of Automatic Identification Methods, Linear (One-Dimensional) Bar Code, Two-Dimensional Bar Codes, Radio Frequency Identification, Magnetic Stripes, Optical Character Recognition, Machine Vision	
Unit –III	**09 Hrs**
Group Technology and Cellular Manufacturing Part Family, Intuitive Grouping, Parts Classification and Coding, Production Flow Analysis, cellular manufacturing - Composite Part Concept, Machine Cell Design, applications of group technology, Opitz Part Coding System, Machine Cell Organization and Design Rank-Order Clustering - Numericals	
Unit –IV	**09 Hrs**
Industrial Networking Introduction, Hierarchy of Industrial Networks, Network Topologies, Data Flow Management, Transmission Hardware, Network Backbones, Network Communication Standards, Fieldbus Networks **Simulating Industrial Processes** Queues and Queueing – waiting time, service time, machine utilisation, Modelling an Industrial Process Designing a Process Simulation, managing resource utilisation, product mixes, Queuing network models.	
Unit –V	**09 Hrs**
Clustering Similarity measures, hierarchical clustering – single linkage, complete linkage, average linkage Non heirerchial clustering – Numericals, multidimensional scaling correspondence analysis - Numericals **Prediction Models** K- Nearest neighbour, RMS Error and Mean Absolute Error, Mean Absolute Percentage Error, Coefficient of Determination, Underfitting and Overfitting, Cross-Validation, multiple regression – Numericals.	

Course Outcomes: After completing the course, the students will be able to	
CO1	***Analyze*** the differences between IoT and IIoT, and evaluate the challenges, architectures, and sensing layers involved in the deployment of IIoT for manufacturing and industrial applications.
CO2	***Demonstrate*** the ability to interface sensors in IIoT systems, and apply automatic identification techniques for process automation.
CO3	***Design*** machine cells using group technology principles, and implement cellular manufacturing systems for optimized production workflows.
CO4	***Develop*** simulation models for industrial processes, and predict outcomes to optimize industrial system performance.

Reference Books	
1.	Jeschke, S., Brecher, C., Song, H., & Rawat, D. B. (Eds.). (2017). Industrial Internet of Things: Cyber manufacturing Systems. Springer. ISBN: 978-3-319-42559-7.
2.	Groover, M. P. (2018). Automation, Production Systems, and Computer-Integrated Manufacturing (5th ed.). Pearson. ISBN: 978-0134605463.
3.	Johnson, R. A., & Wichern, D. W. (2007). Applied Multivariate Statistical Analysis (6th ed.). Pearson Prentice Hall. ISBN: 978-0131877153.
4.	Hill, R., & Berry, S. (2021). Guide to Industrial Analytics: Solving Data Science Problems for Manufacturing and the Internet of Things. Springer. ISBN: 978-3-030-79103-2

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	**COMPONENTS**	**MARKS**
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	**20**
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	**40**
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video- seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	**40**
	MAXIMUM MARKS FOR THE CIE THEORY	**100**

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	**CONTENTS**	**MARKS**
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	**20**
3 & 4	Unit 2: Question 3 or 4	**20**
5 & 6	Unit 3: Question 5 or 6	**20**
7 & 8	Unit 4: Question 7 or 8	**20**
9 &10	Unit 5: Question 9 or 10	**20**
	TOTAL	**100**

SEMESTER: II						
Course Code	:	MIM416RT	**RESEARCH METHODOLOGY**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	16L	*(Common Course to all M.Tech Programs)*	SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 8 Weeks

Week 1: A group discussion on what is research; Overview of research
Week 2: Literature survey, Experimental skills
Week 3: Data analysis, Modelling skills
Week 4: Technical writing; Technical Presentations; Creativity in Research
Week 5: Creativity in Research; Group discussion on Ethics in Research
Week 6: Design of Experiments
Week 7: Intellectual Property
Week 8: Department specific research discussions

Course duration: 8 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors:
Prof. Edamana Prasad, Prof. Prathap Haridoss

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

Reference Books:

1. Krishnaswami, K.N., Sivakumar, A. I. and Mathirajan, M., Management Research Methodology, Integration of Principles, Methods and Techniques, 17th Impression, Pearson India Education Services Pvt. Ltd, 2018. ISBN: 978-81-7758-563-6
2. William M. K. Trochim, James P. Donnelly, The Research Methods Knowledge Base, 3rd Edition, Atomic Dog Publishing, 2006, ISBN: 978-1592602919
3. Kothari C.R., Research Methodology Methods and Techniques, 4th Edition, New Age International Publishers, 2019, ISBN: 978-93-86649-22-5.
4. Levin, R.I. and Rubin, D.S., Statistics for Management, 8th Edition, Pearson Education: New Delhi, 2017, ISBN-13- 978-8184957495.

Semester: II						
SKILL LAB (LAYOUT DESIGN LAB)						
Course Code	**:**	**MVE427SL**		**CIE**	**:**	**50 Marks**
Credits: L:T:P	**:**	**0:0:2**		**SEE**	**:**	**50 Marks**
Total Hours	**:**	**15P**		**SEE Duration**	**:**	**03 Hours**

- **Module 1:** Design and perform analysis of a current mirror circuit and draw the optimized layout of the same using a suitable analog layout technique.
- **Module 2:** Design a differential input circuit and draw the optimized layout using 45nm CMOS technology.
- **Module 3:** Design a single-stage differential amplifier and draw the optimized layout using 45nm CMOS technology.
- **Module 4:** Perform pre and post-layout simulation of three-stage single-ended VCO using 45nm CMOS technology.
- **Module 5:** Design a Common Source Amplifier and draw the optimized layout using 45nm CMOS technology.
- **Module 6:** Develop a standard cell layout of the inverter (INVX1, INVX2) using 45nm CMOS technology, and verify the layout.
- **Module 7:** Perform the pre and post-layout simulation of a standard cell layout of NAND using 45nm CMOS technology
- **Module 8:** Perform the pre and post-layout simulation of a standard cell layout of AOI21/OAI21 using 45nm CMOS technology.
- **Module 9:** Design of an OPAMP, Developing a standard cell library.

Course Outcomes: After completing the Lab, the students will be able to	
CO1	Apply the analog layout techniques to understand the effects of antenna effect, latch-up, Electro- Migration, IR drop, etc.
CO2	Analyze the challenges in deep sub-micron process using well proximity effect, LOD, and Shallow trench isolation.
CO3	Verify chip layout design using all physical verification concepts and tools.
CO4	Develop layout for standard cells and their characterization with different process corners.

Reference Text Books	
1.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits," 2000, McGraw-Hill Education, ISBN 978-0072380323.
2.	Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits," 2009, Wiley, ISBN 978-0470245996.
3.	Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design," 2011, Oxford University Press, ISBN 978-0199765072.
4.	Willy M.C. Sansen, "Analog Design Essentials," 2006, Springer, ISBN 978-0387257464.

RUBRIC FOR CONTINUOUS INTERNAL EVALUATION (CIE-Lab)		
1	Conduction of the experiments relevant to the modules & Report	15
2	Design and testing of the Prototype / Projects / Modules	20
3	Final presentation and report	15
	MAXIMUM MARKS FOR THE SEE	**50**

RUBRIC FOR SEMESTER END EXAMINATION (SEE-Lab)

The evaluation will be carried out by Internal and External examiners through Exhibition Mode.
The following weightage would be given for the exhibition.

Q.NO.	CONTENTS	MARKS
1	Presentation through posters	15
2	Demonstration of the Prototype / Projects / Modules	25
3	Vivavoce	10
	MAXIMUM MARKS FOR THE SEE	**50**

SEMESTER: III						
ALGORITHM FOR VLSI DESIGN AUTOMATION (Theory) (Professional Core Course)						
Course Code	**:**	**MVE361TA**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**3:1:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**45L+30T+45EL**		**SEE Duration**	**:**	**03 Hrs**

Unit – I	**09 Hrs**
Scheduling Algorithms: Introduction, A model for scheduling problems, Scheduling without and with resource constraints, Scheduling algorithms for extended sequencing models, Scheduling pipelined circuits, Resource sharing and binding.	
Unit – II	**09 Hrs**
Data Structure and Basic Algorithms: Basic Terminology, Graph Search Algorithms, Computational Geometry Algorithms, Basic Data Structures. **Partitioning:** Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms	
Unit – III	**09 Hrs**
Floor Planning and Pin Assignment: Problem formulation, classification, Constraint-based, Integer programming-based, rectangular Dualization, simulated evolution floor planning algorithms. **Placement:** Problem formulation, Classification, Simulation-based, Partitioning based Placement Algorithms	
Unit – IV	**09 Hrs**
Global Routing: Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path-based Algorithms, Steiner tree-based Algorithms **Detailed Routing:** Problem formulation, Classification single Layer routing, General river routing, Single row routing	
Unit – V	**09 Hrs**
Channel, Clock and Power Routing: Two-layer channel routing Algorithms, Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms, Introduction to compaction, shadow propagation algorithm.	

Course Outcomes: After going through this course the student will be able to	
CO1	Apply the knowledge of MOSFET & amplifiers to investigate various design trends of analog IC design
CO2	Analyze the functionality of analog/mixed-signal circuits & systems
CO3	Design and implement analog integrated circuits & systems
CO4	Evaluate the different performance parameters of analog/mixed-signal integrated circuits

Reference Books	
1.	Synthesis and Optimization of Digital Circuit, 1994, Giovanni De Micheli, McGraw-Hill, ISBN: 10-0070163332
2.	Algorithms for VLSI Physical Design Automation, N.A. Sherwani, 2002, Kluwer Academic Publishers, ISBN: 0-7923-8393-1
3.	An Introduction to VLSI Physical Design, M Sarraf Zadeh, C K Wong, 1996, McGraw Hill, ISBN:0070571945
4.	Algorithms for VLSI Design Automation, S.H. Gerez, 1998, John Wiley & Sons, ISBN: 978-0-471 98489-4

RUBRICS FOR THE CONTINUOUS INTERNAL EVALUATION (THEORY)		
#	COMPONENTS	MARKS
1.	**QUIZZES:** Quizzes will be conducted in online/offline mode. **TWO QUIZZES** will be conducted & Each Quiz will be evaluated for 10 Marks. **THE SUM OF TWO QUIZZES WILL BE THE FINAL QUIZ MARKS.**	20
2.	**TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **TWO tests will be conducted**. Each test will be evaluated for **50 Marks**, adding up to 100 Marks. **FINAL TEST MARKS WILL BE REDUCED TO 40 MARKS.**	40
3.	**EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning (10), Program-specific requirements (10), Video-seminar/presentation/demonstration (10**)** Real-time problem solving (10) **ADDING UP TO 40 MARKS**.	40
	MAXIMUM MARKS FOR THE CIE THEORY	100

RUBRICS FOR SEMESTER END EXAMINATION (THEORY)		
Q.NO.	CONTENTS	MARKS
Each unit consists of TWO questions with 20 marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5]		
1 & 2	Unit 1: Question 1 or 2	20
3 & 4	Unit 2: Question 3 or 4	20
5 & 6	Unit 3: Question 5 or 6	20
7 & 8	Unit 4: Question 7 or 8	20
9 &10	Unit 5: Question 9 or 10	20
	TOTAL	100

SEMESTER: III						
Course Code	:	MVE232E1	**DIGITAL VLSI TESTING**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	24L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 12 Weeks

Week 1: Introduction: Importance, Challenges, Levels of abstraction, Fault Models, Advanced issues
Week 2: Design for Testability: Introduction, Testability Analysis, DFT Basics, Scan cell design, Scan Architecture
Week 3: Design for Testability: Scan design rules, Scan design flow . Fault Simulation: Introduction, Simulation models
Week 4: Fault Simulation: Logic simulation, Fault simulation
Week 5: Test Generation: Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms
Week 6: Test Generation: ATPG for non stuck-at faults, Other issues in test generation Built-In-Self-Test: Introduction, BIST design rules
Week 7: Built-In-Self-Test: Test pattern generation, Output response analysis, Logic BIST architectures
Week 8: Test Compression: Introduction, Stimulus compression
Week 9: Test Compression: Stimulus compression, Response compression
Week 10: Memory Testing: Introduction, RAM fault models, RAM test generation
Week 11: Memory Testing: Memory BIST Power and Thermal Aware Test: Importance, Power models, Low power ATPG
Week 12: Power and Thermal Aware Test: Low power BIST, Thermal aware techniques

Course duration: 12 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors: **Prof. Santanu Chattopadhyay,** IIT Kharagpur
Reference Books: "Digital Systems Testing and Testable Design" by Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

SEMESTER: III						
Course Code	:	MVE232E2	**C BASED- VLSI DESIGN**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	24L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 12 Weeks

Week 1: Introduction to Electronic Design Automation
Week 2: Introduction to C-based VLSI Design: Background
Week 3: Introduction to C-based VLSI Design: HLS Flow
Week 4: C-Based VLSI Design: Scheduling
Week 5: C-Based VLSI Design: Resource allocation and Binding, Data-path and Controller Generation
Week 6: Efficient Synthesis of C Code
Week 7: Hardware Efficient C Coding
Week 8: Impact of Compiler Optimizations in Hardware
Week 9: Verification of High-level Synthesis
Week 10: FPGA Technology Mapping Week 11: Securing Design with High-level Synthesis
Week 12: Recent Advances in C-Based VLSI Design

Course duration: 12 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors: Prof. Chandan Karfa ,IIT Guwahati
Reference Textbook: "Advanced Chip Design: Practical Examples in Verilog" by Kishore K. Mishra

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

SEMESTER: III						
Course Code	:	MVE232E3	**VLSI INTERCONNECTS**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	24L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 12 Weeks

Week 1: Introduction to VLSI Interconnects. Distributed RC interconnect model, Elmore delay, Elmore delay in interconnects, Elmore delay in RC tree and branched interconnects

Week 2: Equivalent circuit of RC interconnect, Scaling Effects, Delay mitigation in RC interconnects, RC interconnect simulation session, Inductive effects in interconnects

Week 3: Distributed RLC Interconnect model (Frequency domain analysis), Transmission line equations. When to consider the inductive effects? The transfer function of an interconnect, Time-domain response of a lumped model RLC circuit

Week 4: Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parameters. Simulation of RLC interconnects. Origin of the skin effect, Effective resistance at high frequencies

Week 5: Equivalent circuit to simulate skin effect, Power dissipation due to interconnects, Optimum interconnect width for minimizing total power dissipation. Heating effects and thermal modelling,

Week 6: Electromigration in interconnects, Mitigation of electromigration. Capacitive coupling in interconnects. Cross-talk and timing jitters in two identical interconnects. Effects of cross-talk and timing jitters.

Week 7: Techniques for mitigation of cross-talk, 23-erutceL Matrix formulation of coupled interconnects. Coupled RLC interconnects,

Week 8: Analysis of coupled interconnects: Examples-2, Simulation of RC coupled interconnects, Extraction of capacitance (part-1 & part-2), Estimation of interconnect parameters from S parameters

Course duration: 12 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors: Prof. Sarang Pendharker, IIT Kharagpur
Reference Books : "High-Speed Digital Design: A Handbook of Black Magic" by Howard Johnson and Martin

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL. Exam is conducted by NPTEL.

SEMESTER: III						
Course Code	:	MVE232E4	**SENSOR TECHNOLOGIES: PHYSICS,FABRICATION & CIRCUITS**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	16L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 8 Weeks

Week 1: Basics of Sensors
Week 2: Basics of Sensors
Week 3: Physics of Sensors
Week 4: Physics of Sensors
Week 5: Physics of Sensors
Week 6: Sensor Fabrication and Characterization Techniques
Week 7: Sensor Fabrication and Characterization Techniques
Week 8: Basics of Sensor Systems and Circuits

Course duration: 8 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors: **Prof. Mitradip Bhattacharjee,** IISER Bhopal
Reference Textbook: "Sensor Technologies: Physics, Fabrication, and Applications" by Michael J. McGrath, Cliodhna Ni Scanaill, and Dympna O'Connell

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

SEMESTER: III					
MINOR PROJECT					
Course Code	**:**	**MVE443P**		**CIE Marks**	**50**
Credits L:T:P	**:**	**0:0:6**		**SEE Marks**	**50**
Hours/Week	**:**	**7**		**SEE Duration**	**03 Hrs**

Guidelines

1. Students can form group of two to execute the Minor Project.
2. Students are required to select topics related to their PG Program Specialization after extensive Literature Survey and analyzing the Research gaps.
3. Students will be assigned to guides in accordance with the expertise of the faculty.
4. Minor project topics could also be aligned to be implemented/executed based on any of the 16 Centre of Excellence (CoE)/ 06 Center of Competence (CoC) domain. The details of these could be obtained by visiting the website https://rvce.edu.in/rvce-center-excellence
5. Minor project has to be implemented/executed in-house, using the resources available in the department/college/CoE/CoC.
6. Students have to note the periodic progress in the Minor Project Diary and report the work carried to their respective guides.
7. Students have to present the Minor project work to the departmental committee and only upon approval by the committee, the student can proceed to prepare and submit the hard copy of the final Minor project report.
8. The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be softbound in Ivory/White color for PG circuit Programs and Light Blue for Non-Circuit Programs.

Course Outcomes: After completing the course, the students will be able to

CO1	:	Analyze the research gaps, formulate the problem definition, conceptualize the objectives and design solution to cater to specific problems.
CO2	:	Apply higher order thinking skills and develop skill competencies specific to program specialization to implement real world problems with professional ethical standards.
CO3	:	Demonstrate the skill and knowledge by applying appropriate tools and techniques specific to their domain.
CO4	:	Communicate, work in teams and demonstrate the learning through oral presentations and report writing.

Scheme of Continuous Internal Evaluation (CIE):

The evaluation committee shall consist of Guide, Professor, Associate Professor/Assistant Professor. The committee shall assess and evaluate the presentation and the progress reports.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
I	Approval of the selected topic, formulation of Problem Statement and Objectives along with Synopsis submission	10%
II	Demonstrate the skill and knowledge by applying appropriate tools/techniques to design solution specific to the problem.	30%
III	Demonstrates the work carried out through experimental results, analysis and testing. Exhibits writing and communication skills through presentations and report writing.	60%

Scheme for Semester End Evaluation (SEE):

The SEE examination shall be conducted by an external examiner (domain expert) and an internal examiner. Evaluation shall be done in batches, not exceeding 6 students per batch.
RUBRICS FOR SEMESTER END EXAMINATION
The SEE examination shall be conducted by an external examiner (domain expert) and an internal examiner.

Q.NO.	**CONTENTS**	Marks
1	Write Up	20%
2	Demonstration of Minor Project Work	60%
3	Viva voce	20%

SEMESTER: III					
INTERNSHIP					
Course Code	**:**	**MVE434N**		**CIE Marks**	**50**
Credits L:T:P	**:**	**0:0:6**		**SEE Marks**	**50**
Hours/Week	**:**	**23**		**SEE Duration**	**03 Hrs**

Guidelines

1. Students can opt for undergoing internship at the industry or research organizations like BEL, DRDO, ISRO, NAL, etc.
2. Students must submit letter from the industry/research organizations clearly specifying the candidate's name and the duration of the internship on the company letter head with authorized signature.
3. The duration of the internship shall be for a period of 6 weeks on full time basis after II semester final exams and before the commencement of III semester.
4. RVCE hosts around 16 Centre of Excellence (CoE) in various domains and around 06 Center of Competence (CoC). The details of these could be obtained by visiting the website https://rvce.edu.in/rvce-center-excellence
5. Students can approach the CoE/CoC for registering and working on relevant domain for training/internship at the CoE/CoC.
6. Internship must be related to the field of specialization of the respective PG program in which the student has enrolled.
7. Students undergoing internship training are advised to report their progress and submit periodic progress reports/diary to their respective guides.
8. Students have to present the internship activities carried out to the departmental committee and only upon approval by the committee, the student can proceed to prepare and submit the hard copy of the final internship report.
9. The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be softbound in Ivory/White color for PG circuit Programs and Light Blue for Non-Circuit Programs.

Course Outcomes: After completing the course, the students will be able to

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Explore the workplace, operating procedures of the department/company and its products, and other organizational concepts.
CO2	:	Learn and improve writing and communication skills, research and technology, work in a team, and develop leadership skills.
CO3	:	Apply higher order thinking skills - critical thinking, analysis, synthesis and evaluate complex problems to solve real world problems with professional ethical standards.
CO4	:	Develop and demonstrate skill competencies and knowledge specific to program specialization by applying appropriate tools and techniques.

Scheme of Continuous Internal Evaluation (CIE):

The evaluation committee shall consist of Guide, Professor, Associate Professor/Assistant Professor. The committee shall assess and evaluate the presentation and the progress reports.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
I	Ability to comprehend the functioning/operating procedures of the Organization/Departments. Application of Engineering knowledge, Critical thinking and analysis to solve problems.	40%

II	Demonstrates skill competencies, Resource Management and Sustainability. Exhibits writing and communication skills through presentations and report writing.	60%

Scheme for Semester End Evaluation (SEE):

The SEE examination shall be conducted by an external examiner (domain expert) and an internal examiner. Evaluation shall be done in batches, not exceeding 6 students per batch.

RUBRICS FOR SEMESTER END EXAMINATION

The SEE examination shall be conducted by an external examiner (domain expert) and an internal examiner.

Q.NO.	CONTENTS	MARKS
1	Write Up	**20%**
2	Demonstration of Internship Work	**60%**
3	Viva	**20%**

SEMESTER: IV						
Course Code	:	MVE341F1	**VLSI DESIGN FLOW: RTL to GDS**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	24L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 12 Weeks

Week 1: Basic Concepts of Integrated Circuit: Structure, Fabrication, Types, Design Styles, Designing vs. Fabrication, Economics, Figures of Merit Overview of VLSI Design Flow: Design Flows and Abstraction; Pre-RTL Methodologies: Hardware-software Partitioning, SoC Design, Intellectual Property (IP) Assembly, Behavioral Synthesis

Week 2: Overview of VLSI Design Flow: RTL to GDS Implementation: Logic Synthesis, Physical Design; Verification and Testing; Post-GDS Processes

Week 3: Hardware Modeling: Introduction to Verilog Functional verification using simulation: testbench, coverage, mechanism of simulation in Verilog

Week 4: RTL Synthesis: Verilog Constructs to Hardware Logic Optimization: Definitions, Two-level logic optimization

Week 5: Logic Optimization: Multi-level logic optimization, FSM Optimization Formal Verification: Introduction, Formal Engines: BDD, SAT Solver

Week 6: Formal Verification: Model Checking, Combinational Equivalence Checking Technology Library: Delay models of Combinational and Sequential Cells

Week 7: Static Timing Analysis: Synchronous Behavior, Timing Requirements, Timing Graph, Mechanism, Delay Calculation, Graph-based Analysis, Path-based Analysis, Accounting for Variations

Week 8: Constraints: Clock, I/O, Timing Exceptions Technology Mapping Timing-driven Optimizations

Week 9: Power Analysis, Power-driven Optimizations Design for Test: Basics and Fault Models, Scan Design Methodology

Week 10: Design for Test: ATPG, BIST Basic Concepts for Physical Design: IC Fabrication, FEOL, BEOL, Interconnects and Parasitics, Signal Integrity, Antenna Effect, LEF files

Week 11: Chip Planning: Partitioning, Floorplanning, Power Planning Placement: Global Placement, Wirelength Estimates, Legalization, Detailed Placement, Timing-driven Placement, Scan Cell Reordering, Spare Cell Placement

Week 12: Clock Tree Synthesis: Terminologies, Clock Distribution Networks, Clock Network Architectures, Useful Skews Routing: Global and Detailed, Optimizations Physical Verification: Extraction, LVS, ERC, DRC, ECO and Sign-off

Course duration: 12 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors:Prof. Sneh Saurabh**,** IIIT Delhi
Reference Textbook: "Introduction to VLSI Design Flow" by Sneh Saurabh

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on

NPTEL website http://nptel.ac.in/

4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

SEMESTER: IV						
Course Code	:	MVE341F2	**PHASED- LOCKED LOOP**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	24L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 12 Weeks

Week 1: Basic concepts in PLL, Simple PLL
Week 2: Small Signal Analysis of Type-I/II/III PLLs for Phase Step, Frequency Step and Frequency Ramp Frequency acquisition in Type-I PLLs acquisition in Type-II PLLs, Clock multipliers, Analog phase error detectors
Week 4: Digital phase error detectors, Range extension for phase error detectors, Phase frequency detector, Digital
Week 5: Problems in charge-pump PLL, Design procedure for Type-II Order 3 charge-pump PLL, Design procedure for charge pump clock multiplier, Sources of non-linearities in CP-PLL, Noise analysis in CP-PLL
Week 6: Noise analysis in CP-PLL (continued), Design of PLL building blocks: Introduction to oscillators
Week 7: Design of PLL building blocks: Ring oscillators
Week 8: Design of PLL building blocks: Ring oscillators (continued), Supply regulated oscillators
Week 9: Phase noise in ring oscillators, Design of PLL building blocks: PFD
Week 10: Design of PLL building blocks: Charge-pump, Circuit-level design of clock frequency divider
Week 11: Techniques for wide frequency range clock multiplier, Digital PLLs
Week 12: Noise analysis in digital PLLs, Analog/Digital Hybrid PLL

Course duration: 12 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors:Prof. Saurabh Saxena ,IIT Madras
Reference Textbook: "Phase-Locked Loops: Theory and Applications" by Roland E. Best

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

SEMESTER: IV						
Course Code	:	MV341F3	**VLSI DATA CONVERSION CIRCUITS**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	16L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 8 Weeks

Week 1: Introduction to A/D and D/A conversion
Week 2: Sampling, quantization, quantization noise, aliasing and reconstruction filtering
Week 3: ADC/DAC metrics : Differential and Integral Nonlinearity, SNR, SNDR, SFDR and dynamic range.
Week 4: ADC Architectures
Week 5: (a) Flash and Floding ADCs. (b) Oversampling Converters.
Week 6: (c) Successive Approximation Converters.
Week 7: DAC Design
Week 8: (a) Current steering DACs.

Course duration: 8 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors:Dr. Shanthi Pavan, IIT Madras
Reference Textbook: "CMOS Data Converters for Communications" by Mikael Gustavsson, J. Jacob Wikner

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

SEMESTER: IV						
Course Code	:	MVE341F4	**MULTI-CORE COMPUTER ARCHITECTURE**	CIE Marks	:	NA
Credits L-T-P	:	2-0-0	*(Theory - NPTEL Online Course)*	SEE Marks	:	50
Hours	:	24L		SEE Duration	:	2 Hrs

This course is indicative only and it is subject to change based on the courses running at that time by NPTEL

Duration of the ONLINE Course - 12 Weeks

Week 1: Basic Computer Organization
Week 2: Instruction Pipeline Principles
Week 3: Pipeline Hazards and Branch Prediction Techniques
Week 4: Pipeline Scheduling and Speculative execution
Week 5: Superscalar Processors and GPU architectures
Week 6: Cache Memory Principles
Week 7: Cache Memory Optimizations
Week 8: Cache Coherence Protocols
Week 9: Primary Storage Systems
Week10: Tiled Chip Multi-Core Processors & Network-on-Chip
Week 11: Energy Efficient NoCs
Week 12: Quality of Service for TCMPs

Course duration: 8 Weeks
Course start Date: Jan 20,2025
Course end date: March 14,2025
Probable Exam date: March 22,2025
Course Instructors: Prof. John Jose, IIT Guwahati
Reference Textbook: "Multi-Core Computer Architecture" by Prof. John Jose

GENERAL GUIDELINES

1. NPTEL is an acronym for National Programme on Technology Enhanced Learning which is an initiative by seven Indian Institutes of Technology (IIT Bombay, Delhi, Guwahati, Kanpur, Kharagpur, Madras and Roorkee) and Indian Institute of Science (IISc) for creating course contents in engineering and science.
2. NPTEL is offering online certification courses through its portal -https://swayam.gov.in/nc_details/NPTEL
3. Enrollment to courses and exam registration can be done in ONLINE mode only. The link is available on NPTEL website http://nptel.ac.in/
4. Students need to enroll for the NPTEL course and clear the exam.
5. In case students fail to get the certificate, they need to enroll for the same course once again, in the subsequent NPTEL semester and clear the exam.
6. If the same course is not offered by NPTEL (i.e. if the same course is not re-run) in the subsequent semester by NPTEL, the students need to write letter seeking permission from the Counsellor, HoD and Dean Academics with further approval from BoS Committee to take alternative course from the list announced by NPTEL.
7. Exam is conducted by NPTEL.

SEMESTER: IV					
MAJOR PROJECT					
Course Code	:	**MVE442P**		**CIE Marks**	**100**
Credits L:T:P	:	**0:0:18**		**SEE Marks**	**100**
Hours/Week	:	**42**		**SEE Duration**	**03 Hrs**

Guidelines

1. Major Project is to be carried out for a duration of 18
2. weeks
3. Student have to implement the Major Project individually.
4. Students are required to select topics related to their PG Program Specialization after extensive Literature Survey and analyzing the Research gaps.
5. Students will be assigned to guides in accordance with the expertise of the faculty.
6. Major project topics could also be chosen to be implemented/executed based on any of the 16 Centre of Excellence (CoE)/ 06 Center of Competence (CoC) domain. The details of these could be obtained by visiting the website https://rvce.edu.in/rvce-center-excellence
7. Major Project could be implemented in Industry/Research organizations after providing the letter of approval. Students can also implement Major Project, in-house using the resources available in the department/college/CoE/CoC.
8. Students have to adhere to the Project Presentation Schedule note the periodic progress in the Major Project Diary and report the work carried to their respective guides.
9. It is mandatory for the students to present/publish their project work in National/International Conferences/Journals
10. Students have to present the Major Project work to the departmental committee and only upon approval by the committee, the student can proceed to prepare and submit the hard copy of the final Major Project report.
11. Major Project report has to be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be softbound in Ivory/White color for PG circuit Programs and Light Blue for Non-Circuit Programs.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Analyze the research gaps, formulate the problem definition, conceptualize the objectives and design solution to cater to specific problems.
CO2	:	Apply higher order thinking skills and develop skill competencies specific to program specialization to implement real world problems with professional ethical standards.
CO3	:	Demonstrate the skill and knowledge by applying appropriate tools and techniques specific to their domain.
CO4	:	Communicate, work in teams and demonstrate the learning through oral presentations and report writing.

Scheme of Continuous Internal Evaluation (CIE):
The evaluation committee shall consist of Guide, Professor, Associate Professor/Assistant Professor. The committee shall assess and evaluate the presentation and the progress reports.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
I	Selection of Project Title, Formulation of Problem Statement and Objectives	**20%**
II	Design, Implementation and Testing	**40%**
III	Experimental Result & Analysis, Conclusions and Future Scope of Work, Report Writing and Paper Publication	**40%**

Scheme for Semester End Evaluation (SEE):

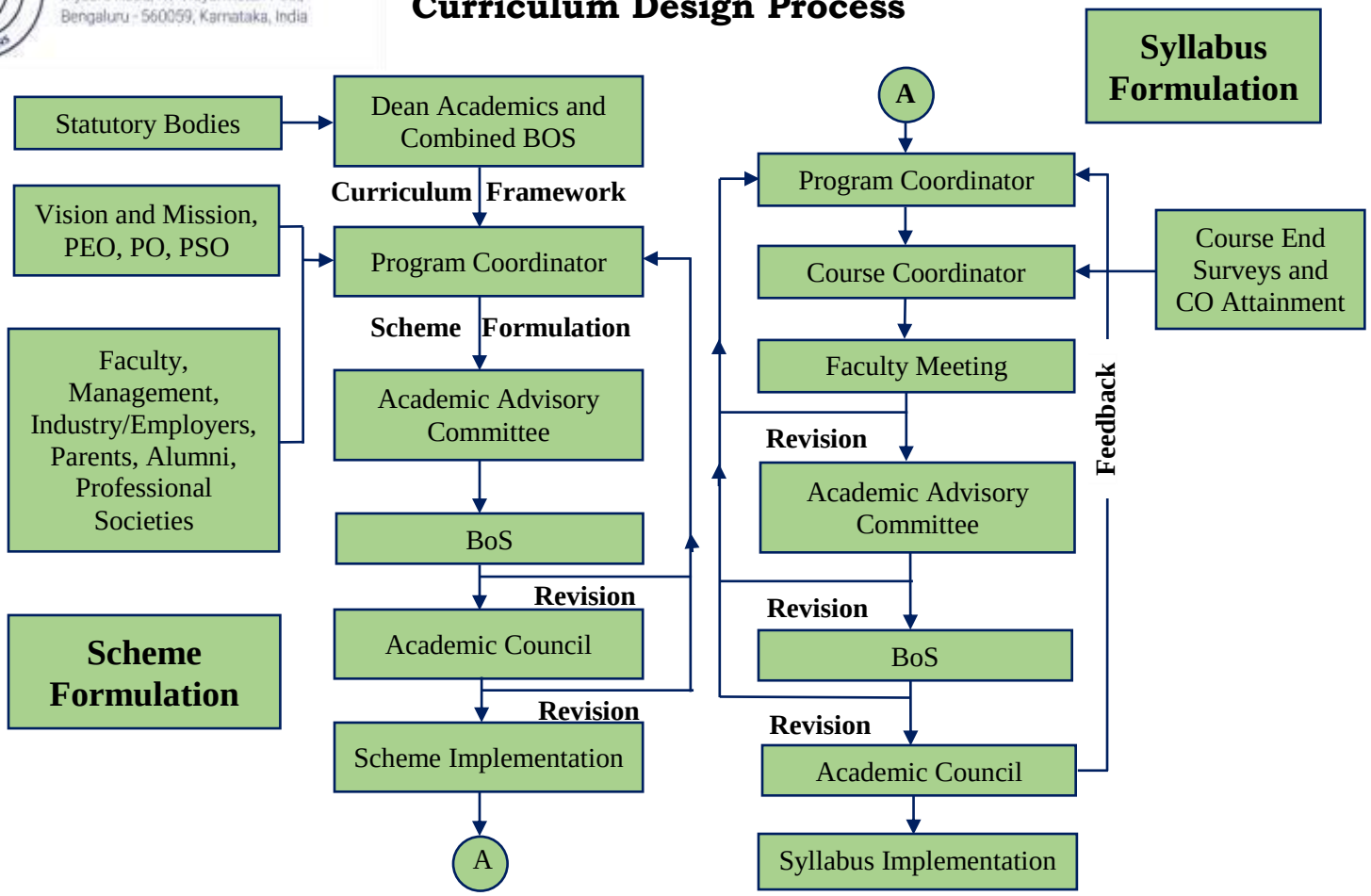
Major Project SEE evaluation shall be conducted in two stages. This is initiated after fulfilment of submission of Project Report and CIE marks.
Stage-1 Report Evaluation: Evaluation of Project Report shall be done by the Guide and an External examiner.
Stage-2 Project Viva-voce: Major Project Viva-voce examination is conducted after receipt of evaluation reports from Guide and External examiner.

RUBRICS FOR SEMESTER END EXAMINATION

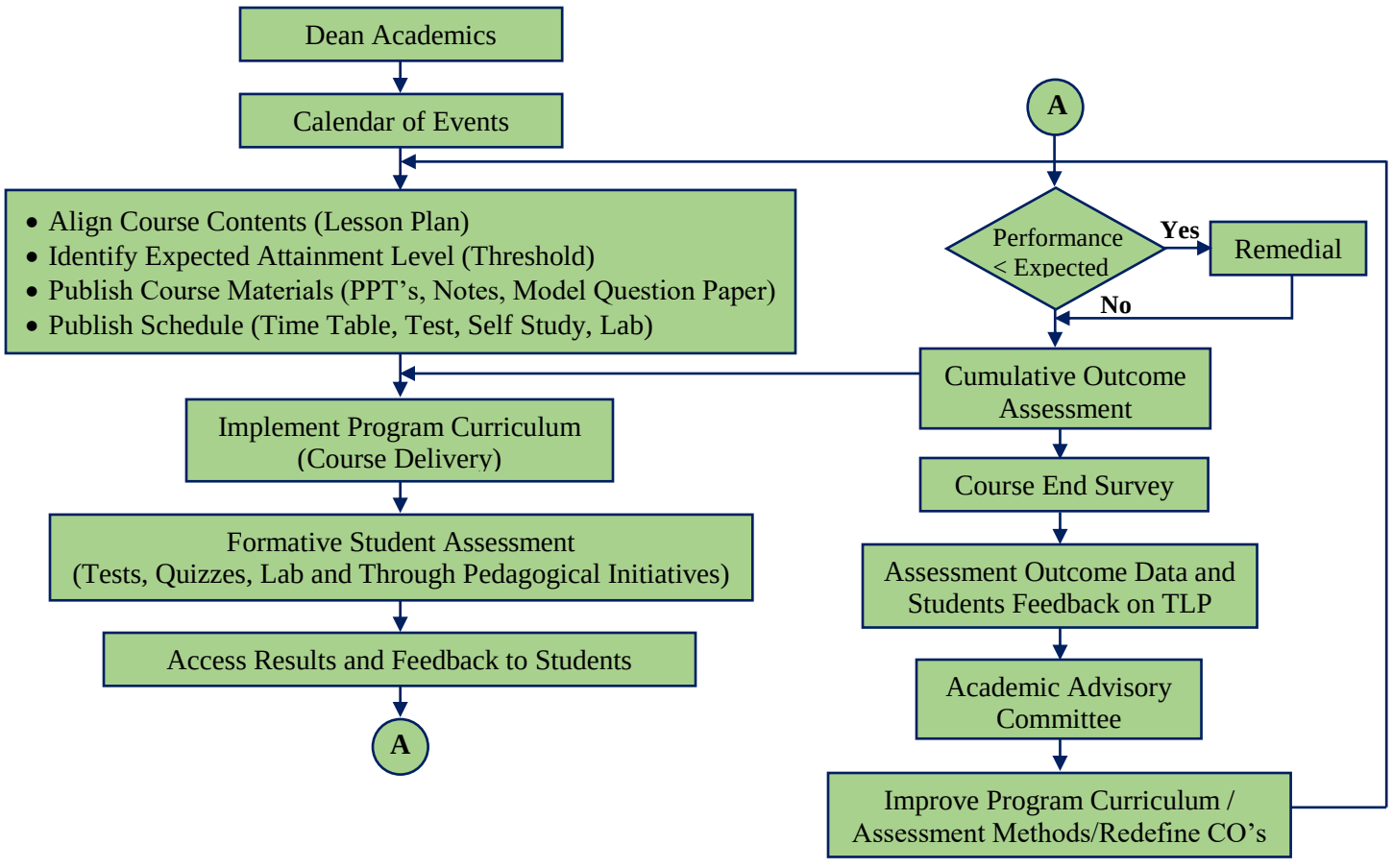
SEE procedure is as follows:

Report Evaluation	Internal Examiner: 100 Marks External Examiner: 100 Marks	**200 M/2=100M (A)**
Viva-Voce	Jointly evaluated by Internal Guide & External Evaluator	**100 M (B)**
Total Marks = (A + B) / 2 = 100		

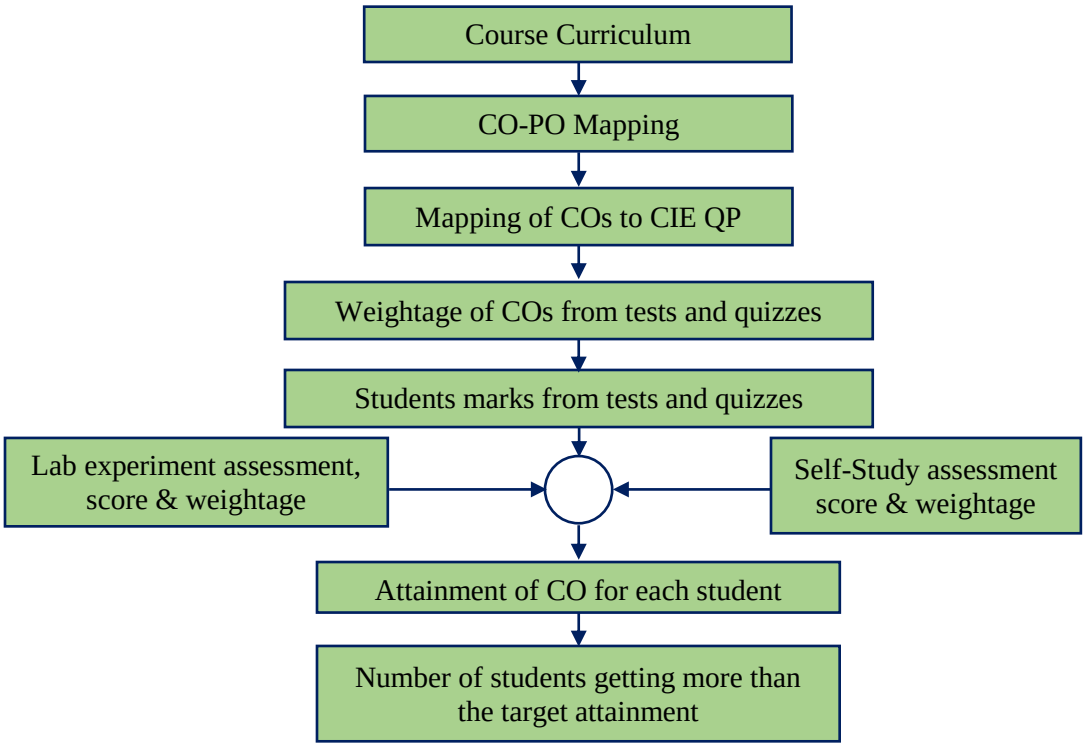
Curriculum Design Process



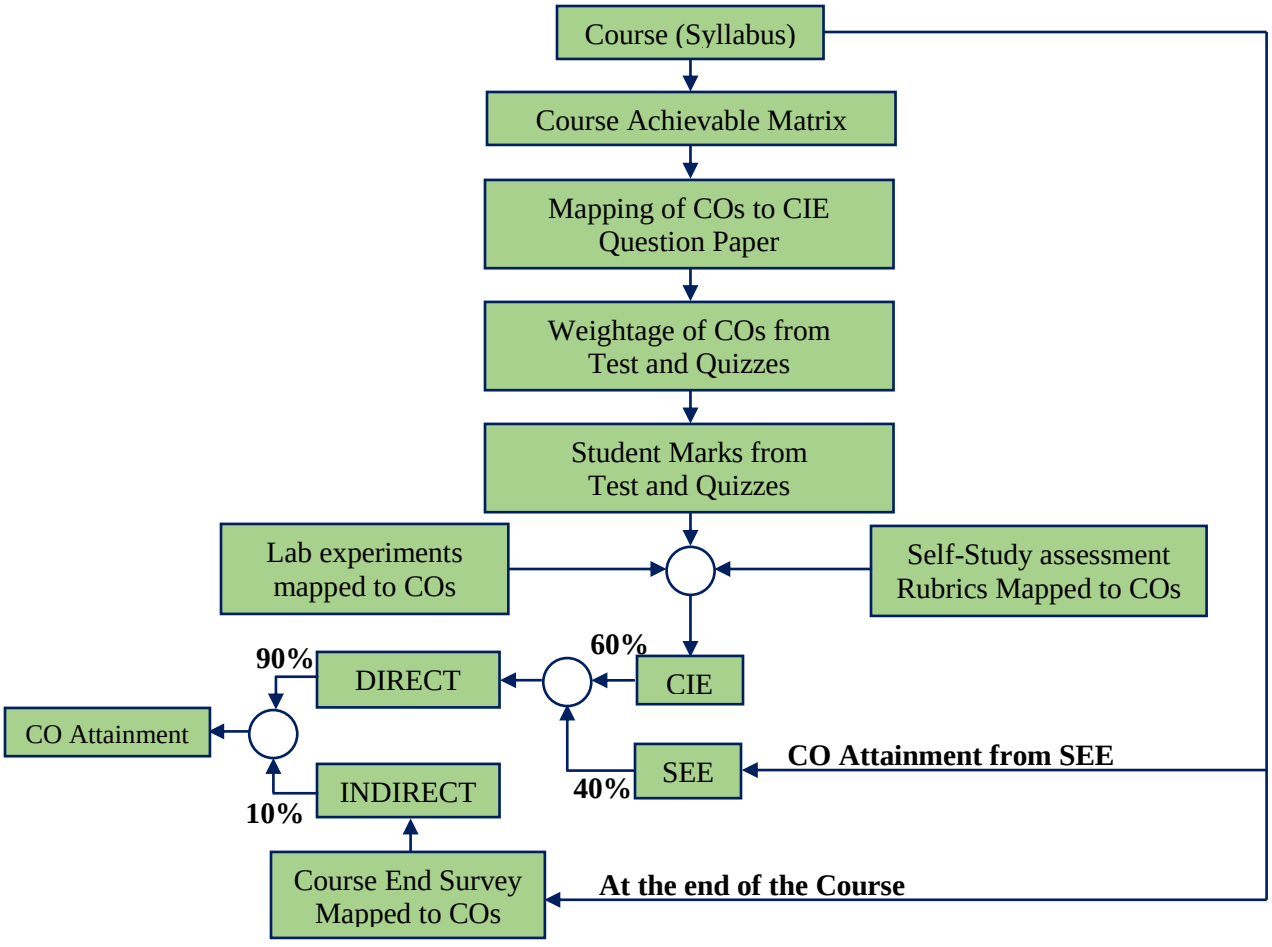
Academic Planning and Implementation



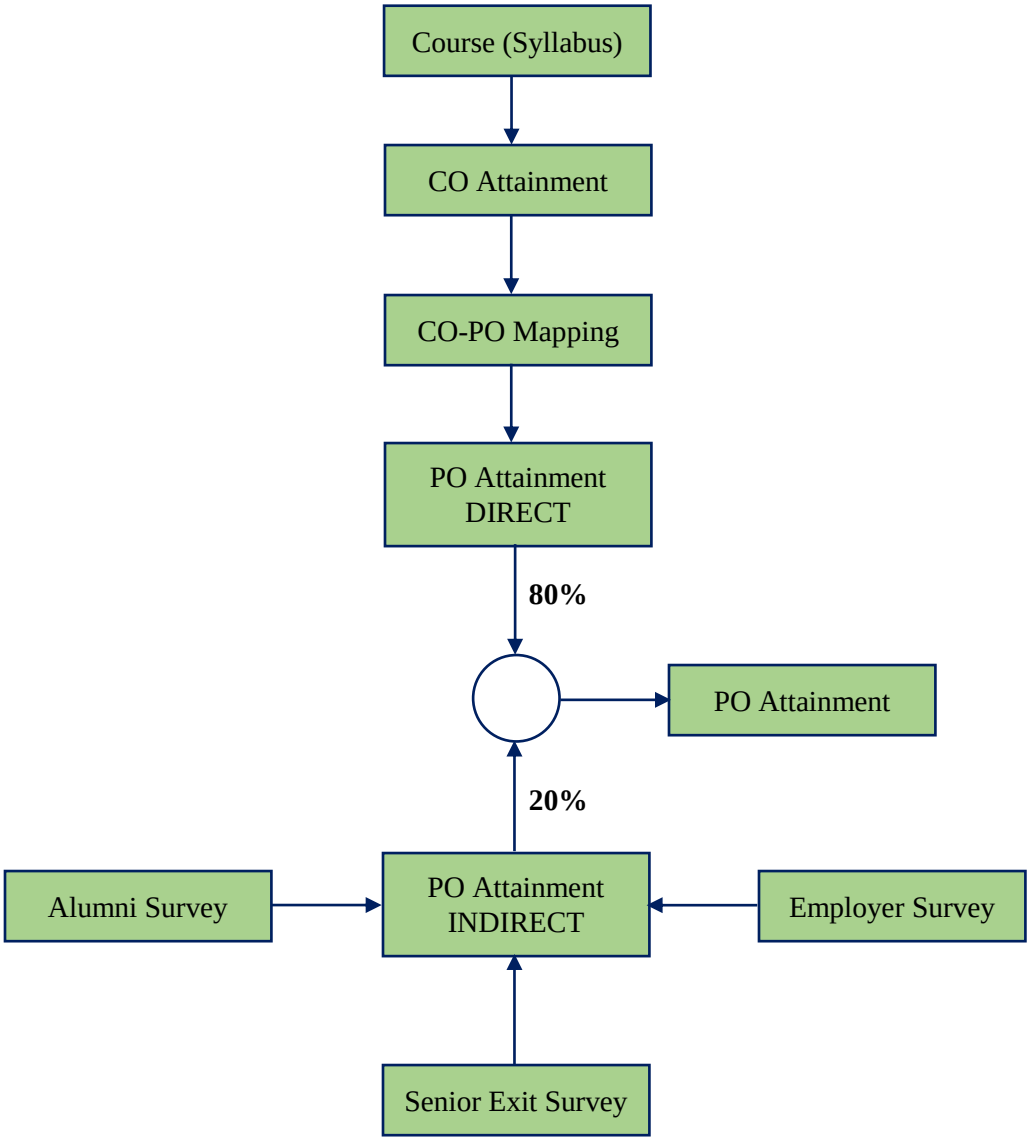
Process For Course Outcome Attainment



Final CO Attainment Process



Program Outcome Attainment Process



RV College of Engineering®
Mysore Road, RV Vidyaniketan Post,
Bengaluru - 560059, Karnataka, India

KNOWLEDGE & ATTITUDE PROFILE

- **WK1:** A systematic, theory-based understanding of the natural sciences applicable to the discipline and awareness of relevant social sciences.
- **WK2:** Conceptually-based mathematics, numerical analysis, data analysis, statistics and formal aspects of computer and information science to support detailed analysis and modelling applicable to the discipline.
- **WK3:** A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline.
- **WK4:** Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline.
- **WK5:** Knowledge, including efficient resource use, environmental impacts, whole-life cost, re-use of resources, net zero carbon, and similar concepts, that supports engineering design and operations in a practice area.
- **WK6:** Knowledge of engineering practice (technology) in the practice areas in the engineering discipline.
- **WK7:** Knowledge of the role of engineering in society and identified issues in engineering practice in the discipline, such as the professional responsibility of an engineer to public safety and sustainable development.
- **WK8:** Engagement with selected knowledge in the current research literature of the discipline, awareness of the power of critical thinking and creative approaches to evaluate emerging issues.
- **WK9:** Ethics, inclusive behaviour and conduct. Knowledge of professional ethics, responsibilities, and norms of engineering practice. Awareness of the need for diversity by reason of ethnicity, gender, age, physical ability etc. with mutual understanding and respect, and of inclusive attitudes.

INNOVATIVE TEAMS OF RVCE

Ashwa Mobility Foundation (AMF): Designs and fabricates Formula-themed race cars and mobility solutions to address urban transportation issues.

Astra Robotics Team: Focuses on designing and building application-specific robots.

Coding Club: Helps students gain coding skills and succeed in competitions like GSoC and ACM-ICPC.

Entrepreneurship Development Cell (E-Cell): Promotes entrepreneurship through workshops, speaker sessions, and mentoring for startups.

Frequency Club Team: Works on software and hardware, emphasizing AI and Machine Learning.

Team Garuda: Develops a supermileage urban concept electric car and E-mobility products.

Team Jatayu: Builds low-cost UAVs with autonomous capabilities for various tasks.

Solar Car Team: Aims to create a solar electric vehicle for sustainable transportation.

Team Antariksh: Focuses on space technology and the development of operational rockets.

Team Chimera: Builds a Formula Electric Car through R&D in E-Mobility.

Helios Racing Team: Designs and tests All-Terrain Vehicles, participating in SAE's BAJA competitions.

Team Hydra: Develops autonomous underwater vehicles for tasks like water purification.

Team Krushi: Creates low-cost farming equipment to assist farmers in cultivation and harvesting.

Team Vyoma: Designs and tests radio-controlled aircraft and UAVs.

Team Dhruva: Engages in astronomy-related activities and collaborates on projects with organizations like ICTS and IIA.

Ham Club: Promotes Amateur Radio and explores technical innovations in communications, especially for disaster response.

Cultural Activity Teams

1. AALAP (Music club)
2. DEBSOC (Debating society)
3. CARV (Dramatics club)
4. FOOTPRINTS (Dance club)
5. QUIZCORP (Quizzing society)
6. ROTARACT (Social welfare club)
7. RAAG (Youth club)
8. EVOKE (Fashion team)
9. f/6.3 (Photography club)
10. CARV ACCESS (Film-making

NSS of RVCE

NCC of RVCE

VISION

Leadership in Quality Technical Education, Interdisciplinary Research & Innovation, with a Focus on Sustainable and Inclusive Technology

MISSION

- To deliver outcome based Quality education, emphasizing on experientiallearning with the state of the art infrastructure.
- To create a conducive environment for interdisciplinary research and innovation.
- To develop professionals through holistic education focusing on individual growth, discipline, integrity, ethics and social sensitivity.
- To nurture industry-institution collaboration leading to competency enhancement and entrepreneurship.
- To focus on technologies that are sustainable and inclusive, benefiting all sections of the society.

QUALITY POLICY

Achieving Excellence in Technical Education, Research and Consulting through an Outcome Based Curriculum focusing on Continuous Improvement and Innovation by Benchmarking against the global Best Practices.

CORE VALUES

Professionalism, Commitment, Integrity, Team Work, Innovation