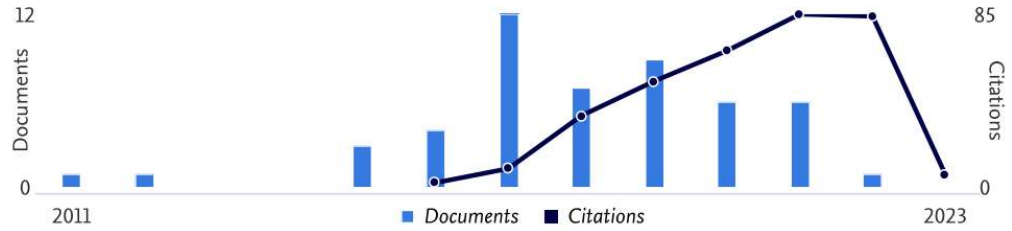
Dr. H V R Aradhya, Prof and Head, ECE, Paper Publication Details:

Papers published in Journals/Conferences: Total - - 161

S. No	Dr. HVR – Author Profile/Credentials can be viewed at	Publisher
1	http://www.scopus.com/authid/detail.url?authorId=55616592800 As on 27/03/2023 and http://orcid.org/0000-0003-3076-9120 Aradhya, H. V.Ravish Department of Electrical & Computer Engineering, Bengaluru, India https://orcid.org/0000-0003-3076-9120 497 Citations by 392 documents 56 Documents 12 h-index View h-graph View more metrics Document & citation trends 	Scopus
2	https://publons.com/dashboard/records/publication/authored/ As on 27/03/2023 and Researcher ID: 0-6994-2016.	WOS

	 Ravish Aradhya H. V "Aradhya H V Ravish" Web of Science ResearcherID O-6994-2016 Faculty - Electronics and Communication Engineering, R V College of Engineering, Bangalore Profile summary 78 Total documents 28 Publications indexed in Web of Science 28 Web of Science Core Collection publications 0 Preprints 0 Dissertations or Theses 50 Non-indexed publications 0 Verified peer reviews 0 Verified editor records Web of Science Core Collection metrics 5 H-Index 28 Publications 111 Sum of Times Cited 103 Citing Articles 0 Sum of Times Cited by Patents 0 Citing Patents a	
3	https://www.semanticscholar.org/author/H.-V.-Ravish-Aradhya/19255649 https://www.semanticscholar.org/author/H.-V.-Ravish-Aradhya/9377770?sort=year As on 27/03/2023 and ORCID: 0000-0003-3076-9120 RAVISH ARADHYA H V RV College of Engineering, Bengaluru 0000-0003-3076-9120 www.rvce.edu.in Publications 38 h-index 12 Citations 371 Highly Influential Citations 8	**Semantic Scholar**
4	https://scholar.google.com/citations?hl=en&user=T0QNp0kAAAAJ	**Google**

	https://scholar.google.com/citations?hl=en&user=C5X7B-AAAAAJ As on 27/03/2023. 10/22/24, 10:21 AM Ravish Aradhya H. V. - Google Scholar  Ravish Aradhya H. V. Professor and Head, Electronics and Communication Engineering, R. V. College of Low Power VLSI design and Embedded … All Since 2019 Citations 789 618 h-index 14 10 i10-index 20 11	**Scholar**
	Published by	**Number**
1.	**International Journals**	**50**
2.	**International Conferences**	**85**
3.	**National Conferences**	**24**
4.	**National Journals**	**00**
5.	**PhD Forum**	**03**
	Total Number of Publishes	**162**
IEEE, SPRINGER, ELSEVIER PAPERS		
1	**VLSI Transactions**	**01**
2	**SCI Indexed**	**27**
3	**WOS Indexed**	**77**
4	**Scopus Indexed**	**45**
5	**IEEE Conferences**	**43**
6	**SPRINGER Conferences**	**06**
6	**ELSEVIER Conferences**	**02**

7	**Others**	**60**
BEST PAPER AWARDS - - 04		
1	**Journal – Paper No. 16**	**01**
2	**Conference – Paper No. 10**	**01**
3	**Conference – Paper No. 32 (IEEE Conference)**	**01**
4	**PhD forum presentation @ IISc and IIIT–B Conference -Paper No. 31 and Paper No. 55**	**03**
YEAR WISE PUBLICATIONS		
1.	**Year 2024**	**10**
2.	**Year 2023**	**08**
3.	**Year 2022**	**04**
4.	**Year 2021**	**12**
5	**Year 2020**	**12**
6.	**Year 2019**	**16**
7.	**Year 2018**	**12**
8.	**Year 2017**	**09**
9.	**Year 2016**	**16**
10.	**Year 2015**	**15**
11.	**Year 2014**	**04**
12.	**Year 2013**	**04**
13.	**Year 2012**	**15**

14.	**Year 2011**	**07**
15.	**Year 2010**	**04**
16.	**Year 2009**	**07**
17.	**Year 2008**	**01**
18	**Year 2007**	**01**
	Total Publications	**157**
	To be published	**04**

Important Publications:

1. Ravish Aradhya H V, Arunkumar P C, Shrish Shrinath Vaidya, Sanket M Mantrashetti, Abhishek G Dastikopp, Kishan S Murthy, Prakash Pawar (IIIT, Dharwad, India), **"A Novel TriNet Architecture for Enhanced Analog IC Design Automation", *IEEE Transactions on Very Large Scale Integration Systems,*** Sep 2024. No. TVLSI-00159-2024.R2 (Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10672521)
2. H V Ravish Aradhya, Wafa Naaz Shaik, Nandu Saseendran, **, "Digital Intellectual Property Verification using Universal Verification Methodology,"** International Journal of Creative Research Thoughts (IJCRT), Vol. 12, Issue. 06, June 2024, ISSN: 2320-2882, pp. C372-C377. (UGC approved).
   (Download Link: https://ijcrt.org/papers/IJCRT2406258.pdf)
3. H V Ravish Aradhya, Neethu S, **"Evaluation of distributed denial of service attacks detection in software defined networks,"** IAES International Journal of Artificial Intelligence (IJ-AI), Vol. 13, No. 4, October 2024, pp. 4488~4498, ISSN: 2252-8938, DOI: 10.11591/ijai.v13.i4.pp4488-4498, **(Q2 Journal). (Scopus indexed).**
   (Download Link: https://ijai.iaescore.com/index.php/IJAI/article/view/24988/14270)
4. Ravish Aradhya H. V. Gopal Kanase gplkanase@gmail.com Vinayakgouda Y G vinayakgouda1997@gmail.com, **"RTL to GDSII of Harvard Structure RISC Processor"** 2021 IEEE International Conference on Electronics, Computing and Communication Technologies (**CONECCT-2021**), 978-1-6654-2849-1/21/$31.00 ©2021 IEEE, **DOI: 10.1109/CONECCT52877.2021.9622735**.

(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9622735)

5. Ravish Aradhya H V, Arunkumar P C, Shrish Shrinath Vaidya, Sanket M Mantrashetti, Abhishek G Dastikopp, Kishan S Murthy, Prakash Pawar (IIIT, Dharwad, India), **"Integrating Neural Network Models for Advanced Automation in Analog Amplifier Circuit Design",** 2024 IEEE International Conference on Electronics, Computing and Communication Technologies (**CONECCT-2024**), Indian Institute of Science, 12-14 July 2024, Circuits, Devices & VLSI pp. 1-6, doi: 10.1109/CONECCT62155.2024.10677072.
(Download Link: https://ieeexplore.ieee.org/document/10677072)

6. Ravish Aradhya H. V, Ashish Kapania, **"Design Space Exploration of Power Efficient Cache Design Techniques,"** Advances in Networks and Communications, Book-1, ISBN: 978-3-642-17878-8_37, SPRINGER Berlin Heidelberg, Jan-2011, Vol. 132, pp. 362-371. DOI: 10.1007/978-3-642-17878-8_37. Part of the Communications in Computer and Information Science book series (CCIS, Volume 132)
(Download link: https://link.springer.com/chapter/10.1007/978-3-642-17878-8_37)

PhD Forum paper Presentations:

1. Mohana, Ravish Aradhya H. V, **"Design and Implementation of Object Detection, Tracking, Counting and Classification Algorithms using Artificial Intelligence for Automated Video Surveillance Applications,"** in Proceedings of ACCS 24th Annual International Conference on Advanced Computing and Communications (ADCOM 2018), pp. 119-122, 21-23 September 2018, at International Institute of Information Technology (IIIT-B), Organized by Advanced Computing and Communication Society (ACCS), Indian Institute of Science (IISc), Bangalore 560012, India, (PhD Forum paper Presentation), https://accsindia.org/adcom-2018-programme/, Published in ACCS open access digital library, https://journal.accsindia.org/.
2. Mohana, Ravish Aradhya H. V, **"Elegant and Efficient Algorithms for Real Time Implementation of Object Detection, Classification, Tracking and Counting using FPGA Zynq XC7Z020 for Automated Video Surveillance Applications,"** 10th IEEE Advanced Networks and Telecommunications Systems (ANTS-2016), 6-9 November 2016, J. N. Tata Auditorium, Indian Institute of Science (IISc), Bangalore, India.
ISBN: 9781509021949; (PhD Forum - Only presentation, not published)

3. Ravish Aradhya H V, Mohana, **"Design of Efficient Algorithms for Video Surveillance Applications using Artificial Intelligence,"** 25th IEEE Advanced Computing and

Communications Conference (ADCOM 2019), 5-7 September 2019, at International Institute of Information Technology (IIIT-B), Bangalore, India. (PhD Forum - Only presentation, this work will not be published)
DOI:10.34048/adcom.2019.phdforumpaper.5, Corpus ID: 219255664

(i) International Journals: 50

1. Ravish Aradhya H. V, Ashish Kapania, **"Design Space Exploration of Power Efficient Cache Design Techniques,"** Advances in Networks and Communications, Book-1, ISBN: 978-3-642-17878-8_37, SPRINGER Berlin Heidelberg, Jan-2011, Vol. 132, pp. 362-371. DOI: 10.1007/978-3-642-17878-8_37. Part of the Communications in Computer and Information Science book series (CCIS, Volume 132)
   (Download link: https://link.springer.com/chapter/10.1007/978-3-642-17878-8_37)
2. Ravish Aradhya H. V, B. V. Praveen Kumar, Dr. K. N Muralidhara, **"Design of Low Power Arithmetic Unit (AU) based on Reversible Logic,"** International Journal of VLSI and Signal Processing Applications (IJVSPA), Vol. 1, Issue 1, ISSN: 2231-3575, Apr-2011, pp. 30- 38.
   (Download Link: http://www.sciencedirect.com/science/article/pii/S1877705812009186)
3. Ravish Aradhya H. V, G Mithun Kumar, Dr. K. N Muralidhara, **"Modelling of complex analog circuits with assertions and automatic processing of Waveforms,"** International Journal of Advanced Engineering Sciences and Technologies (IJAEST), Vol. No. 6, Issue No. 2, pp. 220 – 223, ISSN: 2230-7818, May-2011.
   (Download Link: https://www.researchgate.net/profile/Ravish-Aradhya-H-V/publication/260766686)

4. Ravish Aradhya H. V, G Mithun Kumar, Dr. K. N Muralidhara, **"A Novel assertion based Methodology to verify mixed signal SOC designs in Digital and Mixed signal verification flow,"** International Journal of Engineering Science and Technology (IJEST), ISSN: 0975–5462, Vol. No. 3, Issue No. 6, June 2011, pp. 4721-4727, June-2011.
5. H V Ravish Aradhya, B. V. Praveen Kumar, Dr. K. N Muralidhara, "**Design of Control unit for Low Power ALU Using Reversible Logic,"** International Journal of Scientific and Engineering Research, France, Volume 2, Issue 7, ISSN 2229-5518, Sep-2011, pp. 01-07.

(Download Link: http://www.ijser.org/researchpaper%5CDesign-of-Control-unit-for-Low-Power-ALU-Using-Reversible-Logic.pdf)

6. H V Ravish Aradhya, J. Lakshmesha, Dr. K. N Muralidhara, **"Design Optimization of Reversible Logic Universal Barrel Shifter for Low Power Applications,"** International Journal of Computer Applications, New York, USA, Volume 40, Issue 15, ISSN 0975-8887, Feb-2012, pp. 26-34. (Paper Reference ID**:** pxc3877379)

(Download Link: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.259.783&rep=rep1&type=pdf)

7. H V Ravish Aradhya, G. Rekha, Dr. K. N Muralidhara, **"Simulation and Synthesis of Combinational Shifter using Reversible Gates,"** International Journal of Computer Applications, USA, Vol. 41, Issue 15, ISSN 0975-8887, Mar-2012, pp.26-35 (Paper Reference ID**:** pxc3879354).

(Download Link: https://pdfs.semanticscholar.org/d114/1b0ebcac839372255b37a5496a12be791887.pdf)

8. H V Ravish Aradhya, R. Chinmaye, Dr. K. N Muralidhara, **"Design, Optimization and Synthesis of Efficient Reversible Logic Binary Decoder,"** International Journal of Computer Applications (IJCA), New York, USA, ISSN- 0975-8887, Vol. 46, Issue. 6, May-2012, pp.45-51 (Paper Reference ID**:** pxc3879354).

(Download Link: http://research.ijcaonline.org/volume46/number6/pxc3879354.pdf)

9. H V Ravish Aradhya, H. R. Madan, M. Girish Kumar, V. Ebenezer, **"Considerations of FinFET Based 6T SRAM Cells,"** International Journal of Science Research, Vol. 01, Issue 03, Dec-2012, pp. 134-136.
   (Download Link: http://journal.tumkuruniversity.ac.in:8080/index.php/ijsr/article/view/68)
10. H V Ravish Aradhya, H. R. Madan, M. Akshay Bhounsley, V. Ebenezer, **"Comparative Study of DRAM for High & Low Power CMOS process technology,"** International Journal of Science Research, Vol. 01, Issue 03, Dec-2012, pp. 137-138.
    (Download Link: http://journal.tumkuruniversity.ac.in:8080/index.php/ijsr/article/view/69)
11. H V Ravish Aradhya, H. R. Madan, M. Akshay Bhounsley, V. Ebenezer, **"Comparative Study of SRAM & DRAM for various CMOS process technology,"** International Journal of Science Research, Vol. 01, Issue 03, Dec-2012, pp. 141-143.
    (Download Link: http://journal.tumkuruniversity.ac.in:8080/index.php/ijsr/article/view/72)
12. H V Ravish Aradhya, H. R. Madan, Md. Luqman, K. Suresh, **"Design and Performance Analysis of 8T SRAM for Different Scaled Technologies,"** International Journal of Science Research, Vol. 01, Issue 03, Dec-2012, pp. 151-153.
    (Download Link: http://journal.tumkuruniversity.ac.in:8080/index.php/ijsr/article/view/74)

13. H V Ravish Aradhya, J. Lakshmesha, Dr. K. N Muralidhara, **"Reduced Complexity Hybrid Ripple Carry Look Ahead Adder,"** International Journal of Computer Applications (IJCA), New York, USA, ISSN- 0975-8887, Vol. 70, Issue. 28, May-2013, pp. 13-16. (Paper Reference ID**:** pxc388202).

(Download Link: http://research.ijcaonline.org/volume70/number28/pxc3888202.pdf)

14. H V Ravish Aradhya, G. Rekha, Arun Kumar P. Chavan, **"Bio-Inspired Motion Detector Model Simulated on Xilinx ISE,"** International Journal of Computer Applications (IJCA), New York, USA, ISSN- 0975-8887, Vol. 72, Issue. 13, May-2013, pp.29-32. (Paper Reference ID**:** pxc388202)

(Download Link: http://research.ijcaonline.org/volume72/number13/pxc3889129.pdf)

15. Dr. H V Ravish Aradhya, Srikant M. Pattar, **"Novel Low Power and High Speed 8T-Full Adder,"** International Journal of Scientific and Engineering Research (IJSER), France, ISSN: 2229-5518, Vol. 4, Issue. 8, Aug-2013, pp. 1156-1160. (Paper Reference ID**:** I027256)

(Download Link: http://www.ijser.org/researchpaper/Novel-Low-Power-and-High-Speed-8T-Full-Adder.pdf)

16. Dr. H V Ravish Aradhya, et al, **"Design and Optimization of Reversible carry look ahead Adder Circuit,"** International Journal of Electronics and Communication Engineering (IJECE), ISSN: 2278-991X, Vol. 03, Issue.3, May-2014, pp. 65-72. Received "***Best Paper***" Award (Dated: 09th Dec 2014).

(Download Link: https://issuu.com/iaset/docs/7._electronics_-_ijece_-_design_and)

17. Dr. H V Ravish Aradhya and Roopa H K, **"Comparative study of Bluetooth Testing Automation Tools on Android,"** International Journal of Scientific Engineering and Technology Research, ISSN: 2319-8885, Vol. 3, Issue.15, June-2014, pp. 3196-3198.

(Download Link: http://ijsetr.com/uploads/425316IJSETR1639-545.pdf)

18. Dr. H V Ravish Aradhya, et al, **"Design and Verification of Analog Phase Locked Loop Circuit,"** International Journal of Combined Research and Development (IJCRD), ISSN: 2321-225X, Vol. 02, Issue.6, June-2014, pp. 01-05.

(Download Link: http://www.ijcrd.com/files/vol_2_issue_6/4627.pdf)

19. Dr. H V Ravish Aradhya, Aravindkumar D Gumtaj, Mohana, Gouri S Katageri, "**GPS and GSM Based Database Systems for User Access,**" International Journal of Software and Web Sciences (IJSWS), ISSN: 2279-0071, Vol.1, Issue.12, March-May-2015, pp. 24-28. STEM Scientific Online Media and Publishing House, Georgia-31008, USA.

(Download Link: http://iasir.net/IJSWSpapers/IJSWS15-214.pdf)

20. Dr. H V Ravish Aradhya, et al, **"Design and Performance Comparison of finFET, CNFET and GNRFET based 6T SRAM,"** International Journal of Science and Research (IJSR), ISSN: 2319-7064, Vol. 4, Issue. 04, Apr-2015, pp. 24-28.

(Download Link: https://www.ijsr.net/conf/NCKITE2015/162.pdf)

21. Dr. H V Ravish Aradhya, B. V. Vishwas, **"A Novel SRAM Cell Design for Low Power Applications,"** International Journal of Engineering Research and Technology (IJERT), ISSN: 2278-0181, Vol. 04, Issue. 06, June-2015, pp. 1146-1149.

(Download Link: http://www.ijert.org/view-pdf/13570/a-novel-sram-cell-design-for-low-power-applications)

22. Dr. H V Ravish Aradhya, et al, **"GNRFET based 8-Bit ALU,"** International Journal of Electronics and Communication Engineering (IJECE), ISSN: 2278-991X, Vol. 05, Issue. 01, Jan-2016, pp. 65-72. Impact Factor (JCC) - 2015:3.6986; Index Copernicus Value (ICV) - 2015:3.0; NAAS Rating: 3.06.

(Download Link: https://archive.org/details/4.IJECEGNRFETBASED8BITALU)

23. Dr. H V Ravish Aradhya, Ranjit K G, Arunkumar P Chavan, "**Design and Implementation of 8-bit ALU in Sub-Threshold Adiabatic Logic**," International Journal of Communication in Applied Electronics (IJCAE), July 2017, Communications on Applied Electronics (CAE) – ISSN : 2394-4714, Foundation of Computer Science FCS, New York, USA, Volume 7 – No.4, July 2017, pp. 39-43.
(Download Link: https://www.caeaccess.org/archives/volume7/number4/ranjith-2017-cae-652648.pdf)

24. Ravish Aradhya H. V, Sachin M. Revannanavar, **"Analysis, Physical Design and Power Optimization of Block Signal Estimator for High Speed Serial Interface,"** International Journal of Science and Research (IJSR), ISSN (Online): 2319-7064, Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391, Aug 2017. Vol. 06, Issue. 08, pp. 916-920. (Download Link: https://www.ijsr.net/archive/v6i8/ART20176029.pdf)

25. Ravish Aradhya H. V, Manjunatha Rao V, **"Clock Power Optimization in VLSI design at Advanced Technology Nodes,"** International Journal of Computer Applications (IJCA), ISSN: 0975 – 8887, Vol. 169, Issue. 09, July 2017, pp. 29-34.

(Download Link: www.ijcaonline.org/archives/volume169/number9/rao-2017-ijca-914880.pdf)

26. Shreyas H S, Arunkumar P C and Ravish Aradhya H V, "**Design and Analysis of Low Power VCO Enabled Quantizer for CT Sigma Delta ADC**," in the proceedings of International Conference on Advanced Trends in Computer Science & Information Technology (ICATCSIT-18), 24-25 Aug 2018, Geethanjali Institute of Science and Technology, Nellur, AP. (**Scopus Indexed**). Indian Journal of Public Health Research &

Development, Year: 2019, Volume: 10, Issue: 5, pp: 921- 927, Print ISSN: 0976-0245. Online ISSN: 0976-5506, DOI : 10.5958/0976-5506.2019.01197.5 (Download link: https://www.ijour.net/ijor.aspx?target=ijor:ijphrd&volume=10&issue=5&article=174&type=pdf Or http://www.indianjournals.com/ijor.aspx?target=ijor:ijphrd&volume=10&issue=5&article=174)

27. Ravish Aradhya H. V, Apoorva Raghunandan, **"Performance Analysis of Advanced Adders Under Changing Technologies,"** International Journal of Innovations in Engineering and Technology (IJIET), Vol. 12, Issue 2, January 2019, ISSN: 2319-1058, pp. 87-94. DOI: http://dx.doi.org/10.21172/ijiet.122.15 (Download Link: https://ijiet.com/wp-content/uploads/2019/05/151.pdf)
28. Ravish Aradhya H. V, Nehal B, **"Design of Field Area Network on Advanced Metering Infrastructure,"** International Journal of Emerging Technologies and Innovative Research (JETIR), Vol. 12, Issue 2, January 2019, ISSN: 2349-5162, pp. 87-94. (Download Link: https://ijiet.com/.pdf)
29. Dr. Ravish Aradhya H.V, Ganesh Kumar M. T, Sandeep Malik, Madan H. R, **"Implementation and Performance Comparison of CMOS and GNRFET based Advanced Multiplier Designs"**, International Journal of Emerging Technologies and Innovative Research, ISSN:2349-5162, Vol.6, Issue 4, page no. pp1497-1502, April-2019, Publisher: IJ Publication, DOI: http://doi.one/10.1729/Journal.24731 (UGC Care Journal-No 63975) (Download link: http://www.jetir.org/papers/JETIR1904S19.pdf)
30. Ravish Aradhya H. V, Bharath B. Shetty, **"User Service REST API using Spring Boot,"** International Journal of Computer Sciences and Engineering (IJCSE), Vol. 12, Issue 2, May 2019, ISSN: 2347-2697, pp. 87-94.
31. Ravish Aradhya H. V, Gagan A, **"Logic Structure Reduction Scheme for FINFET based TSPC Flip-Flop,"** International Journal of Engineering Research and Technology (IJERT), Vol. 8, Issue 6, Jun 2019, ISSN: 2278-0181, pp. 431-435. DOI : 10.17577/IJERTV8IS060349. (Download link: https://www.ijert.org/research/logic-structure-reduction-scheme-for-finfet-based-tspc-flip-flop-IJERTV8IS060349.pdf)
32. Ravish Aradhya H. V, Mohana, **"Object Detection and Classification Algorithms using Deep Learning for Video Surveillance Applications,"** International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 8, Issue 8, Jun 2019, ISSN: 2278-3075, pp. 386-395, Publisher: Blue Eyes Intelligence Engineering & Sciences Publication.

(**Scopus Indexed**) (Download link: https://www.ijitee.org/wp-content/uploads/papers/v8i8/H6362068819.pdf)

33. Mohana, Ravish Aradhya H V, **"Object Detection and Tracking using Deep Learning and Artificial Intelligence for Video Surveillance Applications,"** International Journal of Advanced Computer Science and Applications(IJACSA); West Yorkshire Vol. 10, Iss. 12, Jun 2019, pp. 517-530, e-ISSN: 2156-5570, p-ISSN: 2158-107X, Dec-2019. DOI:10.14569/IJACSA.2019.0101269 (**Scopus Indexed**).
    Publisher: SAI-The Science and Information Organization. DOI: 10.14569/IJACSA.2019.0101269 (Download link: https://thesai.org/Publications/ViewPaper?Volume=10&Issue=12&Code=IJACSA&SerialNo=69) or https://www.ijitee.org/portfolio-item/H6362068819/)
34. Pragna G, Ravish Aradhya H V, **"Review on Skilled Optimization of Voltage Controlled Oscillator,"** International Journal of Research and Analytical Reviews (IJRAR), Vol. 7, Issue. 2, pp. 330-334, e-ISSN: 2348-1269, p-ISSN: 2349-5138, Jun 2020 (**UGC Approved-Journal No: 43602(19)**). DOI: http://www.ijrar.org/IJRAR19L1566.pdf
    (Download link: https://ijrar.org/viewfull.php?&p_id=IJRAR19L1566)
35. Abhishek R. Deshmukh, Ravish Aradhya H V, **"Experimental analysis of performance metrics for configuration of AutoScaling Groups,"** International Research Journal of Engineering and Technology (IRJET), e-ISSN: 2395-0056, p-ISSN: 2395-0072, Vol: 07 Issue: 05, pp. 1-9, May 2020. (**ISO 9001:2008 Certified Journal**).
    (Download link: https://www.irjet.net/archives/V7/i5/IRJET-V7I5849.pdf)
36. Manjunath K M, Muralidhara K M, HV Ravish Aradhya, **"Binary Multiplier (n-Bit Size) Design, Implementation, Analysis and Comparison of Various Logics,"** International Journal of Advanced Science and Technology, Vol. 29, No. 7, (2020), pp. 8206-8223 (**Elsevier-Scopus indexed**). ISSN: 2005-4238 (Print)
    ISSN: 2207-6360 (Online), Impact Factor: 6.78, Publisher: Science and Engineering Research Support Society
    http://sersc.org/journals/index.php/IJAST/article/view/24645
    (Download link: http://sersc.org/journals/index.php/IJAST/article/view/24645/13005**)**
37. Manjunath K M, Muralidhara K M, Ravish Aradhya H V, **"Incrementer and Decrementer of an N-Bit Input, by a Value 'M' Circuit Design and Analysis for Various Parameters,"** Journal of Critical Reviews (JCR), Vol. 7, Issue 05, June 2020, ISSN: 2394-5125, pp. 1781-1794. (**Scopus indexed**). doi: 10.31838/jcr.07.05.302
    (Download link: https://drive.google.com/file/d/1Rfa8cMoQjMJOJVeXdrPHJcGaVbSdeCAB/view**)**

38. Kiran G Shetty, H V Ravish Aradhya, **"Comparison of Dynamic Voltage Scaling(DVS) of Core Voltage Using the Onboard Voltage Regulator and External Voltage Regulator via I2C Protocol in Automotive Microcontroller,"** Journal of University of Shanghai for Science and Technology, ISSN: 1007-6735, Volume: 23, Issue: 6, (Scopus Indexed), pp: 794-804, https://jusst.org/comparison-of-dynamic-voltage-scalingdvs-of-core-voltage-using-the-on-board-voltage-regulator-and-external-voltage-regulator-via-i2c-protocol-in-automotive-micro-controller/, Jun 2021. (WOS and Scopus Indexed-IEEE)
    (Download Link: https://jusst.org/wp-content/uploads/2021/06/Comparison-of-Dynamic-Voltage-ScalingDVS-of-Core-Voltage-Using-the-On-board-Voltage-Regulator-and-External-Voltage-Regulator-via-I2C-Protocol-in-Automotive-Microcontroller.pdf)
39. Kiran G Shetty, H V Ravish Aradhya, **"Instruction Based Power Estimation Method in AURIX Microcontroller,"** Journal of University of Shanghai for Science and Technology, ISSN: 1007-6735, Volume: 23, Issue: 6, (Scopus Indexed), pp: 784-793, https://jusst.org/instruction-based-power-estimation-method-in-aurix-micro-controller/, Jun 2021.
    (Download Link: https://jusst.org/wp-content/uploads/2021/06/Instruction-Based-Power-Estimation-Method-in-AURIX-Microcontroller.pdf) (WOS and Scopus Indexed-IEEE)
40. Ravish Aradhya H V, Ankitha, **"A Python Based Design Verification Methodology,"** Journal of University of Shanghai for Science and Technology, ISSN: 1007-6735, Volume: 10, Issue: 6, (Scopus Indexed), pp: 901-911, https://jusst.org/a-python-based-design-verification-methodology/, Jun 2021. (WOS and Scopus Indexed-IEEE)
    (Download Link: https://jusst.org/wp-content/uploads/2021/06/A-Python-based-Design-Verification-Methodology.pdf)
41. Ravish Aradhya H V, Deekshith Nayak, **"Orchestrating a Stateful application using Operator,"** Journal of University of Shanghai for Science and Technology, ISSN: 1007-6735, Volume: 23, Issue: 6, (Scopus Indexed), pp: 514-520, https://jusst.org/orchestrating-a-stateful-application-using-operator/, Jun 2021.
    (Download Link: https://jusst.org/wp-content/uploads/2021/06/Orchestrating-a-stateful-application-using-Operator.pdf) (WOS and Scopus Indexed-IEEE)
42. Ravish Aradhya H V, Karthik S Kulkarni, **"MAC Unit Optimization for Area, Power and Timing Constraints,"** International Journal for Research in Applied Science & Engineering Technology (IJRASET), ISSN: 2321-9653, Volume: 9, Issue: 5, pp: 2030-2035, https://doi.org/10.22214/ ijraset.2021.34753, May 2021.
    (Download Link: https://www.ijraset.com/fileserve.php?FID=34753)
43. Ravish Aradhya H V, Kishan Maladkar, **"Design and Implementation of a 32-bit Floating**

Point Unit," International Journal for Research in Applied Science & Engineering Technology (IJRASET), ISSN: 2321-9653, Volume: 9, Issue: 6, pp: 731-736, https://doi.org/10.22214/ ijraset.2021.35052, Jun 2021.
(Download Link: https://www.ijraset.com/fileserve.php?FID=35052)

44. Ravish Aradhya H V, Neethu S**, "Detection of DDoS Attacks in SDN,"** ECS Transactions (IOPscience), ISSN: 1938-5862, 1938-6737, Vol. 107, No. 1, pp: 18305-18313 https://doi.org/10.1149/10701.18305ecst, Apr 2022.
45. Ravish Aradhya H V, Arunkumar P Chavan, **"Ultra Low Power Hybrid Voltage Controlled oscillator for Data Acquisition System"** International Journal of Emerging Trends & Technology in Computer Science (IJETTCS), ISSN: 2278-6856, pp. 1938-6737, Vol: 11, Issue: 4, July-2022 DOI: https://doi.org/10.2749/IJETTCS.1008.2284. **(Scopus indexed)**
(Download Link: https://www.ijraset.com/fileserve.php?FID=35052)??
46. H V Ravish Aradhya, Arunkumar P Chavan**, "Design of 5.1GHz Ultra-Low Power and Wide Tuning Range Hybrid Oscillator,"** International Journal of Electrical and Computer Engineering (IJECE), Vol. 13, No. 4, ISSN 2088-8708, e-ISSN 2722-2578, pp. 3778-3787, DOI: http://doi.org/10.11591/ijece.v13i4, Aug 2023. Institute of Advanced Engineering and Science (IAES), **(Scopus and WOS Indexed)**. (**Q2 Journal**), (Download Link: https://ijece.iaescore.com/index.php/IJECE/search/authors/view?firstName=Arunkumar&middleName=Pundalik&lastName=Chavan&affiliation=RV%20College%20of%20Engineering&country=IN)
47. H V Ravish Aradhya, G Sushanth, **"Hardware in Loop Network Simulators - An Insight Overview"** International Journal of Modeling, Simulation, and Scientific Computing, (**Q2 Journal**), Vol. 15, No. 01, ISSN (print): 1793-9623 | ISSN (online): 1793-9615, pp. 18305--18313 DOI: https://doi.org/10.1142/S1793962324300012, Feb 2023. World Scientific Publisher, **(Scopus and WOS Indexed)**.
(Download Link:
https://www.worldscientific.com/doi/abs/10.1142/S1793962324300012?journalCode=ijmssc)
48. H V Ravish Aradhya, Wafa Naaz Shaik, Nandu Saseendran, **, "Digital Intellectual Property Verification using Universal Verification Methodology,"** International Journal of Creative Research Thoughts (IJCRT), Vol. 12, Issue. 06, June 2024, ISSN: 2320-2882, pp. C372-C377. (UGC approved).
(Download Link: https://ijcrt.org/papers/IJCRT2406258.pdf)
49. Ravish Aradhya H V, Arunkumar P C, Shrish Shrinath Vaidya, Sanket M Mantrashetti, Abhishek G Dastikopp, Kishan S Murthy, Prakash Pawar (IIIT, Dharwad, India), **"A Novel TriNet Architecture for Enhanced Analog IC Design Automation", *IEEE Transactions***

on Very Large Scale Integration Systems, Sep 2024. No. TVLSI-00159-2024.R2 (Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10672521)

50. H V Ravish Aradhya, Neethu S, **"Evaluation of distributed denial of service attacks detection in software defined networks,"** IAES International Journal of Artificial Intelligence (IJ-AI), Vol. 13, No. 4, October 2024, pp. 4488~4498, ISSN: 2252-8938, DOI: 10.11591/ijai.v13.i4.pp4488-4498, **(Q2 Journal)**. **(Scopus indexed).** (Download Link: https://ijai.iaescore.com/index.php/IJAI/article/view/24988/14270)
51. Ravish Aradhya H V, Sushanth G, **"Hardware in,"** International Journal of Advanced Computer Science and Applications (IJACSA) August 2022, Edition (Volume 13 No 8). **(Q2 Journal)**. **(Scopus indexed)** Publisher: IJ Publication
52.

(ii) International Conferences: 85

1. H. V. Ravish Aradhya, Prasad P. Kamat, Dr. K. N. Muralidhara, **"Multi Core ALU – a low power approach,"** in the proceedings of International Conference on Computer, Communication and Instrumentation (3CI-07); RVCE, Bangalore-59, India, 23-25 Nov, 2007.
2. H. V. Ravish Aradhya, V. Swetha, Dr. K. N. Muralidhara, **"Practical Aspects Power Verification & Automation,"** in the proceedings of International Conference on Sensors, security, software& Intelligent systems (ISSSIS-09), CIT, Coimbatore, India, 08-10, Jan 2009.
3. H. V. Ravish Aradhya, Mahesh K, Dr. K. N. Muralidhara, **"Design and Implementation of an Advanced External Interrupt Controller Unit [AEICU] on Cortex-R4 Processor,"** in the proceedings of International Conference on System Dynamics and Control (ICSDC-10); MIT, Manipal, India, 19-22, Aug-2010.
4. H. V. Ravish Aradhya, B. V. Praveen Kumar, Dr. K. N. Muralidhara, **"Design of Control unit for Low Power AU Using Reversible Logic,"** in the proceedings ELSEVIER-International Conference on Communication technology and System design (ICCTSD-2011), AIT, Coimbatore, India., Dec 07-09, 2011. (Download Link: https://www.sciencedirect.com/science/article/pii/S1877705812009186)
5. H. V. Ravish Aradhya, R. Chinmaye, Dr. K. N. Muralidhara, **"Design, Optimization and Synthesis of Efficient Reversible Logic Binary Encoder,"** in the proceedings of International Conference on Recent Trends in Computer Science and Engineering

(ICRTCSE-2012), Apollo College of Engineering, Kanchipuram, TN, India, 07-09, Apr-2012. IJCA, Vol. 46, No. 06, 2012. **DOI: 10.5120/6916-9354**.
(Download Link: https://ijcaonline.org/archives/volume46/number6/6916-9354/)

6. Ravish Aradhya H. V, G. Malleswara Rao, Dr. K. N. Muralidhara, **"FPGA Implementation of IEEE-754, Single Precision Floating Point Arithmetic,"** in the proceedings of International Conference on Recent Trends in Computer Science and Engineering (ICRTCSE-2012), Apollo College of Engineering, Kanchipuram, TN, India, 07-09, Apr-2012.
7. Ravish Aradhya H V, G. Rekha, Arun Kumar P. Chavan, **"Bio-Inspired Motion Detector Model Simulated On Xilinx ISE,"** in the proceedings of International Conference on Information & Communication Engineering (ICICE-2013), ISBN: 978-81-31703-83-2, June-2013, Bangalore, India, pp. 45-50. IJCA, Vol. 72, No. 13, 2013. **DOI: 10.5120/12554-9129**

(Download Link: https://ijcaonline.org/archives/volume72/number13/12554-9129/)

8. Ravish Aradhya H V, Mohana, R. Chethan, R. Shridhar, **"Optical Character Recognition to Speech Conversion,"** in the proceedings of ELSEVIER - 2nd International Conference on Emerging Research in Computing, Information, Communication and Applications (ERCICA-2014), Nitte Meenakshi Institute of Technology, Bangalore, Karnataka, India, 01-02 Aug-2014. Elsevier Science and Technology Publications, ISBN: 9789351072607, pp: 132-136.
9. Ravish Aradhya H V, Mohana, Kiran Anil Chikodi, **"Real Time Objects Detection and Positioning in Multiple Regions Using Single Fixed Camera View for Video Surveillance Applications,"** in the proceedings of IEEE - International Conference on Electrical, Electronics, Signals, Communication and Optimization (EESCO-2015), 24-25 Jan 2015, Vignan's Institute of Information Technology, Duvvada, Visakhapatnam, AP, India. IEEE Explorer: 978-1-4799-7678-2/15/$31.00, ©2015 IEEE, pp:1631-1636, **DOI: 10.1109/EESCO.2015.7253654**.
(Download Link: http://ieeexplore.ieee.org/document/7253654/)
10. Ravish Aradhya H V, Mohana, Nikhil Raju Shalgar, **"Design of Square Spiral Nano-Antenna in Infra-red Region for Solar Energy Harvesting,"** in the proceedings of ***IEEE*** - International Conference on Engineering and Technology (ICETECH-2015), 20 Mar 2015, Rathinam Institute of Technology, Coimbatore, Tamilnadu, India. IEEE: 978-1-4799-7678-2/15/$31.00, ©2015 IEEE, (Conference Record Number: #35961), 20th March 2015, pp: 1026-1031. Received "***Best Paper***" Award (Dated: 20th Mar 2015). **DOI: 10.1109/ICETECH35961.2015**
11. Ravish Aradhya H. V, Mohana, R. Chethan, **"Correlator Based Group Delay Measurement for Delta-DOR Signals,"** in the proceedings of IEEE - Global Conference

on Communication Technologies (GCCT-2015), Noorul Islam University, Kanyakumari district, Tamil Nadu, India. IEEE Explorer: 978-1-4799-8553-1/15/$31.00 ©2015 IEEE, (Conference Record Number: #35855), pp: 419-422, **DOI: 10.1109/GCCT.2015.7342697**.
(Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7342697&isnumber=7342608)

12. Ravish Aradhya H. V, Mohana, R. Sagar, **"Remote Monitoring of Heart Rate and Music to Tune the Heart Rate,"** in the proceedings of IEEE - Global Conference on Communication Technologies (GCCT-2015), Noorul Islam University, Kanyakumari district, Tamil Nadu, India. IEEE Explorer: 978-1-4799-8553-1/15/$31.00 ©2015 IEEE, pp: 678-681.
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7342748)
13. Ravish Aradhya H. V, Mohana, Kiran Anil Chikodi, **"Real Time Object Counting and Classification for Video Surveillance Applications from single fixed camera,"** in the proceedings of 2nd SPRINGER - International Conference on Networking, Information & Communication (ICNIC-2015), 18-20 May 2015, Sri Venkateshwara College of Engineering, Bengaluru, Karnataka, India, pp:1-6.
14. Ravish Aradhya H. V, Mohana, G. S. Pallavi, **"CAP - Ro Translator for UMTS to LTE Protocol Conversion,"** in the proceedings of 2nd SPRINGER - International Conference on Networking, Information & Communication (ICNIC-2015), 18-20 May 2015, Sri Venkateshwara College of Engineering, Bengaluru, Karnataka, India, pp:1-4, **DOI: 10.1109/ICGCIoT.2015.7380535**.
(Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7380535&isnumber=7380415)
15. Ravish Aradhya H. V, Aravindkumar D. Gumtaj, Mohana, **"Real Time Smart, Intelligent and Novel Embedded Vehicle Interceptor for Security Applications,"** in the proceedings of 3rd SPRINGER - International Conference on "Emerging Research in Computing, Information, Communication and Applications (ERCICA-2015), 31st July – August 1st 2015 at NMIT Bangalore, India, pp-521-534. **ISBN978-81-322-2553-9**
(Download Link: https://link.springer.com/chapter/10.1007%2F978-81-322-2553-9_47)
16. Ravish Aradhya H. V, Mohana, G. S. Pallavi, **"CAP to Diameter Protocol Converter,"** in the proceedings of IEEE - International Conference on Green Computing and Internet of Things (ICGCIOT-2015), 08-10 Oct 2015, Galgotias College of Engineering and Technology, Greater Noida, New Delhi, India, pp-598-602. [978-1-4673-7910-6/15/$31.00 ©20 15 IEEE], **DOI: 10.1109/ICGCIoT.2015.7380535**.

(**Download Link: http://ieeexplore.ieee.org/document/7380535/**) **Or**
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7380535&isnumber=7380415)

17. Ravish Aradhya H. V, Mohana, Sagar R, **"Correlator Based Group Delay Measurement for Delta - DOR Signals,"** in the Proceedings of IEEE - Global Conference on Communication Technologies (GCCT 2015), 08-10 Mar 2015, College of Engineering and Technology, Kanyakumari, Tamilnadu, India, pp:419-422. [978-1-4799-8553-1/15/$31.00 © 2015 IEEE]
(**Download Link: http://ieeexplore.ieee.org/document/7342697/**)
18. Ravish Aradhya H. V, Mohana, Sagar R, **"Remote Monitoring of Heart Rate and Music to Tune the Heart Rate,"** in the Proceedings of IEEE - Global Conference on Communication Technologies (GCCT 2015), 08-10 Mar 2015, College of Engineering and Technology, Kanyakumari, Tamilnadu, India, pp:678-681. [978-1-4799-8553-1/15/$31.00 © 2015 IEEE]
(Download Link: http://ieeexplore.ieee.org/document/7342748/)
19. Ravish Aradhya H. V and Karnati Gopi Manohar, **"Multiple Valued Logic (MVL) Based Combinational Building Blocks,"** in the proceedings of IEEE -International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2016), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 20-21 May 2016. Pp: 2088-2092, [978-1-5090-0774-5/16/$31.00 © 2016 IEEE], **DOI: 10.1109/RTEICT.2016.7808207**. (**Scopus Indexed**)
(Download Link: http://ieeexplore.ieee.org/document/7808207/ OR
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7808207&isnumber=7807761)
20. Ravish Aradhya H. V, et al, **"Design, Analysis and Performance comparison of GNRFET based Adiabatic 8-Bit ALU,"** in the proceedings of IEEE - International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2016), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 20-21 May 2016. Pp: 1584-1588, [978-1-5090-0774-5/16/$31.00 © 2016 IEEE], pp. 1584-1588, **DOI: 10.1109/RTEICT.2016.7808099**. (**Scopus Indexed**)
(Ravish Aradhya H V, Madan H R, Suraj M S, Megaraj T Mahadikar, Muniraj R and Mohammed Moiz),
(**Download Link:** http://ieeexplore.ieee.org/document/7808099/ OR
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7808099&isnumber=7807761)
21. Ravish Aradhya H. V, et al, **"Design, Analysis and Performance comparison of GNRFET based 8-Bit ALUs,"** in the proceedings of IEEE - International conference on Recent Advances in Integrated Navigation Systems (RAINS-2016), R. L. Jalappa Institute of

Technology, Doddaballapur, Bengaluru, Pp: 1-6, 6-6, May 2016. (Ravish Aradhya H V, Madan H R, Suraj M S, Megaraj T Mahadikar, Muniraj R and Mohammed Moiz), **DOI: 10.1109/RAINS.2016.7764366**.
(Download Link: http://ieeexplore.ieee.org/document/7764366/ OR http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7764366&isnumber=7764359)

22. Ravish Aradhya H. V, et al, **"Real-Time Implementation of Object Detection and Tracking on DSP for Video Surveillance Applications,"** in the proceedings of IEEE - International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2016), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 20-21 May 2016, pp. 1965-1969, **DOI: 10.1109/RTEICT.2016.7808180**. (Ravish Aradhya H V, Suraj M, Suraj S, Prasad Dongrekar, Srikanth Sajjanar and Mohana), [978-1-5090-0774-5/16/$31.00 © 2016 IEEE]
(Download Link: http://ieeexplore.ieee.org/document/7808180/ OR http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7808180&isnumber=7807761**)**

23. Ravish Aradhya H. V, Smitha G. S, **"mGDI Based Parallel Adder For Low Power Applications,"** in the proceedings of 3rd Springer - International Conference on 'Microelectronics Circuits and Systems' (MICRO-2016), 9-10th July 2016, pp. 26-31, Science City, Kolkata, India. (Organizer: Forum of CCSN).
(Download Link: https://link.springer.com/article/10.1007/s00542-017-3438-1
Or https://link.springer.com/content/pdf/10.1007/s00542-017-3438-1.pdf)
[SCI : Springer-Microsystem Technologies, ISSN: 0946-7076 (Print) 1432-1858 (Online)]

24. Ravish Aradhya H. V, et al, **"Implementation of Real Time Moving Object Detection and Tracking on FPGA for Video Surveillance Applications,"** in the proceedings of IEEE - International conference on Distributed Computing, VLSI, Electrical Circuits, and Robotics (DISCOVER-2016), National Institute of Technology (NITK), Surathkal, Karnataka, 13-14 August 2016, pp. 289-295, **DOI: 10.1109/DISCOVER.2016.7806248**. (Ravish Aradhya H V, Suraj M, Suraj S, Prasad Dongrekar, Srikanth Sajjanar and Mohana)
(Download Link: http://ieeexplore.ieee.org/document/7806248/ OR http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7806248&isnumber=780620)

25. Ravish Aradhya H. V, et al, **"Design and Performance comparison of Adiabatic 8-Bit Multipliers,"** in the proceedings of IEEE - International conference on Distributed Computing, VLSI, Electrical Circuits, and Robotics (DISCOVER-2016), National Institute of Technology (NITK), Surathkal, Karnataka, 13-14 August 2016, pp. 141-147, **DOI: 10.1109/DISCOVER.2016.7806237**.

(Ravish Aradhya H V, Madan H R, Suraj M S, Megaraj T Mahadikar, Muniraj R and Mohammed Moiz)

(Download Link: http://ieeexplore.ieee.org/document/7806237/ OR http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7806237&isnumber=780620)

26. Ravish Aradhya H. V, Suraj K Mankani, Shreekant Sajjanar, Mohana, **"Power and Area Optimization of Decimation Filter for Application in Sigma Delta ADC,"** in the Proceedings of IEEE - International Conference on Circuits, Control, Communication and Computing (I4C-2016), 4-6 October 2016, M. S. Ramaiah Institute of Technology, Bangalore, India, pp. 1-5, **DOI: 10.1109/CIMCA.2016.8053268**.

(Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8053268 OR http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8053268&isnumber=8053250)

27. Guruprasad, Mohana, Ravish Aradhya H. V, **"PAPR Reduction and Performance Analysis of Modulation Techniques in OFDM for WLAN Applications,"** in the Proceedings of IEEE - International Conference on Signal Processing, Communication, Power & Embedded System (SCOPES-2016), 3-5 October 2016, Centurion University, Odisa, India.

(Download Link: ieeexplore.ieee.org/document/7955703/)

28. Mohana, Ravish Aradhya H. V, **"Elegant and Efficient Algorithms for Real Time Object Detection, Counting, and Classification for Video Surveillance Applications from Single Fixed Camera,"** in the Proceedings of IEEE-International Conference on Circuits, Control, Communication and Computing (I4C-2016), pp. 1-7, 4-6 October 2016, M S Ramaiah Institute of Technology, Bangalore, India, **DOI: 10.1109/CIMCA.2016.8053292**.

(Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8053292 OR http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8053292&isnumber=8053250)

29. Mohana, Ravish Aradhya H. V, "**Real Time Implementation of Emotion Detection and Classification system for Autism Patients,"** in the Proceedings of IEEE - International Conference on Advance Computing and Software Engineering (ICACSE-2016), 14-15 October 2016, Kamla Nehru Institute of Technology, Sultanpur, Uttara Pradesh, India.
30. Md. Musharaf Uddin Quraishi, Mohana, H.V. Ravish Aradhya, "**Design of Skin Detection Algorithm Tool for Analysis of Real Time and Non-real Time Images using MATLAB,"** in the Proceedings of IEEE - International Conference on Advance Computing and Software Engineering (ICACSE-2016), 14-15 October 2016, Kamla Nehru Institute of Technology, Sultanpur, Uttara Pradesh, India.

31. Ravish Aradhya H. V, Vidya P. K, Mohana, **"Implementation of Highly Efficient Sorting Algorithm for Median Filtering using FPGA Spartan 6,"** in the proceedings of IEEE - International Conference on 'Innovative Mechanisms for Industry Applications' (ICIMIA-2017), 21-23 Feb 2017, pp. 265-269, Dayananda Sagar College of Engineering, Bengaluru, India. ISBN: 978-1-5090-5960-7/17/$-31.00©2017, Received "***Best Paper***" Award (Dated: 23rd Feb 2017).
    (Download Link: ieeexplore.ieee.org/document/7975614/)
32. Ravish Aradhya H. V, et al, **"Design and Implementation of Low power Mitchell Algorithm based Logarithmic Multiplier,"** in the proceedings of IEEE - International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2017), Sri Venkateshwara College of Engineering, Bengaluru – 562 Electronic ISBN:978-1-5090-3704-9, Print on Demand(PoD) ISBN:978-1-5090-3705-6 157, 19-20 May 2017. pp. 1402-1406, DOI: 10.1109/RTEICT.2017.8256828, ISBN: IEEE: **978-1-5090-3704-9/17/$31.00 © 2017 IEEE**. (Ravish Aradhya H V, Ranjitha H V, and Pooja K S)
    (Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8256828)
33. Ravish Aradhya H. V, et al, **"Sub-threshold Adiabatic Logic (SAL) Based Building Blocks for Combinational System Design,"** in the proceedings of IEEE - International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2017), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 19-20 May 2017. pp. 96-100, ISBN: **978-1-5090-3704-9/17/$31.00 © 2017 IEEE**. (Ravish Aradhya H. V, Ranjit K. G and Arun Kumar P. Chavan)
    (Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8256565)
34. Ravish Aradhya H. V, et al, **"Single Bit-line Low Power 9T Static Random Access Memory,"** in the proceedings of IEEE - International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2017), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 19-20 May 2017. pp. 1943-1947, **ISBN: 978-1-5090-3704-9/17/$31.00 © 2017 IEEE**. (Ravish Aradhya H V, Akshatha P Inamdar and Divya P A)
    (Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8256937)
35. Ravish Aradhya H. V, et al, **"An Area efficient FPGA Implementation of Moving Object Detection and Face Detection using Adaptive Threshold method,"** in the proceedings of IEEE-International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2017), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 19-20 May 2017. pp. 1606-1611, ISBN: **978-1-5090-3704-9/17/$31.00 © 2017 IEEE**. (Ravish Aradhya H V, Vidya P Korakoppa and Mohana)

(Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8256870)

36. Ravish Aradhya H. V, et al, **"Design and Analysis of Compact Printed Circuit Antenna for wireless Medical Telemetry Service,"** in the proceedings of IEEE-International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2017), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 19-20 May 2017. pp. 1139-1142, ISBN: **978-1-5090-3704-9/17/$31.00 © 2017 IEEE**. (Ravish Aradhya H V, Vijayashanth D, Vijith Venugopalan and Mohana)
(Download Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8256776)
37. Ravish Aradhya H. V, N Sameeksha Rai, Arun Kumar P. Chavan, **"Design and implementation of 16 tap FIR filter for DSP Applications,"** in the proceedings of IEEE – 2nd International Conference on Advances in Electronics, Computers and Communications (ICAECC 2018), 09-10 Feb 2018, REVA University, Karnataka, India. DOI: 10.1109/ICAECC.2018.8479480 (**Scopus Indexed**)
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8479480)
38. Apoorva Raghunandan, Mohana Mohana, Pakala Raghav and H.V. Ravish Aradhya, **"Object Detection Algorithms for Video Surveillance Applications,"** in the proceedings of IEEE - 7th International Conference on Communication and Signal Processing (ICCSP 2018), 03-05 April 2018, Melmaruvathur, TN, India. 978-1-5386-3521-6/18/$31.00 ©2018 IEEE, PP. 563-568
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8524461)
39. Akshay Mangawati, Mohana, Mohammed Leesan, H. V. Ravish Aradhya, **"Object Tracking Algorithms for Video Surveillance Applications,"** in the proceedings of IEEE - 7th International Conference on Communication and Signal Processing (ICCSP 2018), 03-05 April 2018, Melmaruvathur, TN, India.
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8524260)
40. Akshatha P. Inmdar, Syed Shadab and H.V. Ravish Aradhya, "**Optimization of Test Register Access Time for Next Generation SoCs,**" in the proceedings of IEEE - International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2018), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 18-19 May 2018. pp. 601 - 605, ISBN: **978-1-5386-2440-1/18/$31.00 © 2018 IEEE.**
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9012237)
41. Akshatha P. Inamdar, Ravish Aradhya H V, "**Low Power Single Bit-line Power-gated SRAM**," in the proceedings of IEEE-International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2018), Sri

Venkateshwara College of Engineering, Bengaluru – 562 157, 18-19 May 2018. pp. 1478-1482, ISBN: **978-1-5386-2440-1/18/$31.00 © 2018 IEEE**.
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9012552)

42. Pooja K S, Ravish Aradhya H V, "**Design and Implementation of Low Power 6:3 Fast Counter based on Symmetric Stacking,**" in the proceedings of IEEE-International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2018), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 18-19 May 2018. pp. 1513-1517, ISBN: **978-1-5386-2440-1/18/$31.00 © 2018 IEEE, DOI: 10.1109/RTEICT42901.2018.9012150**. (**Scopus indexed**)
(Download link: https://ieeexplore.ieee.org/document/9012150)
43. Pooja K S, Sundar Krishnakumar and Ravish Aradhya H V, "**Verification of Interconnection IP for Automobile Applications using SystemVerilog and UVM**" in the proceedings of IEEE-International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2018), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 18-19 May 2018. pp. 1119-1123, ISBN: **978-1-5386-2440-1/18/$31.00 © 2018 IEEE**. DOI: 10.1109/RTEICT42901.2018.9012309. (**Scopus indexed**)
(Download link: https://ieeexplore.ieee.org/document/9012309)
44. Vaishnavi Kumbargeri, and Ravish Aradhya H V, "**Design and Implementation of Logarithmic Multiplier Using FinFETs for Low Power Applications**," in the proceedings of Springer-3rd International Conference on Advanced Trends in Computer Science & Information Technology (ICERECT-18), 24-25 Aug 2018, PES College of Engineering, Mandya, Karnataka, pp: 895-902. Part of the Lecture Notes in Electrical Engineering book series (LNEE, volume 545), **DOI:** https://doi.org/10.1007/978-981-13-5802-9_78, ISBN: 978-981-13-5801-2 (print), 978-981-13-5801- 9 (on-line). (**Scopus Indexed**)
(Download link: https://link.springer.com/chapter/10.1007/978-981-13-5802-9_78)
45. Ravish Aradhya H V, Mohana, "**Simulation of Object Detection Algorithms for Video Survillance Applications**," in the proceedings of IEEE – 2nd International conference on I-SMAC (IoT in Social, Mobile, Analytics and Cloud (I_SMAC-2018), SCAD Institute of Technology, Palladam, Coimbatore, TN, India, 30 - 31 Aug 2018.
(Download link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8653665)
46. Ravish Aradhya H V, M T Ganesh Kumar, Madan H R and Sandeep Malik, "**Design and performance analysis of 8-bit Modified Booth Multiplier**," in the proceedings of IEEE – 3rd International conference on Electrical Electronics, Communication, Computer

Technologies and Optimization Techniques (ICEECCOT-2018), GSSS Institute of Engineering and Technology, Mysuru, Karnataka, India, 14 - 15 Dec 2018. (**Scopus Indexed**)
(Download link: https://www.jetir.org/indexx?v=5&i=9&j=September%202018)

47. Ravish Aradhya H V, Apoorva Raghunandan, **"Area and Timing Analysis of Advanced Adders under changing Technologies,"** in the proceedings of IEEE – 4TH International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2019), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 17-18 May 2019. pp. 33-38**, ISBN: 978-1-7281-0630-4/19/$31.00 © 2019 IEEE. DOI: 10.1109/RTEICT46194.2019.9016808.** (**Scopus Indexed**)
(Download link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9016808)
48. Ravish Aradhya H V, Mohd Leesan U A, **"Design of a Sequential Circuit Based on Multi-Threshold FinFET Technique,"** in the proceedings of IEEE – 4TH International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2019), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 17-18 May 2019. pp. 05-09**, ISBN: 978-1-7281-0630-4/19/$31.00 © 2019 IEEE.** (**Scopus Indexed**)
(Download link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9016975)
49. Ravish Aradhya H V, Ganesh Kumar M T, Madan H R, Sandeep Malik, **"Design and performance analysis of 8-bit Modified Wallace Tree Multiplier,"** in the proceedings of IEEE – 4TH International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2019), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 17-18 May 2019. pp. 666-670**, ISBN: 978-1-7281-0630-4/19/$31.00 © 2019 IEEE.** (**Scopus Indexed**)
(Download link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9016975)
50. Ravish Aradhya H V, Arun Arahunashi, Neetu S, **"Performance Analysis of Various SDN Controllers In Mininet Emulator,"** in the proceedings of IEEE – 4TH International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2019), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 17-18 May 2019. pp. 752-756**, ISBN: 978-1-7281-0630-4/19/$31.00 © 2019 IEEE.**
(**Scopus Indexed**)
(Download link: https: //ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9016693)
51. Ravish Aradhya H V, Mohd Leesan Ul Aktab, Furqan Saberi, **"Development of a Random Test Generator for Multi-Core Processor Design Verification,"** in the proceedings of IEEE – 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA-2019), PPG Institute of Technology, Coimbatore, India, 17-19 July

2019, pp. 1200-1204**, ISBN: 978-1-5386-2440-1/18/$31.00 © 2019 IEEE. DOI: 10.1109/ICECA.2019.8822103** (**Scopus indexed**)
(Download link: https://ieeexplore.ieee.org/document/8822103).

52. Ravish Aradhya H V, Mohana, **"Real Time Implementation of Emotion Detection and Classification System for Autism Patients,"** in Easy chair pre-prints series, Paper No. 2207, Dec-2019. (**Scopus Indexed**)
(Download link: https://easychair.org/publications/preprint/m54w)
53. Ravish Aradhya H V, Mohana, **"Performance Evaluation of Background Modeling Methods for Object and Tracking,"** 2020 Proceedings of the Fourth IEEE International Conference on Inventive Systems and Control (ICISC 2020), JCT Institutions, Coimbatore, TN, India, 8-10 Jan, 2020, pp: 413-419, **ISBN**: 978-1-7281-2812-2 (**Scopus indexed**).
(Download link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9171192)
54. Ravish Aradhya H V, Neethu S, "**Performance Analysis of Various SDN Controllers In Mininet Emulator,"** IEEE- 2019 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT-2019), MAY 17th & 18th 2019, pp. 752 -756, 978-1-7281-0630-4/19/$31.00 ©2019 IEEE, Bangalore, India – 562157. (**Scopus indexed**).
(Download link: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9016693)
55. Ravish Aradhya H. V, Ganesh Kumar M T, Madan H R, Sandeep Malik, **"Performance analysis of 8-bit Multiplier Architectures,"** in the proceedings of SPRINGER – International conference on Recent Trends in Science and Technology (ICRTST-2020), ATME College of Engineering, Mysuru – 570 028, 17-18 June 2020. **pp. 1139-1142, ISBN: 978-93-5396-830-4/18/$31.00 © 2020 IEEE. [**Springer nature' (**Scopus indexed**)
(Download link: https://ieeexplore.ieee.o92) https://icrtst.atme.in/assets/ICRTST-2020%20Proceeding.pdf
56. Ravish Aradhya H V, Manjunath K M, Muralidhara K N, **"N-bit Incrementer and Decrementer by a value 'M' Operation Circuit Design and Analysis for Various Parameters,"** International Web Conference on Smart Engineering Technologies- 2020. (IWCSET20), 26-27 June 2020, Ramco Institute of Technology, TN, **ISBN:** 978-93-5407-648-0 (**Scopus indexed**).
(Download link: https://ieeexplore.ieee.o92)
https://www.jcreview.com/issue.php?volume=Volume%207%20&issue=Issue-5&year=2020
57. Ravish Aradhya H V, Arunkumar P Chavan, **"A 2.5mW low-power dual VCO Quantizer for Σ-Δ modulator in 0.09µm technology,"** IEEE VLSI Device, Circuit and System

Conference (VLSIDCS-2020), 18-19 July, 2020, ED MSIT SBC, Kolkata, India. DOI:10.1109/ICAECC.2018.8479480 **(Scopus Indexed)**
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9179869)

58. Ravish Aradhya H. V, Shruthi Goudar, **"Development and Analysis of Parameters to Evaluate Design Partitioning of SOC,"** in the proceedings of IEEE – 2nd International Conference on Inventive Research in Computing Applications (ICIRCA-2020), RVS College of Engineering and Technology, Coimbatore– 641402, India, 15-17 July 2020. **pp. 1139-1142, ISBN: 978-1-7281-5374-2/18/$31.00 © 2020 IEEE. (Scopus indexed)**
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9182834)
59. Ravish Aradhya H. V, Basaveswari Biradar, Robert Chan (Qualcom, USA), **"A Novel Technique to Optimize Regressions in L2 Cache Verification,"** in the proceedings of IEEE – 2nd International Conference on Inventive Research in Computing Applications (ICIRCA-2020), RVS College of Engineering and Technology, Coimbatore– 641402, India, 15-17 July 2020. **pp. 1139-1142, ISBN:** 978-1-7281-5374-2/18/$31.00 © 2020 IEEE**. (Scopus indexed)**
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9183338)
60. Ravish Aradhya H V, Arunkumar P Chavan, **"Design and Synthesis of Low Power, High Speed 5th Order Digital Decimation Filter for Sigma- Delta Analog to Digital Converter,"** IEEE-International Conference on Communication and Signal Processing (ICCSP-2020), July 28-30, 2020, Meghnad Saha Institute of Technology, Kolkata, India. 978-1-7281-4987-5/20/$31.00©2020 IEEE, pp. 92-96. **DOI:** 10.1109/ICCSP48568.2020.9182295, **(Scopus Indexed)**
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9182295)
61. Ravish Aradhya H V, Arunkumar P Chavan, **"Design and Synthesis of Low Power, High Speed 5TH Order Digital Decimation Converter,"** in the proceedings of International conference on Communication and Signal Processing, (ICCSP-2020), July 28 - 30, 2020, Adhiparasakthi Engineering College, Melmaruvathur, Tamilnadu, India, Dec-2019. IEEE: 978-1-7281-4988-2/20/$31.00 ©2020 IEEE, pp. 92-96 **(Scopus Indexed)**
(Download link: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9182154)
62. Ravish Aradhya H V, Spoorthi G Gojanur, Juhie Fadnavis, **"Memory Design and Verification of SRAM-based Energy Efficient Ternary Content Addressable Memory,"** 11th IEEE-International Conference on Recent Engineering and Technology (ICRET-2021), CPET, Bengaluru, India, 20, June 2021. **(Scopus Indexed-IEEE)**. 2021 5th International Conference on Information Systems and Computer Networks (ISCON) GLA University, Mathura, India. Oct 22-23, 2021, 978-1-6654-0341-2/21/$31.00 ©2021 IEEE.

(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9702386)

63. Ravish Aradhya H V, Kevin Mathew, Vivek T M, **"A Review of Next Generation NVM Technologies,"** 11th IEEE-International Conference on Recent Engineering and Technology (ICRET-2021), CPET, Bengaluru, India, 20, June 2021. (**Scopus Indexed-IEEE**)
(Download Link: https://www.icret)
64. Ravish Aradhya H V, Kishan Maladkar, **"Design and Implementation of Automatic Gain Control Unit for Dual-Mode Bluetooth Modem,"** 6th International Conference on Communication and Electronics Systems (ICCES-2021), PPG Institute of Technology, Coimbatore, India, 8-10, July 2021. Paper ID: ICCES205, (**Scopus Indexed-IEEE**). **DOI: 10.1109/ICCES51350.2021.9488926**. Electronic ISBN: 978-1-6654-3587-1, Print on Demand (PoD) ISBN: 978-1-6654-1182-0.
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9488926)
65. Ravish Aradhya H. V., K. S. Kulkarni, **"Dataset development of GPU block using Scan Dump for Silicon Debug,"** 2021 6th International Conference on Communication and Electronics Systems (ICCES), [PPG Institute of Technology, Coimbatore, India, 8-10, July 2021. Paper ID: ICCES431], pp. 322-326, **doi: 10.1109/ICCES51350.2021.9489220. ISBN:978-1-6654-1182-0**
(Download Link: https://ieeexplore.ieee.org/document/9489220)
66. Ravish Aradhya H V, Arun Kumar Chavan, Rohan A V, Pranshu Orian, Preetham Kaka **"Design and Implementation of Automated Industrial Robots in Cylinder Liner Production Lines,"** IEEE- 2021 Asian Conference on Innovation in Technology (ASIANCON), PCCOER, Pune, India, 28 - 29 Aug 2021. (**WOS & Scopus Indexed-IEEE**)
(Download Link: https://ieeexplore.ieee.org/document/9545017)
67. Ravish Aradhya H V, M. R. Govinda, **"Comparison of Power Dissipation for CMOS and FinFET Dependent 6T SRAM at 18 nm Technology,"** 2021 International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT-2021), SVCE, Bengaluru, 27-28 Aug. 2021. (**Scopus Indexed**) pp. 975-979, **doi: 10.1109/RTEICT52294.2021.9573749**.
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9573749)
68. Ravish Aradhya H.V., Neethu S, **"Approaches to providing Quality of Service (QoS) in Software-Defined Networking,"** International Conference on Technologies for Smart Green Connected Society 2021 (ICTSGS-1-2021) conference led by Yamagata University Japan, Nov, 29-30, 2021.
(Download Link:)

69. Ravish Aradhya H. V. Gopal Kanase gplkanase@gmail.com Vinayakgouda Y G vinayakgouda1997@gmail.com, **"RTL to GDSII of Harvard Structure RISC Processor"** 2021 IEEE International Conference on Electronics, Computing and Communication Technologies (**CONECCT-2021**), 978-1-6654-2849-1/21/$31.00 ©2021 IEEE, **DOI: 10.1109/CONECCT52877.2021.9622735**.
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9622735)
70. Ravish Aradhya H V, Arunkumar P Chavan, **"A 7.7 GHz, 3.59mW Active Load Inverter Based VCO achieving -152.26dBc/Hz Phase Noise for VCO based Converter,"** 2nd International conference on Nanoelectronics, Machine Learning, Internet of things and computing systems NMIC-2022, 23-24th April 2022, Indian Society for VLSI Education, ISVE & ARTTC BSNL Ranchi (**Springer**)
(Download Link:)
71. Ravish Aradhya H.V, Aishwarya K M, **"Static Timing Analysis – Quality Analysis Methodology for Efficient Timing Analysis,"** 7th International Conference on Microelectronics, Computing, Communication Systems (MCCS-2022), ARTTC, BSNL near Jumar River Bridge, Hazaribag Road, Ranchi, 29-30 July, 2022.
(Download Link:)
72. Ravish Aradhya H.V, Archana M, **"Automation of Automotive Radar Software and System Qualification,"** 7th International Conference on Microelectronics, Computing, Communication Systems (MCCS-2022), ARTTC, BSNL near Jumar River Bridge, Hazaribag Road, Ranchi, 29-30 July, 2022.
(Download Link:)
73. Ravish Aradhya H V, Darshan Hegde, **"Implementation of Power Efficient Radix-4 Booth Multiplier with Pre-encoding,"** 7th International Conference on Computational Systems and Information Technology for Sustainable Solutions (CSITSS-2023), RVCE, Bangalore, India, IEEE, Nov2-4, 2023 pp. 1-5, DOI: 10.1109/CSITSS60515.2023.10334241 **(SCOPUS indexed)**
(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10334241)
74. Ravish Aradhya H V, Darshan Hegde, **"Microarchitecture Data Mining Debugs of CPU Core Simulation Challenges,"** 4th International Conference on Microelectronics, Communication Systems, Machine Learning & Internet of Things (MCMI-2023), 09 Nov-23, Indian Society for VLSI education (ISVE), Ranchi, India, Springer **(SCOPUS & SCI indexed)**
(Download Link:)

75. Ravish Aradhya H V, Manjunath R, **"Design and Verification of High Performance, Scalable Memory Controller for Server SOC,"** 4th International Conference on "Microelectronics, Communication Systems, Machine Learning & Internet of Things" (MCMI-2023), 09 Nov-23, Indian Society for VLSI education (ISVE), Ranchi, India, Springer **(SCOPUS & SCI indexed)**.
(Download Link:)
76. Ravish Aradhya H V, Manjunath R, **"A Review of High-Performance Memory Controller Designs in Solid State Drives",** 4th International Conference on Microelectronics, Communication Systems, Machine Learning & Internet of Things (MCMI-2023), 09 Nov-23, Indian Society for VLSI education (ISVE), Ranchi, India, Springer **(SCOPUS & SCI indexed)**.
(Download Link:)
77. Ravish Aradhya H V, Deepa Suranam Lamani, **"Power Performance Area optimization of Block-Level SoC Design,"** 4th International Conference on Microelectronics, Communication Systems, Machine Learning & Internet of Things (MCMI2023), 09 Nov 2023, Indian Society for VLSI education (ISVE), Ranchi, India, Springer **(SCOPUS & SCI indexed)**
(Download Link:)
78. Ravish Aradhya H V, Mohammed Zeeshan A, **"UPF Schematic Generation of Low Level Cache Controller Using Python",** 4th International Conference on Microelectronics, Communication Systems, Machine Learning & Internet of Things (MCMI-2023), 09 Nov 2023, Indian Society for VLSI education (ISVE), Ranchi, India, Springer **(SCOPUS & SCI indexed)**
(Download Link:)
79. Ravish Aradhya H V, Suma S, **"Design Methodology for Low Power Multi - Bit Flip Flop,"** 4th International Conference on Microelectronics, Communication Systems, Machine Learning & Internet of Things (MCMI-2023), 09 Nov-2023, Indian Society for VLSI education (ISVE), Ranchi, India, Springer **(SCOPUS & SCI indexed)**
(Download Link:)
80. Ravish Aradhya H V, Nethravathi K A, Rajath Duggal, Samarth Patil**,** Rahul Anand Benni, **"Square Shape Microstrip Patch Antenna-Array With Defected Ground Structure: Versatile Design for Emerging 5G Communication Technologies and Beyond"** IEEE, 9 International Conference for Convergence in Technology (I2CT), 5-6, April 2024, The Fern-Hotel, Lonavala, Maharashtra 410401 (**Scopus and WOS Indexed**). 2024 IEEE 9th

International Conference for Convergence in Technology (I2CT) | 979-8-3503-9447-4/24/$31.00 ©2024 IEEE, pp. 1-9, DOI: 10.1109/I2CT61223.2024.10543765
(Download Link: https://ieeexplore.ieee.org/document/10543765)

81. Ravish Aradhya H V, Arunkumar P C, Shrish Shrinath Vaidya, Sanket M Mantrashetti, Abhishek G Dastikopp, Kishan S Murthy, Prakash Pawar (IIIT, Dharwad, India), **"Integrating Neural Network Models for Advanced Automation in Analog Amplifier Circuit Design",** 2024 IEEE International Conference on Electronics, Computing and Communication Technologies (**CONECCT-2024**), Indian Institute of Science, 12-14 July 2024, Circuits, Devices & VLSI pp. 1-6, doi: 10.1109/CONECCT62155.2024.10677072.
(Download Link: https://ieeexplore.ieee.org/document/10677072)
82. Ravish Aradhya H V, Navya Singh, Harshil Kundety, Mohana, **"Performance Analysis of Cloud-Based Applications with CloudAnalyst"** 5th IEEE_International Conference on Electronics and Sustainable Communication Systems (ICESC 2024), Hindusthan Institute of Technology, Coimbatore, TN, ISBN: 979-8-3503-7994-5, 7-9 Aug 2024.
(Download Link: https://ieeexplore.ieee.org/document/10690112)
83. H V Ravish Aradhya, Skanda V Jois, **"Robust and Efficient Implementation of Design for Testability for Integrated Circuits,"** 8th IEEE_International Conference on Computational Systems and Information Technology for Sustainable Solutions (CSITSS-2024), RVCE, Bangalore, Karnataka,3-4, Nov 2024, ISBN: 979-8-3503-7994-5.
(Download Link:)
84. H V Ravish Aradhya, Roriech P A, **"Advanced ESD Protection Mechanism for a CMOS Low Noise Amplifier,"** 8th IEEE_ International Conference on Computational Systems and Information Technology for Sustainable Solutions (CSITSS-2024), RVCE, Bangalore, Karnataka,3-4, Nov 2024, ISBN: 979-8-3503-7994-5.
(Download Link:)
85. H V Ravish Aradhya, Roriech P A, Skanda V Jois, **"Design & Analysis of a Three-Stage Latched Comparator,"** 8th IEEE_International Conference on Computational Systems and Information Technology for Sustainable Solutions (CSITSS-2024), RVCE, Bangalore, Karnataka,3-4, Nov 2024, ISBN: 979-8-3503-7994-5.
(Download Link:)

(iii) National Journals: NIL

(iv) National Conferences: 24

1. H. V. Ravish Aradhya, V. Swetha, Dr. K. N. Muralidhara, **"Practical aspects of FEV using Cadence LEC,"** in the proceedings of National level technical paper meet (NLTPM-08), Sambhram Institute of technology, Bangalore-97 during 04-05 Apr-2008.

2. H. V. Ravish Aradhya, U. Jeevan Kumar, Dr. K. N. Muralidhara, **"CAD tool for computing iteration bound of DSP chips,"** in the proceedings of National conference on Information Technology (NCIT-09) Bangalore Institute of technology, Bangalore-01, INDIA, March 2009.

3. H. V. Ravish Aradhya, S. Sunitha, Dr. K. N. Muralidhara, **"Square FIFO for data transfer between unrelated clock domains,"** in the proceedings of National conference on recent trends in soft computing (NCRTSC-09), New Horizon CE, Bangalore-87 during 24-25 Apr-2009.

4. H. V. Ravish Aradhya, G. Sunil Kumar Reddy, Dr. K. N. Muralidhara, **"ASIC Implementation of Systolic Array Architecture for Full Search Block Matching Algorithm,"** in the proceedings of National conference on Recent Trends in Communication, Electronics and Information Technology(NCRTCEIT-09), CMRIT, Bangalore-37 during 14-15 May-2009.

5. H. V. Ravish Aradhya, S. Sunitha, Dr. K. N. Muralidhara, **"Practical Aspects of Boundary Scan and applications beyond interconnect test,"** in the proceedings of National conference on recent trends in communication, electronics and information technology (NCRTCEIT-09), CMRIT, Bangalore-37 during 14-15 May-2009.

6. H V Ravish Aradhya, G. Sunil Kumar Reddy, Dr. K. N. Muralidhara, **"Design and Implementation of an optimized systolic array architecture for FSBMA for real time applications,"** in the proceedings of National conference on recent trends in communication, electronics and information technology (NCRTCEIT-09), CMRIT, Bangalore-37 during 14-15 May-2009.

7. H. V. Ravish Aradhya, U. Jeevan Kumar, Dr. K. N. Muralidhara, **"Estimation of Iteration Bound For DSP Algorithms Using LPM Method,"** in the proceedings of National conference on VLSI and Multimedia communication (NCVM-09), RVCE, Bangalore-59 during 23-24 Oct-2009.

8. H. V. Ravish Aradhya, K. Mahesh, Dr. K. N. Muralidhara, **"Design and implementation of an advanced external interrupt controller unit [AEICU] on cortex-r4 processor,"** in the proceedings of National Level Conference on Computers, Communication and Controls (N4C-11), R. V. College of Engineering, Bangalore, during 29-30 Apr-2010.

9. H. V. Ravish Aradhya, C. Rohith Kumar, Dr. K. N. Muralidhara, **"Design and implementation of Wireless fire surveillance system,"** in the proceedings of National Level Conference on Computers, Communication and Controls (N4C-11), R. V. College of Engineering, Bangalore, during 29-30 Apr-2010.

10. H. V. Ravish Aradhya, V. Sandeep, Dr. K. N. Muralidhara, **"SPI Interface and Physical Layer of Low Energy Bluetooth,"** in the proceedings of National Level Conference on Computers, Communication and Controls (N4C-11), R. V. College of Engineering, Bangalore, during 29-30 Apr-2010.

11. H. V. Ravish Aradhya, V. Sandeep, Dr. K. N. Muralidhara, **"Low Energy Bluetooth: An Evolution in Short Range Wireless Communication,"** in the proceedings of National Level Technical Symposium TECHNISIUM'11, Siddaganga Institute of Technology (SIT), Tumkur, during 09-10 Apr-2011.

12. H. V. Ravish Aradhya, H. R. Madan, Dr. K. N. Muralidhara, **"CMOS Realization of Reversible BCD Adder,"** in the proceedings of National conference on Recent Trends in Communication Technology, Vol. no. 01, pp. 227 – 233, during 13.01.2012.

13. H. V. Ravish Aradhya, H. R. Madan, Dr. K. N. Muralidhara, **"CMOS implementation of reversible comparators,"** in the proceedings of National conference on Recent Trends in Communication Technology, Vol. no. 01, pp. 227 – 233, during 13.01.2012.

14. H. V. Ravish Aradhya, H. R. Madan, Dr. K. N. Muralidhara, "**Design and Performance Analysis of 6T-SRAM for Different Scaled Technologies,"** in the proceedings of National conference on Recent Trends in Communication Technology, Vol. no. 01, pp. 227 – 233, during 13.01.2012.

15. H. V. Ravish Aradhya, H. R. Madan, Dr. K. N. Muralidhara, **"Comparative Study of logic circuits based on MOSFET and FinFET under 32 nm process technology,"** in the proceedings of National conference on Recent Trends in Communication Technology, Vol. no. 01, pp. 227 – 233, during 13.01.2012.

16. H. V. Ravish Aradhya, H. R. Madan, Dr. K. N. Muralidhara, **"Comparative Study of DRAM for various CMOS process technology,"** in the proceedings of National conference on Recent Trends in Communication Technology, Vol. no. 01, pp. 227 – 233, during 13.01.2012.

17. H. V. Ravish Aradhya, R. Chinmaye, Dr. K. N. Muralidhara, **"Design and Optimization of Reversible Logic Decoder For Low Power Applications,"** National conference on advanced VLSI and embedded technology (NCAVET-2012), New Delhi, during 28-29, Feb-2012.

18. Dr. H V Ravish Aradhya, et al, **"Design and Performance Comparison of finFET, CNFET and GNRFET based 6T SRAM,"** in the proceedings of National Conference on Knowledge, Innovation in Technology and Engineering (NCKITE), Kruti Institute of Technology and Engineering, Raipur, 10-11 Apr-2015, pp. 24-28.

19. Dr. H V Ravish Aradhya, et al, **"Design and Performance Analysis of Low-Power Hybrid CMOS Full Adder Cells,"** in the proceedings of National Conference on "ICT-Innovations for sustainability," R. V. College of Engineering, Bengaluru, 16-17 May-2015.
20. Ravish Aradhya H. V and Karnati Gopi Manohar, **"Realization of universal gates of Multiple Valued Logic (MVL) using CMOS technology,"** National conference on "Engineering, Technology and Management, 22-23 April 2016, R. V. College of Engineering, Bengaluru 560059.

21. Ravish Aradhya H. V and Smitha G. S, **"De-skew model for High speed Source synchronous SerDes PHY,"** National conference on "Engineering, Technology and Management, 22-23 April 2016, R. V. College of Engineering, Bengaluru 560059

22. Ravish Aradhya H. V and Pooja K S, **"Verification of Peripheral Interconnect IP using SystemVerilog and UVM,"** National conference on "Engineering, Technology and Management, 22-23 April 2018, R. V. College of Engineering, Bengaluru 560059

23. Ravish Aradhya H. V and Akshatha P. Inamdar, "Verification of Peripheral Interconnect IP using SystemVerilog and UVM," National conference on "Engineering, Technology and Management, 22-23 April 2018, R. V. College of Engineering, Bengaluru 560059

24. Ravish Aradhya H V, Arunkumar P Chavan, **"Design and analysis of component for VCO enabled quantizer using Different stages of ring oscillator in CT sigma delta ADC,"** National conference on knowledge dissertation of PG projects and research's work May 7th and 8th 2018, RVCE, Bengaluru.

PhD Forum – Presentations:

1. Mohana, Ravish Aradhya H. V, **"Elegant and Efficient Algorithms for Real Time Implementation of Object Detection, Classification, Tracking and Counting using FPGA Zynq XC7Z020 for Automated Video Surveillance Applications,"** 10th IEEE Advanced Networks and Telecommunications Systems (ANTS-2016), 6-9 November 2016, J. N. Tata Auditorium, ***Indian Institute of Science*** (IISc), Bangalore, India.
2. Mohana, Ravish Aradhya H. V, **"Design and Implementation of Object Detection, Classification, Tracking, Counting and Classification Algorithms using Artificial Intelligence for Automated Video Surveillance Applications,"** 24th International Conference on Advanced Computing Communications (ADCOM-2018), 21st – 23rd September 2018, at the IIIT-Bangalore, India.
3. Mohana, Ravish Aradhya H. V, **"Design of Efficient Algorithms for Video Surveillance Applications using Artificial Intelligence,"** 25th IEEE Advanced Computing and Communications Conference (ADCOM 2019), 5-7 September 2019, at International Institute of Information Technology (IIIT-B), Bangalore, India.

Awards and Appreciations:

1. Recipient of "**Best Research Paper Award**" from ***International Academy of Science***, Engineering and Technology in International Journal of Electronics and Communication Engineering (IJECE), ISSN: 2278-991X, Dec-2014. IF-3.329, for the paper titled "**Design and Optimization of Reversible carry look ahead Adder Circuit**." (PhD research outcome).

2. Recipient of "**Best Research Paper Award**" from ***IEEE-International Conference on Engineering and Technology*** (ICETECH-2015), Mar-2015. IF-3.329, for the paper titled "**Design of square spiral Nano-antenna in infra-red region for Solar Energy Harvesting**," conducted by Rathinam Institute of Technology, Coimbatore, Tamilnadu, India. IEEE Explorer: 978-1-4799-7678-2/15/$31.00, **©2015 IEEE,** (Conference Record Number: #35961), 20th March 2015, pp:1026-1031.

3. Recipient of "**Best Research Paper Award**" from ***IEEE-International Conference on 'Innovative Mechanisms for Industry Applications'*** (ICIMIA-2017), 21-23 Feb 2017, for the paper titled "**Implementation of Highly Efficient Sorting Algorithm for Median Filtering using FPGA Spartan-6**," conducted by Dayananda Sagar College of Engineering, Bengaluru, India. 978-1-5090-5960-7/17/$-31.00, **©2017 IEEE**, ISBN: 978-1-5090-5959-1**,** (Conference Record Number: #35961), 21-23 Feb 2017, pp. 265-269.

Best Teacher Awards:

1. Recipient of "Best Teacher Award" from Carrier Launcher (India), Bangalore, May 2006

2. Recipient of "Best Teacher Award" from ISTE-RVCE Chapter, Sep-2019