



**RV COLLEGE OF ENGINEERING®**  
(Autonomous Institution Affiliated to VTU, Belagavi)  
R.V. Vidyaniketan Post, Mysore Road  
Bengaluru – 560 059



**Bachelor of Engineering (B.E.)**  
**Scheme and Syllabus of V & VI Semesters**

**2018 SCHEME**

**ELECTRONICS & COMMUNICATION**  
**ENGINEERING**

# RV COLLEGE OF ENGINEERING®

(Autonomous Institution Affiliated to VTU, Belagavi)

## ELECTRONICS AND COMMUNICATION ENGINEERING

<b>FIFTH SEMESTER CREDIT SCHEME</b>							
Sl. No.	Course Code	Course Title	BOS	Credit Allocation			Total Credits
				L	T	P	
1.	18HSI51	Intellectual Property Rights & Entrepreneurship	HSS	3	0	0	3
2.	18EC52	Embedded System Design	EC	3	0	0	3
3.	18EC53	Communication Systems – 1 (Theory & Practice)	EC	3	0	1	4
4.	18EC54	Digital VLSI Design (Theory & Practice)	EC	3	0	1	4
5.	18EC55	Digital Signal Processing and Machine Learning	EC	3	1	0	4
6.	18EC5AX	Elective A (PE)	EC	3	0	0	3
7.	18EC5BXX	Elective B (GE)*	EC	3	0	0	3
<b>Total Number of Credits</b>				<b>21</b>	<b>1</b>	<b>2</b>	<b>24</b>
<b>Total number of Hours/Week</b>				<b>21</b>	<b>1</b>	<b>5</b>	

<b>SIXTH SEMESTER CREDIT SCHEME</b>							
Sl. No	Course Code	Course Title	BOS	Credit Allocation			Total Credits
				L	T	P	
1.	18HEM61	Introduction to Management and Economics	HSS	3	0	0	3
2.	18EC62	Computer Networks and Protocols (Theory & Practice)	EC	3	0	1	4
3.	18EC63	Communication Systems – 2 (Theory & Practice)	EC	3	1	1	5
4.	18EC64	Minor Project**	EC	0	0	2	2
5.	18EC6CX	Elective C (PE)	EC	3	0	0	3
6.	18EC6DX	Elective D (PE)	EC	3	0	0	3
7.	18G6EXX	Elective E (GE)*	EC	3	0	0	3
8.	18HSE68	Professional Practice – II (Employability Skills and Professional Development of Engineers)	HSS	0	0	1	1
<b>Total Number of Credits</b>				<b>18</b>	<b>1</b>	<b>5</b>	<b>24</b>
<b>Total number of Hours/Week</b>				<b>18</b>	<b>1</b>	<b>7+1</b>	

**V Semester****GROUP A: PROFESSIONAL ELECTIVES (MOOC COURSES)**

<b>Sl. No.</b>	<b>Course Code</b>	<b>Course Title</b>
1.	18EC5A1	Programming in JAVA
2.	18EC5A2	Probability Foundations for Electrical Engineers
3.	18EC5A3	OP-AMP Practical Application: Design Simulation and Implementation
4.	18EC5A4	Fiber Optic Communication Technology
5.	18OC5A5	The Joy of Computing Using Python

**V Semester****GROUP B: GLOBAL ELECTIVES**

<b>Sl. No.</b>	<b>Course Code</b>	<b>Course Title</b>
1.	18G5B05	Automotive Electronics

**VI Semester****GROUP C: PROFESSIONAL ELECTIVES**

<b>Sl. No.</b>	<b>Course Code</b>	<b>Course Title</b>
1.	18CS6C1	Internet of Things and Edge Computing
2.	18EC6C2	Real Time Systems
3.	18EC6C3	Low power VLSI Design
4.	18EC6C4	Database Management Systems (DBMS)
5.	18EC6C5	Control Engineering
6.	18EC6C6	Cryptography and Network Security

**VI Semester****GROUP D: PROFESSIONAL ELECTIVES**

<b>Sl. No.</b>	<b>Course Code</b>	<b>Course Title</b>
1.	18EC6D1	Digital Signal Processing using ARM Cortex M Devices
2.	18EC6D2	Computer Vision
3.	18EC6D3	Data Structures and Algorithms (Common EC & TE)
4.	18EC6D4	Radio Frequency & Millimetre Wave IC Design
5.	18EC6D5	Deep Learning
6.	18EC6D6	Algorithms for VLSI Design and Automation

**VI Semester****GROUP E: GLOBAL ELECTIVES**

1.	18G6E05	Wearable Electronics
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## V Semester

INTELLECTUAL PROPERTY RIGHTS AND ENTREPRENEURSHIP  
(Theory)

<b>Course Code</b>	:	<b>18HSI51</b>	<b>CIE</b>	:	<b>100</b>
<b>Credits: L:T:P</b>	:	<b>3:0:0</b>	<b>SEE</b>	:	<b>100</b>
<b>Total Hours</b>	:	<b>36L</b>	<b>SEE Duration</b>	:	<b>03Hrs</b>
<b>Course Learning Objectives:</b> The students will be able to					
1	To build awareness on the various forms of IPR and to build the perspectives on the concepts and to develop the linkages in technology innovation and IPR.				
2	To encourage innovation, invention and investment and disclosure of new Technology and to recognize and reward innovativeness				
3	To motivate towards entrepreneurial careers and build strong foundations skills to enable starting, building and growing a viable as well as sustainable venture.				
4	Develop an entrepreneurial outlook and mind set along with critical skills and knowledge to manage risks associated with entrepreneurs.				

## Unit-I

07 Hrs

**Introduction:** Types of Intellectual Property, WIPO**Patents:** Introduction, Scope and salient features of patent; patentable and non-patentable inventions, Patent Procedure - Overview, Transfer of Patent Rights; Biotechnology patents, protection of traditional knowledge, Infringement of patents and remedy, Case studies**Trade Secrets:** Definition, Significance, Tools to protect Trade secrets in India.

## Unit – II

04 Hrs

**Trade Marks:** Concept, function and different kinds and forms of Trade marks, Registrable and non- registrable marks. Registration of trade mark; Deceptive similarity; Transfer of Trade Mark, ECO Label, Passing off. Infringement of trade mark with Case studies and Remedies.

## Unit –III

09 Hrs

**Industrial Design:** Introduction of Industrial Designs, Features of Industrial Design. Procedure for obtaining Design Protection, Revocation, Infringement and Remedies, Case studies**Copy Right:** Introduction, Nature and scope, Rights conferred by copy right, Copy right protection, transfer of copy rights, right of broad casting organizations and performer's rights, Exceptions of Copy Right, Infringement of Copy Right with case studies**Intellectual property and cyberspace:** Emergence of cyber-crime; Meaning and different types of cybercrime. Overview of Information Technology Act 2000 and IT Amendment Act 2008

## Unit –IV

08 Hrs

**Introduction to Entrepreneurship** – Learn how entrepreneurship has changed the world. Identify six entrepreneurial myths and uncover the true facts. Explore E-cells on Campus**Listen to Some Success Stories:** - Global legends Understand how ordinary people become successful global entrepreneurs, their journeys, their challenges, and their success stories. Understand how ordinary people from their own countries have become successful entrepreneurs.**Characteristics of a Successful Entrepreneur** Understand the entrepreneurial journey and learn the concept of different entrepreneurial styles. Identify your own entrepreneurship style based on your personality traits, strengths, and weaknesses. Learn about the 5M Model, each of the five entrepreneurial styles in the model, and how they differ from each other. **Communicate Effectively:** Learn how incorrect assumptions and limiting our opinions about people can negatively impact our communication. Identify the barriers which cause communication breakdown, such as miscommunication and poor listening, and learn how to overcome them.**Communication Best Practices.** Understand the importance of listening in communication and learn to listen actively. Learn a few body languages cues such as eye contact and handshakes to strengthen communication. (Practical Application)

## Unit –V

08 Hrs

**Design Thinking for Customer Delight:** - Understand Design Thinking as a problem-solving process. Describe the principles of Design Thinking. Describe the Design Thinking process.**Sales Skills to Become an Effective Entrepreneur:** - Understand what is customer focus and how all selling effort should be customer-centric. Use the skills/techniques of personal selling, Show and Tell, and Elevator Pitch to sell effectively.**Managing Risks and Learning from Failures:** - Identify risk-taking and resilience traits. Understand that risk-taking

is a positive trait. Learn to cultivate risk-taking traits. (Practical Application) Appreciate the role of failure on the road to success, and understand when to give up. Learn about some entrepreneurs/risk-takers. (Practical Application).

**Are You Ready to be an Entrepreneur:** - Let's ask "WHY" Give participants a real picture of the benefits and challenges of being an entrepreneur. Identify the reasons why people want to become entrepreneurs. Help participants identify why they would want to become entrepreneurs.

**Course Outcomes: After completing the course, the students will be able to**

<b>CO1:</b>	Comprehend the applicable source, scope and limitations of Intellectual Property within the purview of engineering domain.
<b>CO2:</b>	Knowledge and competence related exposure to the various Legal issues pertaining to Intellectual Property Rights with the utility in engineering perspectives.
<b>CO3:</b>	Enable the students to have a direct experience of venture creation through a facilitated learning environment.
<b>CO4:</b>	It allows students to learn and apply the latest methodology, frameworks and tools that entrepreneurs use to succeed in real life.

**Reference Books**

<b>1.</b>	Law Relating to Intellectual Property, Wadehra B L, 5 <sup>th</sup> Edition, 2012, Universal Law Pub Co. Ltd.-Delhi, ISBN: 9789350350300
<b>2.</b>	Intellectual Property Rights: Unleashing Knowledge Economy, Prabuddha Ganguly, 1 <sup>st</sup> Edition, 2001, Tata McGraw Hill Publishing Company Ltd., New Delhi, ISBN: 0074638602.
<b>3.</b>	Intellectual Property and the Internet, Rodney Ryder, 2002, Lexis Nexis U.K., ISBN: 8180380025, 9788180380020.
<b>4.</b>	Entrepreneurship, Rajeev Roy, 1 <sup>st</sup> Edition, 2012, Oxford University Press, New Delhi, ISBN: 9780198072638.

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**CO-PO Mapping**

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
<b>CO1</b>	<b>1</b>	-	-	-	<b>3</b>	<b>3</b>	-	<b>3</b>	<b>1</b>	<b>2</b>	-	<b>3</b>
<b>CO2</b>	<b>1</b>				<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>1</b>	<b>2</b>	-	<b>3</b>
<b>CO3</b>	-	<b>3</b>	<b>2</b>	-	-	<b>2</b>	<b>2</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>
<b>CO4</b>	-	<b>3</b>	<b>2</b>	-	-	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>

**High-3 : Medium-2 : Low-1**

<b>Semester: V</b>						
<b>EMBEDDED SYSTEM DESIGN</b>						
<b>(Theory)</b>						
<b>Course Code</b>	:	18EC52		<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:0:0		<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L		<b>SEE Duration</b>	:	03 Hours
<b>Course Learning Objectives:</b> The students will be able to						
<b>1</b>	Understand embedded computing system, design process and basic building blocks of an embedded system.					
<b>2</b>	Illustrate how microprocessor, memory, peripheral components and buses build an embedded platform and their interaction.					
<b>3</b>	Evaluate how architectural and implementation design decisions influence performance and power dissipation.					
<b>4</b>	Explain the basic operation of a real-time operating system.					
<b>5</b>	Develop application code using APIs of RTX ARM to demonstrate the kernel services.					

<b>Unit-I</b>		<b>07 Hrs</b>
<b>Introduction to Embedded System Design:</b> Introduction, Characteristics of Embedding Computing Applications, Concept of Real time Systems, Challenges in Embedded System Design, Design Process: Requirements, Specifications, Hardware Software Partitioning, Architecture Design. <b>Embedded System Architecture:</b> Co-Processor & Hardware Accelerators, Processor performance Enhancement: Pipelining, Superscalar Execution, Multi Core CPUs.		
<b>Unit – II</b>		<b>0 8Hrs</b>
<b>Designing Embedded System Hardware –I:</b> Memory systems: Memory organization, Error detecting and correcting, memory Access times, DRAM interfaces, DRAM refresh techniques, Cache, Unified versus Harvard caches, Cache Organization, Direct mapped and Set associative caches, Cache coherency, Dual port memory		
<b>Unit –III</b>		<b>07 Hrs</b>
<b>Designing Embedded System Hardware –II:</b> I/O Devices: Watchdog Timers, Interrupt Controllers, Interfacing Protocols: SPI, I2C, CAN: Frame Formats, Wiring Topology, Reset Circuits, Interfacing RTC.		
<b>Unit –IV</b>		<b>07 Hrs</b>
<b>Designing Embedded System Software</b> Application Software, System Software, Use of High Level Languages: C, C++, Java, Programming & Integrated Development Environment tools, Debugger, Board Support Library, Chip Support Library Analysis and Optimization: Execution Time, Energy & Power, Program Size; Floating point data representation, Embedded System Coding Standards: MISRA C 2012.		
<b>Unit –V</b>		<b>07 Hrs</b>
<b>Designing Embedded System Software –II:</b> OS based Design, Real Time Kernel, Process& Thread, Inter Process Communications, Synchronization, Kernel services, Case Study: RTX-ARM.		

<b>Course Outcomes: After completing the course, the students will be able to</b>	
<b>CO1:</b>	Analyse the architecture of embedded system, functional difference between general purpose system, operational & non-operational attributes of embedded system.
<b>CO2:</b>	Analyze the hardware requirements of an embedded system & design according to specifications.
<b>CO3:</b>	Develop software architecture & realize optimally using suitable language.
<b>CO4:</b>	Engage in self-study to formulate, design, implement, analyze and demonstrate an embedded application developed to control real world operations.

<b>Reference Books</b>	
<b>1.</b>	Introduction to Embedded Systems, Shibu K V, 2009, Tata McGraw Hill Education Private Limited, ISBN: 10: 0070678790
<b>2.</b>	Embedded System Design, Steve Heath, 2004, Elsevier, 2 <sup>nd</sup> Edition, ISBN 9780750655460
<b>3.</b>	Embedded Systems – A contemporary Design Tool, James K Peckol, 2008, John Wiley, ISBN: 0-444-51616-6
<b>4.</b>	Real-Time Concepts for Embedded Systems, Qing Li and Carolyn Yao, 2003, CMP Books, ISBN:1578201241.
<b>5.</b>	Reference Manuals: I2C,SPI, Cache Design, MISRA C 2012, RTX-ARM

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**CO-PO Mapping**

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	3	2	-	-	-	-	-	1	-	1
CO2	3	2	2	1	2	2	-	-	-	1	-	1
CO3	3	3	2	2	2	2	2	2	-	1	-	1
CO4	3	3	3	3	2	3	2	3	3	3	3	3

**High-3: Medium-2 : Low-1**

<b>Semester: V</b>						
<b>COMMUNICATION SYSTEMS I</b>						
<b>(Theory &amp; Practice)</b>						
<b>Course Code</b>	:	18EC53		<b>CIE</b>	:	100+50 Marks
<b>Credits: L:T:P</b>	:	3:0:1		<b>SEE</b>	:	100+50 Marks
<b>Total Hours</b>	:	36L+33P		<b>SEE Duration</b>	:	03+03 Hours

<b>Course Learning Objectives:</b> The students will be able to	
<b>1</b>	Understand the concepts of FM, Low pass and bandpass sampling and Random processes to compute performance parameters.
<b>2</b>	Analyse the concepts of sampling, quantization, encoding and apply them to voice conditioning for communication purposes.
<b>3</b>	Understand the concepts of information theory as a prerequisite for error detection and correction.
<b>4</b>	Associate the concepts of Information Theory to the principle of block error coding and decoding for different communication scenario.

<b>UNIT-I</b>	<b>07 Hrs</b>
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**Angle (Exponential) Modulation** Nonlinear Modulations, Bandwidth of Angle-Modulated Waves, Generating of FM Waves by direct methods, Demodulation of FM, PLL.  
**Random Variables and Random Processes**  
 Random variables and their properties, Multiple Random Variables: Properties, Operations. **Random Processes:**  
 From Random Variable to Random Process, Classification of Random Processes, properties and operations

<b>UNIT-II</b>	<b>07 Hrs</b>
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**Baseband Pulse Transmission (Line Codes) (RZ and NRZ)** Unipolar, Polar, Bipolar, Manchester signaling, Discrete form statement of Wiener – Khinchine Theorem – Applications to PSD derivations for these pulses. Highlights of other baseband pulses HDB3, B6ZS.  
**Digital Multiplexing and demultiplexing:** Framing with overheads, Types- Synchronous, Asynchronous, Quasi-Synchronous. Demultiplexing FSM, Retiming FSM with Plesiochronous buffering.

<b>UNIT-III</b>	<b>08 Hrs</b>
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**Sampling and Analog to Digital Conversion** Low Pass Sampling Theorem (Impulse, Pulse and Flat top).  
**Pulse-Code Modulation (PCM)** – Uniform Quantization, Non uniform Quantization – Optimal quantizer and Robust quantizer ( $\mu$ -law and A-law), SNR derivations for all types. Differential Pulse Code Modulation (DPCM), Delta Modulation with SNR derivation, Adaptive DM with SNR statement only.  
 Sigma-delta Modulation concept. Applications to Channel Vocoders and LPC Vocoders.(Conceptual treatment)

<b>UNIT-IV</b>	<b>07 Hrs</b>
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**Introduction to Information Theory** Measure of Information, Source Encoding, Error-Free Communication over a Noisy Channel, Channel Capacity of a Discrete Memory less Channel, Channel Capacity of a Continuous memory less Channel, Practical Communication Systems in Light of Shannon's Equation.

<b>UNIT-V</b>	<b>07 Hrs</b>
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**Error Correcting Codes**  
 Redundancy for error correction, Linear Block Codes, Cyclic Codes, The effect of error correction, Burst-Error Detecting and Correcting Codes. A brief concept of RS Codes + Interleaving

- Practical's: Communication Lab**
1. Frequency Modulation and Demodulation (Matlab)
  2. Verification of Sampling theorem
  3. Implementation of Convolution and DFT
  4. Realization of FIR filter to meet given specifications (DSP kit)
  5. Realization of IIR filter to meet given specifications (DSP kit)
  6. Generation of Noise and study of its properties
  7. Time Division Multiplexing ( Matlab & Circuit)
  8. Pulse Code Modulation & Delta Modulation (Matlab & Simulink)
  9. Linear block code and Huffman code (Matlab)
  10. Line codes generation and Pe & PSD Calculation



<b>Course Outcomes: After completing the course, the students will be able to</b>	
CO1:	Associate and apply the concepts of digital formatting, reconstruction to digital transmitter and receivers used in cellular and other communication devices.
CO2:	Analyze and compute performance of continuous wave modulation, digital formatting schemes.
CO3:	Test and validate digital formatting schemes and block codes under noisy channel conditions to estimate the performance in practical communication systems.
CO4:	Design/Demonstrate by way of simulation or emulation of different functional blocks of digital formatting and block error correction

<b>Reference Books</b>	
1.	Modern Digital and Analog communication Systems, B.P.Lathi and Zhi Ding, 4 <sup>th</sup> Edition, 2010, Oxford University Press, ISBN: 9780198073802.
2.	Analog & Digital Communication Systems, Simon Haykin, 1 <sup>st</sup> Edition, 2014, John Wiley & sons, ISBN 978-0-471-64735-5.
3.	Communication Systems, Simon Haykin , 4 <sup>th</sup> Edition, 2004, John Wiley, India Pvt. Ltd, ISBN 0471178691.

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20.

**Total CIE is 30(Q) +50(T) +20(EL) =100 Marks**

**Scheme of Continuous Internal Evaluation (CIE); Practical Test for 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average marks (AM) over number of weeks is considered for 30 marks. At the end of the semester a test (T) is conducted for 10 marks. The students are encouraged to implement additional innovative experiments (IE) in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

**Total CIE is 30(AM) +10 (T) +10 (IE) =50 Marks.**

**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part A and Part B. Part A consists of objective type questions for 20 marks covering the complete syllabus. Part B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

**Scheme of Semester End Examination (SEE); Practical Exam for 50 Marks**

SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

**Semester End Evaluation (SEE): Theory (100 Marks) + Practical (50 Marks) = Total 150 Marks**

<b>CO-PO Mapping</b>												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	2	-	-	-	1	1	-	2
CO2	3	2	2	1	-	-	-	-	1	1	-	1
CO3	3	3	2	2	2	-	-	-	-	1	-	1
CO4	3	3	3	3	2	-	-	-	-	1	-	2

**Low-1 Medium-2 High-3**

<b>Semester: V</b>						
<b>DIGITAL VLSI DESIGN</b>						
<b>(Theory &amp; Practice)</b>						
<b>Course Code</b>	:	18EC54		<b>CIE</b>	:	100+50 Marks
<b>Credits: L:T:P</b>	:	3:0:1		<b>SEE</b>	:	100+50 Marks
<b>Total Hours</b>	:	36L + 33P		<b>SEE Duration</b>	:	03+03 Hours
<b>Course Learning Objectives:</b> The students will be able to						
<b>1</b>	Analyze the impact of fabrication technologies: Methods for optimizing the area, speed, and power of circuit layouts.					
<b>2</b>	Design and implement combinational circuit.					
<b>3</b>	Design and implement sequential system by considering specifications.					
<b>4</b>	Analyze the impact of RC effect in post simulation.					

<b>Unit-I</b>	<b>8 Hrs</b>
<b>VLSI Design Flow:</b> Specification, Design entry, Functional simulation, planning placement and routing, timing simulation. <b>MOS Transistor:</b> Introduction, Ideal I-V characteristics, C-V Characteristics, Simple MOS Capacitance Models, Detailed MOS Gate Capacitance Model, Non-ideal I-V Effects, Mobility Degradation and Velocity Saturation, Channel Length Modulation, Threshold Voltage Effects, Junction Leakage, Body effect, Tunneling. <b>DC Transfer Characteristics:</b> Static CMOS Inverter DC Characteristics, Beta Ratio Effect, Noise Margin. <b>Combinational Circuit Design:</b> CMOS Logic, Inverter, NAND Gate, NOR Gate, Combinational Logic, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers.	
<b>Unit – II</b>	<b>9 Hrs</b>
<b>Delay:</b> Transient response, RC delay model, linear delay model <b>Circuit Families:</b> Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Complementary Pass-Transistor Logic Circuits.: <b>Datapath Subsystem:</b> Single-Bit Addition, Ripple Carry Adder, Manchester Carry chain adder, Carry Skip adder, Carry Select Adder, Braun, Baugh-wooley and Array multipliers.	
<b>Unit –III</b>	<b>6 Hrs</b>
<b>Sequential MOS Logic Circuitry:</b> Behavioral of Bistable element, SR Latch Circuitry, Clocked latch and Flip Flop Circuitry, C-MOS D-Latch and Edge Triggered Flip-Flop. <b>Sequencing Static Circuits:</b> Sequencing Methods, Max-Delay Constraints, Min-Delay Constraints Time Borrowing, Clock Skew	
<b>Unit –IV</b>	<b>6 Hrs</b>
<b>Array Sub system SRAM:</b> Memory cell Read/Write operation, Decoder, Bit-line conditioning and column circuitry and Column Circuitry, Multi-Ported SRAM. <b>DRAM Subarray Architectures, Column Circuitry Read-Only Memory Programmable ROMs, NAND ROMs. Content-Addressable Memory, PLA</b>	
<b>Unit –V</b>	<b>7 Hrs</b>
<b>CMOS Processing Technology:</b> CMOS Technologies, Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO <sub>2</sub> ), Isolation, Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, Metrology. <b>Layout Design Rules-</b> stick diagrams and Gate layouts, <b>Transistor Scaling</b> <b>Introduction to finFET:</b> Brief History, Construction, Advantages and Disadvantages, Applications.	

<b>Practical's:</b>	
1.	a Realize CMOS Logic-universal gates. b Practice question: Realize XOR/XNOR gates
2.	a Realization of CMOS - adder circuits b Practice question: Realize 4-bit adder/subtractor
3.	a MOS device Characterization b Practice question: Plot $g_m$ Vs $V_{GS}$ for NMOS/PMOS
4.	a Inverter Static Characteristics b Practice question: Plot the Voltage Transfer Characteristic graph of CMOS inverter and calculate the switching voltage for the given specification

5.	a Sequential Circuit Design using Master-Slave configuration b Practice question: Realize 4-bit Ring counter/Johnson counter
6.	Inverter layout and post simulation
7.	a NOR/NAND gates layout and post simulation b Practice question: Realize AND/OR gates
8.	Realize 2-bit multiplier circuit using Mixed mode
9.	a Design 6- transistor binary SRAM cell using FinFET b Practice question: Design 9T/10T binary CAM cell using FinFET
<b>Case study:</b> ASIC design flow using Innovas. (Students should learn the concept and produce the relevant document)	

<b>Course Outcomes: After completing the course, the students will be able to</b>	
<b>CO1:</b>	Analyze transistor circuits and its impact on VLSI design flow.
<b>CO2:</b>	Apply & analyze the design parameters for speed, area & power optimization.
<b>CO3:</b>	Evaluate the functionality of VLSI blocks using various architectures.
<b>CO4:</b>	Analyze various fabrication processes for different logic families/designs.

<b>Reference Books</b>	
1	CMOS VLSI Design, Neil H.E. Weste, David Harris, Ayan Banerjee, 3 <sup>rd</sup> Edition, 2006, Pearson Education, ISBN: 0321149017.
2	CMOS Digital Integrated Circuits, Sung MO Kang, Yousf Leblebici, 3 <sup>rd</sup> Edition, Tata McGrawHill, ISBN: 0-7923-7246-8.
3	Basic VLSI Design, Douglas.A.Pucknell, Kamaran Eshraghian, 3 <sup>rd</sup> Edition 2010 ,PHI, ISBN: 0-321-26977-2.
4	FinFET Modeling for IC Simulation and Design Using the BSIM-CMG Standard, Yogesh Chauhan Darsen Duane Lu Vanugopalan Sriramkumar Sourabh Khandelwal Juan Duarte Navid Payvadosi Ai Niknejad Chenming Hu, 1 <sup>st</sup> Edition 2015, Academic Press, ISBN: 9780124200319.

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20.

**Total CIE is 30(Q) +50(T) +20(EL) =100 Marks**

**Scheme of Continuous Internal Evaluation (CIE); Practical Test for 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average marks (AM) over number of weeks is considered for 30 marks. At the end of the semester a test (T) is conducted for 10 marks. The students are encouraged to implement additional innovative experiments (IE) in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

**Total CIE is 30(AM) +10 (T) +10 (IE) =50 Marks.**

**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part A and Part B. Part A consists of objective type questions for 20 marks covering the complete syllabus. Part B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice.

Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**Scheme of Semester End Examination (SEE); Practical Exam for 50 Marks**

SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

**Semester End Evaluation (SEE): Theory (100 Marks) + Practical (50 Marks) = Total 150 Marks**

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	-	3	-	-	-	1	-	-	2
CO2	3	2	3	2	3	-	1	-	-	-	-	2
CO3	3	3	2	2	3	-	-	-	-	1	-	1
CO4	1	1	3	3	3	-	2	1	-	1	-	1

**Low-1 Medium-2 High-3**

**Semester: V****Digital Signal Processing and Machine Learning**

<b>Course Code</b>	:	18EC55	<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:1:0	<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L	<b>SEE Duration</b>	:	03 Hours

**Course Learning Objectives:** The students will be able to

1	Understand concepts of digital IIR and FIR filter theory.
2	Acquire basic knowledge of machine learning algorithms or techniques.
3	Design, compare and select filters for various application.
4	Identify and apply the appropriate machine learning technique for prediction and classification

**Unit-I****07 Hrs**

**IIR Filter Design:** Structures of IIR: Direct form structure, A/D-H(z)-D/A structure Analog filter design using Butterworth and Chebyshev filter. IIR Filter design by Bilinear Transformation, digital filter designs based on the Bilinear Transformation using analog filter.

**Unit – II****07 Hrs**

**FIR Filter Design:** Symmetric and anti-symmetric FIR Filters, FIR Filter structure: Direct form structure, cascade form structures, frequency sampling structures, lattice structure. Design of Linear phase FIR Filters using Windows, Design of Linear phase FIR filters by frequency Sampling method.

Applications of IIR and FIR filters. Induction to adaptive filter and adaptive systems.

**Unit –III****08 Hrs**

**Introduction to Machine learning:** Types and applications of Machine Learning, Basic Types of Data in Machine Learning, Exploring Structure of Data, Data Quality and Remediation, Data Pre-Processing. Learning Algorithms.

**Supervised Learning Algorithm:** Linear Regression, logistic regression, Capacity, Over fitting and Under fitting, Hyper parameters and Validation Sets, Estimators, Bias and Variance, Maximum Likelihood Estimation, Bayesian Linear Regression, Stochastic Gradient Descent, Back Propagation algorithm.

**07 Hrs**

**Supervised Learning Algorithms:** Classification Model, Classification Learning Steps, Linear and logistic classifier, Support vector machines, k-Nearest Neighbour, Decision tree, Random forest model, Naïve Bayes classifier. Application of Supervised Learning, Clustering.

**07 Hrs**

**Unsupervised Learning:** Unsupervised vs Supervised Learning, Application of Unsupervised Learning, Clustering, K-means Clustering, Mixtures of Gaussians, EM for Gaussian mixtures, Principal Component Analysis.

**Course Outcomes: After completing the course, the students will be able to**

<b>CO1:</b>	Know the characteristics and structures of IIR , FIR and adaptive systems
<b>CO2:</b>	Use the concept of filter design, machine learning to analyse and acquire knowledge about the system and select proper tools for further analysis.
<b>CO3</b>	Design, implementation, analysis and comparison of digital filters for processing of discrete time signals and also various machine learning algorithms.
<b>CO4:</b>	Assess the techniques, skills, and modern engineering tools necessary for analysis of different signals and filtering out noise signals in engineering practice.

**Reference Books**

1	Proakis G, Dimitris G. Manolakis; “Digital Signal Processing”; PHI; 4th Edition; 2007; ISBN: 978-0131873742.
2	Alan .V.Oppenheim; “Discrete Time Signal Processing”; PHI; 2nd Edition; 1998; ISBN:0-13-754920-2
3	Christopher M Bishop: “Pattern Recognition and Machine Learning”, Springer, 2006, ISBN-13: 978-0387-31073-2.
4	Trevor Hastie, Robert Tibshirani, and Jerome Friedman: “The Elements of Statistical Learning”,Springer, 2008, ISBN 978-0387848570
5	Goodfellow, Y, Bengio, A. Courville, “Deep Learning”, MIT Press, 2016, ISBN- 0262035618

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**CO-PO Mapping**

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	1	-	2
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CO3	3	3	2	1	2	-	-	-	-	1	2	2
CO4	3	3	3	1	2	-	-	1	1	1	2	2

**High-3: Medium-2 : Low-1**

<b>Semester: V</b>			
<b>AUTOMOTIVE ELECTRONICS</b>			
<b>(Group F: Global Elective)</b>			
<b>Course Code</b>	:	18G5B05	<b>CIE Marks</b>
<b>Credits: L:T:P</b>	:	3:0:0	<b>SEE Marks</b>
<b>Hours</b>	:	36L	<b>SEE Duration</b>

<b>Course Learning Objectives: The students will be able to</b>			
<b>1</b>	Acquire the knowledge of automotive domain fundamentals, need of Electronics and communication interfaces in Automotive systems.		
<b>2</b>	Apply various types of sensors, actuators and Motion Control techniques in Automotive systems		
<b>3</b>	Understand digital engine control systems and Embedded Software's and ECU's used in automotive systems.		
<b>4</b>	Analyse the concepts of Diagnostics, safety and advances in Automotive electronic Systems.		

<b>UNIT-I</b>		<b>7 Hrs</b>
<b>Fundamentals of Automotive:</b> Evolution and Use of Electronics in Automotive, Automotive Systems, The Engine, Engine Control, Internal Combustion Engines, Spark Ignition Engines and Alternative Engines. Ignition System, Ignition Timing, Drivetrain, Suspensions, Brakes and Steering Systems.		
<b>Basics of electronic engine control:</b> Motivation for Electronic Engine Control, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition.		

<b>UNIT-II</b>		<b>7 Hrs</b>
<b>Automotive Sensors and Actuators:</b> Automotive Control System Applications of Sensors and Actuators, <b>Sensors:</b> Air Flow Sensor, Engine Crankshaft Angular Position Sensor, Throttle Angle Sensor, Temperature Sensor, Sensors for Feedback Control, Sensors for Driver Assistance System: Radar, Lidar, Video Technology. <b>Actuators:</b> Solenoids, Piezo Electric Force Generators, Fluid mechanical Actuators, Electric Motors and Switches.		

<b>UNIT-III</b>		<b>8 Hrs</b>
<b>Digital Engine Control Systems:</b> Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed Loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System.		
<b>Vehicle Motion Control:</b> Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS), Electronic Suspension System, Electronic Steering Control.		

<b>UNIT-IV</b>		<b>7 Hrs</b>
<b>Automotive Communication Systems:</b> Automotive networking: Bus systems, Technical principles, network topology. Buses in motor vehicles: CAN, Flex Ray, LIN, Ethernet, IP, PSI5, MOST, D2B and DSI.		
<b>Automotive Embedded Software Development</b> Fundamentals of Software and software development lifecycles. Overview of AUTOSAR methodology and principles of AUTOSAR Architecture.		

<b>UNIT-V</b>		<b>7 Hrs</b>
<b>Diagnostics and Safety in Automotive:</b> Timing Light, Engine Analyzer, Electronic Control System Diagnostics: Onboard diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems, Case study on ON-BOARD, OFF-BOARD diagnostics.		
<b>Advances in Automotive Electronic Systems:</b> Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Navigation: Navigation Sensors, Radio Navigation, dead reckoning navigation, Video based driver assistance systems, Night vision Systems.		

<b>Course Outcomes: After completing the course, the students will be able to</b>			
<b>CO1:</b>	Acquire the knowledge of automotive domain fundamentals, need of Electronics and communication interfaces in Automotive systems.		
<b>CO2:</b>	Apply various types of sensors, actuators and Motion Control techniques in Automotive systems		
<b>CO3:</b>	Analyze digital engine control systems and Embedded Software's and ECU's used in automotive systems.		
<b>CO4:</b>	Illustrate the concepts of Diagnostics, safety and advances in Automotive electronic Systems.		

Reference Books	
1.	Understanding Automotive Electronics, Williams. B. Ribbens, 6 <sup>th</sup> Edition, 2003, Elsevier science, Newness publication, ISBN-9780080481494.
2.	Automotive Electronics Handbook, Robert Bosch, 2004, John Wiley and Sons, ISBN- 0471288357
3.	Automobile Electrical and Electronic Systems, Tom Denton, Third edition, Elsevier Butterworth-Heinemann. ISBN 0-7506-62190.
4.	Advanced Automotive Fault Diagnosis, Tom Denton, Second edition, Elsevier Butterworth-Heinemann. ISBN 0-75-066991-8.

#### Continuous Internal Evaluation (CIE); Theory (100 Marks)

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#### Semester End Evaluation (SEE); Theory (100 Marks)

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	1	-	-	-	1	2	1	-	1
CO2	3	2	1	1	1	-	1	1	1	1	-	1
CO3	3	2	2	2	1	-	1	1	2	1	-	1
CO4	3	2	2	2	-	1	2	1	1	1	-	1



<b>VI Semester</b>			
<b>INTRODUCTION TO MANAGEMENT AND ECONOMICS</b>			
<b>Course Code</b>	: 18HEM61	<b>CIE Marks</b>	: 100
<b>Credits: L:T:P:</b>	: 3:0:0	<b>SEE Marks</b>	: 100
<b>Hours:</b>	: 36L	<b>SEE Duration</b>	: 3 Hrs
<b>Course Learning Objectives: The students will be able to</b>			
1. Understand the evolution of management thought.			
2. Acquire knowledge of the functions of Management.			
3. Gain basic knowledge of essentials of Micro economics and Macroeconomics.			
4. Understand the concepts of macroeconomics relevant to different organizational contexts			
<b>Unit – I</b>			<b>07Hrs</b>
<b>Introduction to Management:</b> Management Functions, Roles & Skills, Management History – Classical Approach: Scientific Management & Administrative Theory, Quantitative Approach: Operations Research, Behavioral Approach: Hawthorne Studies, Contemporary Approach: Systems & Contingency Theory.			
<b>Unit – II</b>			<b>06 Hrs</b>
<b>Foundations of Planning:</b> Types of Goals & Plans, Approaches to Setting Goals & Plans, Strategic Management Process, Corporate & Competitive Strategies.			
<b>Organizational Structure &amp; Design:</b> Overview of Designing Organizational Structure: Work Specialization, Departmentalization, Chain of Command, Span of Control, Centralization & Decentralization, Formalization, Mechanistic & Organic Structures.			
<b>Unit – III</b>			<b>06 Hrs</b>
<b>Motivating Employees:</b> Early Theories of Motivation: Maslow’s Hierarchy of Needs Theory, McGregor’s Theory X & Theory Y, Herzberg’s Two Factor Theory, Contemporary Theories of Motivation: Adam’s Equity & Vroom’s Expectancy Theory.			
<b>Managers as Leaders:</b> Behavioral Theories: Ohio State & University of Michigan Studies, Blake & Mouton’s Managerial Grid, Contingency Theories of Leadership: Hersey & Blanchard’s Situational Leadership, Contemporary Views of Leadership: Transactional & Transformational Leadership.			
<b>Unit – IV</b>			<b>07 Hrs</b>
Importance of Economics, Microeconomics and Macroeconomics, Theories and Models to Understand Economic Issues, An Overview of Economic Systems			
Demand, Supply, and Equilibrium in Markets for Goods and Services, Price Elasticity of Demand and Price Elasticity of Supply, Elasticity and Pricing, Changes in Income and Prices Affecting Consumption Choices, Monopolistic Competition, Oligopoly.			
<b>Unit – V</b>			<b>07 Hrs</b>
<b>Essentials of Macroeconomics:</b> Prices and inflation, Exchange rate, Gross domestic product (GDP), components of GDP, the Labor Market, Money and banks, Interest rate, Macroeconomic models- an overview, Growth theory, The classical model, Keynesian cross model, IS-LM-model, The AS-AD-model, The complete Keynesian model, The neo-classical synthesis, Exchange rate determination and the Mundell-Fleming model			
<b>Course Outcomes:</b>			
After the successful completion of the course, the students will be able to:			
1. Explain the principles of management theory & recognize the characteristics of an organization.			
2. Demonstrate the importance of key performance areas in strategic management and design appropriate organizational structures and possess an ability to conceive various organizational dynamics.			
3. Select & Implement the right leadership practices in organizations that would enable systems orientation.			
4. Understand the basic concepts and principles of Micro economics and Macroeconomics.			

<b>Reference Books:</b>	
1.	Stephen Robbins, Mary Coulter & Neharika Vohra, Management, Pearson Education Publications, 10 <sup>th</sup> Edition, ISBN: 978-81-317-2720-1.
2.	James Stoner, Edward Freeman & Daniel Gilbert Jr, Management, PHI, 6 <sup>th</sup> Edition, ISBN: 81-203-0981-2.

3.	Steven A. Greenlaw ,David Shapiro,Principles of Microeconomics,2nd Edition,ISBN:978-1-947172-34-0
4.	Dwivedi.D.N, Macroeconomics: Theory and Policy,McGraw Hill Education; 3rd Edition,2010,ISBN-13: 978-0070091450.
5.	Peter Jochumzen, Essentials of Macroeconomics, 1 <sup>st</sup> Edition., 2010, ISBN:978-87-7681-558-5.

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

**CO-PO Mapping**

CO/ PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	H	---	L	---	----	H	----	H	H	H	H	H
CO2	H	M		---	---	---	----	L	M	H	M	M
CO3	---	---	L	---	---	M	---	M	M	H	H	H
CO4	M	---	M	---	----	H	L	H	M	M	H	H

<b>Semester: VI</b>						
<b>COMPUTER NETWORKS AND PROTOCOLS</b>						
<b>(Theory &amp; Practice)</b>						
<b>Course Code:</b>	:	18EC62		<b>CIE Marks</b>	:	100+50
<b>Credits: L:T:P</b>	:	3:0:1		<b>SEE Marks</b>	:	100+50
<b>Hours:</b>	:	36L + 33P		<b>SEE Duration</b>	:	03Hrs+03Hrs
<b>Course Learning Objectives: The students will be able to</b>						
<b>1</b>	Develop awareness towards basic internetworking principles.					
<b>2</b>	Analyze various aspects involved in multiple accesses, various data switching techniques.					
<b>3</b>	Explain protocols operating at different layers of computer networks					
<b>4</b>	Analyze various data compression techniques and security issues.					
<b>5</b>	Analyze various aspects involved in network control and traffic management.					

<b>UNIT-I</b>	<b>07Hrs</b>
<b>Computer Networks and the Internet:</b> Internet, Protocol, Network Edge, Network Core, Access Networks and Physical Media, Delay and Loss in Packet-Switched Networks, Protocol Layers and Their Service Models, Internet Backbones, NAPs, and ISPs. Network models, OSI, TCP/IP. Physical Layer: Introduction to Guided and unguided physical media	

<b>UNIT-II</b>	<b>07 Hrs</b>
<b>Local Area Networks and Connecting Devices:</b> Data Link layer Services, Data link control-Framing, Flow & error control, Multiple Access Protocols-Random Access protocols LAN Addresses and ARP, IEEE 802.3 LANs, Ethernet, Hubs, Bridges, and Switches, Virtual LAN, PPP: The Point-to-Point Protocol, X.25 and Frame Relay. IEEE 802.11 LANs	

<b>UNIT-III</b>	<b>07 Hrs</b>
<b>Network Layer-Logical Addressing&amp; Internet Protocol</b> Network Layer, Logical Addressing, IPV4 Addresses, Structure, Address Space, Classful Addressing, Classless Addressing, Network Address Translation. IPv6 Addresses, Structure, Address Space of IPV6, Transition from IPV4 to IPV6 Forwarding. Subnet addressing. Inter- and intra-domain routing. Datagram networks; virtual circuits. RIP, OSPF, BGP. CI	

<b>UNIT-IV</b>	<b>07 Hrs</b>
<b>Transport Layer:</b> Process to Process Delivery, Connectionless Versus Connection Oriented Service, UDP, TCP. Congestion control and resource allocation-Issues in resource allocation, Queuing disciplines congestion control. Slow start. Fast retransmit. Fast recovery. Rate-based congestion control. Congestion avoidance mechanisms. Leaky Bucket Algorithm	

<b>UNIT-V</b>	<b>08 Hrs</b>
<b>Multimedia Networking:</b> Properties of Audio, Types of multimedia Network Applications, Streaming stored video: UDP Streaming, HTTP Streaming, Adaptive steaming and DASH, Content distribution Networks. Case studies: Netflix, You Tube and Kankan Network support for Multimedia: Dimensioning Best-Effort Networks. Providing multiple classes of service, Different services, Per-connection Quality of service (QOS) Guarantees: Resource Reservation and Call admission.	

<b>Practical's: CCN Lab</b>	
<b>Practical's: Computer Communication Networks Lab</b>	
<b>Part –I: Experiments Using C/C++ programming.</b>	
1) a)Implement Bit stuffing Algorithm b)Character stuffing algorithms and c)Cyclic Redundancy Check codes for error detection using C programs.	
2) Implement Encryption and Decryption algorithms using C program.	
3) Implement following Minimum Spanning Tree algorithms using C program	
i) Kruskal's Algorithm ii) Prim's Algorithms	
4) Implement STOP and WAIT protocol using socket programming concept using C Program.	
5) Implement RSA algorithm using C program.	
<b>Part-II: Experiments that may be carried out using QualNet/NS-3/Packet Tracer</b>	

1 Simulate & Analyze CSMA/CD and CSMA/CA Protocols.	
2 Test and verify Network configurations using Packet Tracer.	
3 Configure Inter VLAN network using Packet Tracer	
4 Configure and test a given network using Packet Tracer	
Simulation of congestion control algorithms using NS-3	

<b>Course Outcomes: After completing the course, the students will be able to</b>	
CO1:	Acquire the knowledge of network architecture, topologies and security issues.
CO2:	Design a network for given configuration by assigning IP addresses.
CO3:	Analyze various aspects involved in network control and traffic management
CO4:	Analyze the performance of various scheduling algorithms

<b>Reference Books</b>	
1.	Computer Networks- A System Approach, Larry L Peterson, Bruce S Davie, 4 <sup>th</sup> edition, 2007, ELSEVIER publication, ISBN: 978-0123705488
2.	Data Communication and Networking, B Forouzan, 4 <sup>th</sup> Edition, 2006, TMH, ISBN: 0-07-010829-3
3.	Computer Networks, James F. Kurose, Keith W. Ross, 2 <sup>nd</sup> Edition, 2003, Pearson Education, ISBN: 0199217637
4.	Computer Communication Networks, Andrew S Tanenbaum and David J Wetherall, 5 <sup>th</sup> Edition, 2010, Person Education. ISBN :978-0-13-212695-3
5.	Multimedia Networks: Protocols, Design and Application Hans W. Barz, Gregory A. Bassett, WILEY publication, ISBN: 978-1-119-09013-7

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**Total CIE is 30(Q) +50(T) +20(EL) =100 Marks**

#### **Scheme of Continuous Internal Evaluation (CIE); Practical Test for 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average marks (AM) over number of weeks is considered for 30 marks. At the end of the semester a test (T) is conducted for 10 marks. The students are encouraged to implement additional innovative experiments (IE) in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

**Total CIE is 30(AM) +10 (T) +10 (IE) =50 Marks.**

#### **Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part A and Part B. Part A consists of objective type questions for 20 marks covering the complete syllabus. Part B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

#### **Scheme of Semester End Examination (SEE); Practical Exam for 50 Marks**

SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

**Semester End Evaluation (SEE): Theory (100 Marks) + Practical (50 Marks) = Total 150 Marks**

<b>Semester: VI</b>						
<b>COMMUNICATION SYSTEMS II</b>						
<b>(Theory &amp; Practice)</b>						
<b>Course Code</b>	:	18EC63		<b>CIE</b>	:	100+50 Marks
<b>Credits: L:T:P</b>	:	3:1:1		<b>SEE</b>	:	100+50 Marks
<b>Total Hours</b>	:	36L+33P		<b>SEE Duration</b>	:	03 + 03 Hours

<b>Course Learning Objectives:</b> The students will be able to	
<b>1</b>	Identify the digital communication system as a series of functional blocks and the concepts of signal and channel representation.
<b>2</b>	Apply the concept of signal conversion to symbols and symbol processing in transmitter and receiver blocks.
<b>3</b>	Compute performance issues and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
<b>4</b>	Compute and mitigate for performance parameters in corrupted and distorted channel conditions.

<b>UNIT-I</b>	<b>09 Hrs</b>
<b>Digital Communication Transmitter:</b>	
Digital communication blocks and impediments. Bandpass and equivalent low pass signal representation, Quadrature Sampling of bandpass signals, Bandpass Sampling Theorem statement with Applications. Geometric Representation of Signals in terms of a low pass basis set, Gram Schmidt procedure, conversion statement to bandpass basis set. Geometric representation of signals: Baseband modulated signals with examples Bandpass band limited signals - BPSK, QPSK, M-PSK, M-QAM. Transmitter Architectures and PSD, Power limited – FSK, DPSK, MSK and applications.	

<b>UNIT-II</b>	<b>09 Hrs</b>
<b>Communication through AWGN Channels:</b>	
<b>Detection :</b> Center point sampling, Matched Filter, and Correlation Receiver.	
<b>Estimation Basics</b> - MAP and MLI Estimation of Binary signals with AWGN, Probability of error for binary signaling, Probability of error for binary baseband pulses (Line codes).	
<b>Coherent demodulation scheme</b> – BPSK, QPSK, BFSK Receiver Architecture, Probability of symbol error.	
<b>Coherent Demodulation scheme for multiple signals</b> – M-PAM, M-PSK and M-QAM. Union Bounded Probability of error these signals, Lower and upper bounds.	

<b>UNIT-III</b>	<b>07 Hrs</b>
<b>Communication Through AWGN Signals</b> (contd) - Non-Coherent demodulation of BFSK and DPSK – Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (Without derivation).	
<b>Communication through Band Limited Channels:</b> Digital Transmission through Band limited channels - Inter Symbol Interference, Signal design for Band limited ideal channel with zero ISI – Nyquist Criterion (statement only), Sinc and Raised pulse shaping.	
Signal design for Band limited channel with controlled ISI – Correlative coding, DB and MDB, with and without Precoding.	

<b>UNIT-IV</b>	<b>07 Hrs</b>
<b>Convolution Codes:</b> Encoding of convolution Codes, Transfer function and distance properties, Maximum Likelihood sequence decoding – Viterbi search Algorithm with Hard and soft decision, Probability of error statement only (No derivation).	

<b>UNIT-V</b>	<b>07 Hrs</b>
<b>Principles of Spread Spectrum (SS)</b> Concept of Spread Spectrum, Direct Sequence/SS, Frequency Hopped SS, Processing Gain, Interference, and probability of error statement only. <b>PN sequences for Spread Spectrum</b> – M-sequences with Properties; Gold, Kasami sequences with basic properties. Spread Spectrum Synchronization (Block diagram treatment) - Code Acquisition and Tracking.	

<b>Practical's: Communication systems 2 Lab</b>	
1. a) Pulse Amplitude Modulation and Demodulation using MATLAB b) Pulse Amplitude Modulation and Demodulation using DSP processor	
2. a) ASK Modulation and Demodulation using MATLAB b) ASK Modulation and Demodulation using DSP processor.	
3. a) BFSK Modulation and Demodulation using MATLAB b) BFSK Modulation and Demodulation using DSP processor	

4.	a) BPSK Modulation and Demodulation using MATLAB b) BPSK Modulation and Demodulation using DSP processor
5.	a) QPSK Modulation and Demodulation using MATLAB b) QPSK Modulation and Demodulation using DSP processor
6.	MSK Modulation and phase trellis using MATLAB
7.	QAM modulation and demodulation using MATLAB Communication systems toolbox
8.	a) Duobinary and modified duobinary coding with and without precoding using MATLAB b) Generation of PN Sequences for spread spectrum communication using MATLAB
9.	a) Convolution encoding for a given input sequence using MATLAB b) Convolution decoding using Viterbi hard decision decoding using MATLAB
Simulation of direct sequence Spread Spectrum and Frequency Hopped Spread Spectrum using MATLAB	

<b>Course Outcomes: After completing the course, the students will be able to</b>	
CO1:	Associate and apply the concepts of Bandpass sampling to well specified signals and channels.
CO2:	Analyze and compute performance parameters and transfer rates for low pass and bandpass symbol under ideal and corrupted non-band limited channels.
CO3:	Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.
CO4:	Demonstrate by simulation and emulation bandpass signals subjected to convolution coding and symbol processed at transmitter and correspondingly demodulated and estimated at receiver after passing through a corrupted channel.

<b>Reference Books</b>	
1.	Digital Communication Systems, Simon Haykin ,1 <sup>st</sup> Edition, 2013, John Wiley and sons, ISBN-978 81 265 2151 7.
2.	Communication systems, Simon Haykin, 3 <sup>rd</sup> or 4 <sup>th</sup> Edition, Reprinted 2013, John Wiley & sons, ISBN 0-471-17869-1.
3.	Modern Digital and Analog communication Systems, B.P.Lathi and Zhi Ding, 4 <sup>th</sup> Edition, 2010, Oxford University Press, , ISBN: 9780198073802.
4.	Digital Communications, Ian A. Glover, Peter M. Grant, 3 <sup>rd</sup> Edition, 2010, Pearson Educations, ISBN:978-0-273-71830-7
5.	Communication System, Bruce Carlson and P.B Chilly, 5 <sup>th</sup> Edition,2011, Tata McGraw-Hill,ISBN: 13: 9780071321174

### **Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20.

**Total CIE is 30(Q) +50(T) +20(EL) =100 Marks**

### **Scheme of Continuous Internal Evaluation (CIE); Practical Test for 50 Marks**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average marks (AM) over number of weeks are considered for 30 marks. At the end of the semester a test (T) is conducted for 10 marks. The students are encouraged to implement additional innovative experiments (IE) in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

**Total CIE is 30(AM) +10 (T) +10 (IE) =50 Marks.**

### **Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks are executed by means of an examination. The Question paper for the course contains two parts, Part A and Part B. Part A consists of objective type questions for 20 marks covering the complete syllabus. Part B consists of five main questions, one from each unit for 16 marks adding up to 80 marks.

Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

**Scheme of Semester End Examination (SEE); Practical Exam for 50 Marks**

SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

**Semester End Evaluation (SEE): Theory (100 Marks) + Practical (50 Marks) = Total 150 Marks**

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	3	-	-	1	-	1	-	1
CO2	3	2	2	1	3	-	-	1	-	1	-	1
CO3	3	3	2	2	3	-	-	1	-	1	-	1
CO4	3	3	3	3	3	-	-	1	-	1	-	1

Low-1 Medium-2 High-3

**Semester: VI**

**INTERNET OF THINGS AND EDGE COMPUTING**

**Group C: Professional Elective  
(Common to CS, EC, EE, EI, IM, IS & ET)**

<b>Course Code</b>	:	18CS6C1	<b>CIE Marks</b>	:	<b>100</b>
<b>Credits: L:T:P</b>	:	3:0:0	<b>SEE Marks</b>	:	<b>100</b>
<b>Total Hours</b>	:	36L	<b>SEE Duration</b>	:	<b>3 Hrs</b>

**Course Learning Objectives:** The students will be able to

1.	Understand design principles in IoT, Edge, Fog computing and its challenges
2.	Identify the Internet Connectivity and its protocols
3.	Explore and implement Internet of Things (IoT) and New Computing Paradigms
4.	Apply and analyze the Orchestration and resource management in IoT, 5G, Fog, Edge, and Clouds

**Unit – I**

**6 Hrs**

**FUNDAMENTAL IOT MECHANISM AND KEY TECHNOLOGIES**-Identification of IoT Object and Services, Structural Aspects of the IoT, Key IoT Technologies. Evolving IoT Standards Overview and Approaches, IETF IPv6 Routing Protocol for RPL Roll, Constrained Application Protocol, Representational State Transfer, ETSI M2M, Third Generation Partnership Project Service Requirements for Machine-Type Communications, CENELEC, IETF IPv6 Over Low power WPAN, Zigbee IP(ZIP), IPSO

**Unit – II**

**10 Hrs**

**LAYER ½ CONNECTIVITY:** Wireless Technologies for the IoT-WPAN Technologies for IoT/M2M, Cellular and Mobile Network Technologies for IoT/M2M. **Application Protocols**- Common Protocols, Web service protocols, MQ telemetry transport for sensor networks (MQTT-S) , ZigBee compact application protocol (CAP) , Service discovery ,Simple Network Management Protocol(SNMP)

**Unit – III**

**10 Hrs**

**Sensor Technologies for IoT Devices**, Prototyping concepts, Basics of Embedded computing, Embedded platforms for prototyping, IoT Connected devices through Cloud Designing software for IoT, Prototyping embedded device software, Case Study& Advanced IoT Applications: Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / ARM Cortex/ Arduino)- Block diagram, specifications.

**Unit – IV**

**7 Hrs**

**Internet of Things (IoT) and New Computing Paradigms** Fog and Edge Computing Completing the Cloud ,Advantages of FEC: SCALE , How FEC Achieves these Advantages: SCANC 9,Hierarchy of Fog and Edge Computing , Business Models ,**Addressing the Challenges in Federating Edge Resources** The Networking Challenge , The Management Challenge ,**Integrating IoT + Fog + Cloud**

**Unit – V**

**6 Hrs**

**Management and Orchestration of Network Slices in 5G, Fog, Edge, and Clouds** Introduction, Background, Network Slicing in 5G, Network Slicing in Software-Defined Clouds, Network Slicing Management in Edge and Fog

**Course Outcomes: After completing the course, the students will be able to**

<b>CO 1:</b>	Understand and Explore Internet of Things (IoT) with New Computing Paradigms like 5G, Fog, Edge, and Clouds
<b>CO 2:</b>	Analyze Prototyping and demonstrate resource management concepts in New Computing Paradigms
<b>CO 3:</b>	Apply optimal wireless technology to implement Internet of Things and edge computing applications
<b>CO 4:</b>	Propose IoT-enabled applications for building smart spaces and services with resource management and edge computing

**Reference Books:**

1.	Internet of Things: Architecture and Design Principles, Raj Kamal, 1 <sup>st</sup> Edition, 2017, TMH Publications, ISBN: 9789352605224
2.	Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications, Daniel Minoli, 1 <sup>st</sup> Edition, 2013, Willy Publications, ISBN: 978-1-118-47347-4,



3.	Fog and Edge Computing: Principles and Paradigms, <u>Rajkumar Buyya</u> , 1 <sup>st</sup> Edition, 2019, Wiley series on parallel and distributed computing, ISBN: 978-1-119-52498-4 , 2019.
4.	Internet of Things (A Hands-on-Approach), Vijay Madiseti and Arshdeep Bahga, 1 <sup>st</sup> Edition, 2014, VPT, ISBN: 978-0996025515

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20.

**Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

Semester: VI						
REAL TIME SYSTEMS						
(Group C: Professional Core Elective)						
Course Code	:	18EC6C2		CIE	:	100 Marks
Credits: L:T:P	:	3:0:0		SEE	:	100 Marks
Total Hours	:	36L		SEE Duration	:	03 Hours
<b>Course Learning Objectives:</b> The students will be able to						
1	Understand functional differences between different real time systems.					
2	Examine and evaluate the hardware functionality required by embedded system to achieve real-time operation.					
3	Analyse, evaluate and implement task control and real-time scheduling algorithms required to perform multitasking.					
4	Demonstrate the concept of real-time programming using tasks and gain knowledge and skills necessary to design and develop embedded applications by means of real-time operating systems.					

Unit-I		07 Hrs
<b>Introduction:</b> Overview, Architecture of Real Time Systems: Hardware and Software, Real Time Services.		
<b>System Resources:</b> Resource Analysis, Real Time Service Utility, Cyclic Executives, Timing Constraints and Modelling of Timing Constraints, Applications of Real Time System.		
Unit – II		08 Hrs
<b>Processing:</b> Scheduling Classes, Scheduler Concepts, Pre-emptive Fixed Priority Policy, Feasibility, Rate Monotonic LUB, Necessary & Sufficient Feasibility, Dead Line Monotonic, Dynamic Priority Policies.		
<b>I/O Resources:</b> WCET, Intermediate I/O, Execution Efficiency.		
Unit –III		07 Hrs
<b>RTOS Services:</b> Task Creation, Inter Task Communication: Pipes, Message Queues, Mail Box, Memory Mapped Objects; Critical Section, Shared Data Problem, Synchronization: Semaphores, Mutex; Remote Procedure and Sockets.		
<b>Real Time Memory Management:</b> Process Stack Management, Dynamic Allocation		
Unit –IV		07 Hrs
<b>Handling Resource Sharing and Dependencies Among Real-Time Tasks</b>		
Resource Sharing among Real-Time Tasks, Priority Inversion, Priority Ceiling Protocol (PCP), Priority Inheritance Protocol (PIP), Highest Locker Protocol (HLP), Types of Priority Inversion Under PCP, Racing, Deadlock, Live lock, Starvation.		
Unit –V		07 Hrs
<b>Examples of Real Time OS:</b> VxWorks: Task Management, Scheduling, Primitive Kernel Services, Application Program development using APIs		

Course Outcomes: After completing the course, the students will be able to	
CO1:	Understand the fundamental concepts of real-time system and real-time operating system.
CO2:	Analyse the given requirements, design hardware & software for real time systems.
CO3:	Apply modern engineering tools for real time firmware development & performance analysis.
CO4:	Verify the specifications of various real time operating systems used for meeting timing constraints of given problem.

Reference Books	
1	Real-Time Embedded Systems and Components, Sam Siewert, 2007, Cengage Learning India Edition, ISBN: 9788131502532
2	Real-Time Systems: Theory and Practice, Rajib Mall, 2007, Pearson, ISBN 978-81-317-0069-3
3	Real-Time Concepts for Embedded Systems, Qing Li and Carolyn Yao, 2003 CMP Books, ISBN:1578201241
4	Technical Reference Manuals: VxWorks, Posix.

### Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

### Semester End Evaluation (SEE); Theory (100 Marks)

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	2	-	-	-	-	-		-	
CO2	3	2	2	1	2	1	-	-	-	1	-	1
CO3	3	3	2	2	3	1	1	1	-	1	-	1
CO4	2	3	2	2	1	1	2	2	2	2	2	1

**High-3: Medium-2: Low-1**

<b>Semester: VI</b>			
<b>LOW POWER VLSI DESIGN</b> <b>(Group C: Professional Core Elective)</b>			
<b>Course Code</b>	<b>:</b>	18EC6C3	<b>CIE</b> <b>:</b> 100 Marks
<b>Credits: L:T:P</b>	<b>:</b>	3:0:0	<b>SEE</b> <b>:</b> 100 Marks
<b>Total Hours</b>	<b>:</b>	36L	<b>SEE Duration</b> <b>:</b> 03 Hours

<b>Course Learning Objectives:</b> The students will be able to	
<b>1</b>	Explain the need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits.
<b>2</b>	Analyze the impact of Device Technology such as Transistor sizing & gate oxide thickness and Device innovation on Low Power.
<b>3</b>	Evaluate various probabilistic based power analysis techniques at various levels of abstraction.
<b>4</b>	Compare the trade-off between accuracy and resources for both simulations based and probability-based power analysis.
<b>5</b>	Apply various logic level techniques to optimize the power dissipation of the design reducing the switching activities in the design
<b>6</b>	Design and analyze digital circuits like combinational, sequential circuits using low power concepts.

<b>Unit-I</b>	<b>07 Hrs</b>
<b>Introduction</b> Need for Low Power VLSI Design, Sources of power dissipation, Power dissipation in CMOS circuits: Short Circuit dissipation, Dynamic dissipation, load capacitance Charging and Discharging, Static Power: Leakage Currents, Static Currents, Emerging low power approaches and limits. Physics of Power Dissipation in CMOS devices, MIS structure, long channel effect, sub-micron MOSFET, Gate induced drain leakage.	
<b>Unit – II</b>	<b>07 Hrs</b>
<b>Power Estimation</b> -Signal Modeling and probability calculation, Probabilistic techniques for signal activity estimation, statistical techniques, Estimation of glitching power, power estimation using input vector compaction, power estimation at circuit level, information theory-based approach.	
<b>Unit –III</b>	<b>07 Hrs</b>
<b>Device and Technology Impact on Low Power Electronics</b> Introduction, Dynamic Dissipation in CMOS, Effects of $V_{DD}$ and $V_t$ on speed, Constraints on $V_t$ Reduction, Transistor and Gate Sizing, Transistor Sizing and Optimal Gate Oxide Thickness (Quantitative analysis only) Impact of Technology Scaling. Equivalent Pin Ordering, Network Restructuring and Reorganization, Technology and Device Innovations, Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-computational Logic, Power gating Techniques.	
<b>Unit –IV</b>	<b>07 Hrs</b>
<b>Low Power Circuit Techniques</b> Introduction, Power consumption in circuits, Circuit design styles, Analysis of adders, multipliers, Flip-Flops and Latches, Low Power Cell Library. <b>Low power SRAM architectures:</b> SRAM organization, MOS SRAM cells-4T and 6T, Banked organization of SRAMs, Reducing voltage swings on bit-lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits.	
<b>Unit –V</b>	<b>08Hrs</b>
<b>Synthesis for Low Power</b> Behavioral level transforms: Architecture-Driven Voltage Scaling, Power reduction using Operation Reduction and Substitution, logic level optimizations: circuit level transforms, CMOS gates, Power Reduction in Clock Networks: power dissipation in clock distribution, single driver Vs distributed buffers, zero sew Vs tolerable skew, CMOS Floating Nodes, Low Power Bus, Delay Balancing, Energy recovery CMOS and Adiabatic computation.	

<b>Course Outcomes: After completing the course, the students will be able to</b>	
<b>CO1:</b>	Acquire the knowledge with regard to the physical principles, analysis and the characteristics of the low power designs.
<b>CO2:</b>	Identify, formulate, and solve engineering problems in the area of low power VLSI designs.
<b>CO3:</b>	Use the techniques and skills in system designing through modern engineering tools such as logic works

	SPICE and description languages such as VHDL and Verilog.
<b>CO4:</b>	Design a digital system, components or process to meet desired needs of low power within realistic constraints.

Reference Books	
1	Low-Power CMOS VLSI Circuit Design, Kaushik Roy and Sharat Prasad, 2009, John Wiley India press, ISBN: 978-81-265-2023-7,
2	Practical Low Power Digital VLSI Design, Gary K. Yeap, 2009, Kluwer Academic Publishers, ISBN: 978-1-4613-77778-8.
3	Low Power Design Methodologies, Jan M. Rabaey and Massoud Pedram, 5 <sup>th</sup> reprint, Kluwer Academic Publishers, , ISBN: 978-1-4613-5975-3, 2002.
4	Low Power CMOS design , Anantha Chandrakasan and Robert W. Brodersen, 1998, Wiley-IEEE press, ISBN: 0-7803-3429-9.

### Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

### Semester End Evaluation (SEE); Theory (100 Marks)

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

### CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	2	1	1	1	-	-	1	1	-	3
CO2	2	2	2	1	1	1	-	-	1	1	-	3
CO3	2	2	2	1	3	2	-	-	2	1	-	3
CO4	2	2	2	1	3	2	-	-	2	1	-	3

**High-3: Medium-2: Low-1**

**Semester: VI****DATABASE MANAGEMENT SYSTEMS  
(Group D: Professional Core Elective)**

<b>Course Code</b>	:	18EC6C4	<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:0:0	<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L	<b>SEE Duration</b>	:	03 Hours

**Course Learning Objectives:** The students will be able to

<b>1</b>	Explain the fundamental differences between logical and physical database design.
<b>2</b>	Understanding of the context, phases and techniques for designing and building database information systems in business.
<b>3</b>	Explain the basic concepts of relational data model, entity relationship model, relational database design, relational algebra and database language SQL and Postgre SQL
<b>4</b>	Design and build a simple database system and demonstrate competence with the fundamental tasks involved with modelling, designing, and implementing a DBMS

**Unit-I****07 Hrs**

**Introduction:** Evolution of Data Centric Systems, Need & Purpose of Database Systems. Transaction Management, Database user categories and Database architecture, Data Modelling- ER Diagrams.

**Entity Relational Model:** Relational Model Concepts, Relational Model Constraints and Relational Database Schemas. Entity types, sets, Relationship, attribute. Integrity constraints, Referential constraints. Update Operations, Transactions and dealing with constraint violations. Concepts of Keys, Super Key, Primary, Candidate and Foreign Keys. Case Study discussions for ER Diagrams. Introduction to Mango DB.

**Unit – II****08Hrs**

**Relational Algebra :** Unary Relational Operations: SELECT and PROJECT, Relational Algebra Operations from Set Theory. Binary Relational operation: equi join, natural join, outer join and inner join. Additional relational operation  
**SQL :** SQL Data Definition and Data Types, Specifying basic constraints in SQL, Schema change statements in SQL, Basic queries in SQL, More complex SQL Queries. Insert, Delete and Update statements in SQL, Specifying constraints as Assertion and Trigger, Views (Virtual Tables) in SQL.

**Unit –III****07Hrs**

**Postgre SQL:** Data types, Creating a database, create a table, drop the database, drop table, select table, insert a record, update record, delete a record, order by, group by, triggers, substring, database keys. Postgre SQL vs MySQL.

**Unit –IV****07 Hrs**

**Database Design – 1:** Informal Design Guidelines for Relation Schemas, Functional Dependencies, Normal Forms Based on Primary Keys, General Definitions of Second and Third Normal Forms, Boyce-Codd Normal Form.  
**Database Design -2** Properties of Relational Decompositions, Algorithms for Relational Database Schema Design, Multivalued Dependencies and Fourth Normal Form, Join Dependencies.

**Unit –V****07 Hrs**

**Transaction Management:** The ACID Properties, Transactions and Schedules, Concurrent Execution of Transactions, Lock- Based Concurrency Control, Performance of locking, Transaction support in SQL, Introduction to crash recovery, 2PL, Serializability and Recoverability, Lock Management, Introduction to ARIES, The log, Other recovery-related structures, The write-ahead log protocol, Check pointing, Recovering from a System Crash, Media Recovery, Other approaches and interaction with concurrency control.

**Course Outcomes: After completing the course, the students will be able to**

<b>CO1:</b>	Understand the fundamentals of Data Base management system, entity-relationship model, Relational Algebra, Database Design, Transaction Management.
<b>CO2:</b>	Illustrate the working of data base & transactions by writing queries using SQL and Postgre SQL
<b>CO3:</b>	Analyze an information storage problem and derive an information model expressed in the form of an entity relation diagram and other optional analysis forms, such as a data dictionary.
<b>CO4:</b>	Design a data model that satisfies relational theory and provides users with business Queries, business forms and business reports.

<b>Course Outcomes: After completing the course, the students will be able to</b>	
<b>CO1:</b>	Understand the fundamentals of Data Base management system, entity-relationship model, Relational Algebra, Database Design, Transaction Management.
<b>CO2:</b>	Illustrate the working of data base & transactions by writing queries using SQL and Postgre SQL
<b>CO3:</b>	Analyze an information storage problem and derive an information model expressed in the form of an entity relation diagram and other optional analysis forms, such as a data dictionary.
<b>CO4:</b>	Design a data model that satisfies relational theory and provides users with business Queries, business forms and business reports.

<b>Reference Books</b>	
<b>1</b>	Elmasri, Navathe, “Fundamentals of Database Systems”, 5 <sup>th</sup> Edition, Pearson Education, 2007, ISBN-13: 9780321369574
<b>2</b>	Raghu Ramakrishnan, Johannes Gehrke, “Database Management Systems”, 3 <sup>rd</sup> Edition, McGraw, ISBN-10: 0072465638
<b>3</b>	DimitriFontaine, ”The art of Postgre SQL”, 2nd edition, O’Reilly Media, Inc., 2014, ISBN-9781788472296
<b>4</b>	Silberschatz, Korth, Sudharshan, “Data base System Concepts”, 6th Edition, Mc, ISBN-10: 9332901384

### **Continuous Internal Evaluation (CIE); Theory (100 Marks)**

**CIE** is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

### **Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

<b>CO-PO Mapping</b>												
<b>CO/PO</b>	<b>PO1</b>	<b>PO2</b>	<b>PO3</b>	<b>PO4</b>	<b>PO5</b>	<b>PO6</b>	<b>PO7</b>	<b>PO8</b>	<b>PO9</b>	<b>PO10</b>	<b>PO11</b>	<b>PO12</b>
<b>CO1</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	-	-	-	-	-	-	<b>2</b>
<b>CO2</b>	<b>3</b>	<b>2</b>	<b>3</b>	-	<b>3</b>	-	-	-	-	-	-	<b>2</b>
<b>CO3</b>	<b>3</b>	<b>3</b>	<b>2</b>	<b>2</b>	<b>3</b>	-	-	-	<b>2</b>	-	-	<b>2</b>
<b>CO4</b>	<b>3</b>	<b>3</b>	-	<b>2</b>	<b>3</b>	-	-	-	<b>2</b>	-	-	<b>2</b>

**High-3: Medium-2 : Low-1**

**Semester: VI****CONTROL ENGINEERING  
(Group C: Professional Core Elective)**

<b>Course Code</b>	: 18EC6C5	<b>CIE</b>	: 100 Marks
<b>Credits: L:T:P</b>	: 3:0:0	<b>SEE</b>	: 100 Marks
<b>Total Hours</b>	: 36 L	<b>SEE Duration</b>	: 3.00 Hours

**Course Learning Objectives:**

<b>1</b>	Acquire the knowledge of classical control system analysis techniques, system response and performance characteristics
<b>2</b>	Develop mathematical model and Analyze control systems using signal flow graphs and block diagram techniques.
<b>3</b>	Design a system to analyze and evaluate stability of feedback control systems using both time and frequency domain methods.
<b>4</b>	Represent a given system using state model by choosing proper state variables using physical and phase variables. Express the effects of PID controllers and compensators on the system performance

**Unit-I****08Hrs****Introduction:**

Definitions, Classification of control systems open loop and closed loop, linear and nonlinear, time variant and time invariant, continuous and discrete time systems. Block diagram of a typical closed loop control system showing the basic structure and different terminologies

**Modeling and Representation Of Control System:** The transfer function concept, transfer function of simple electrical networks, different forms of transfer functions, Modeling of mechanical translational and rotational systems.

**Unit – II****07 Hrs****Block Diagram and Signal Flow Graphs:**

Block Diagram Reduction, Signal Flow Graphs, Mason's Gain Formula (No Proof), Relative Advantages, Conversion from electrical circuit to SFG and Block diagram to SFG.

**Time Response of Feedback Control Systems:**

Standard test signals, step response of first and second order systems, time domain specifications. Type and order of the system, Steady state error and static error constants.

**Stability Analysis:** Concept of stability, types of stability, Routh Hurwitz criterion, relative stability analysis.

**Unit –III****07 Hrs**

**Root Locus:** Introduction, concept of magnitude and angle criterion, construction of root loci, root contours. Effect of adding a pole/zero to the system.

**State variable analysis:** Introduction, concept of state, state variable and state model, state modelling of linear systems.

Characteristic equation, Eigen values, Eigen vectors, generalized Eigen vectors, Similarity transformation, transformation of a state model to diagonal/Jordan canonical form.

**Unit –IV****07 Hrs**

Frequency domain specifications, concept of phase margin and gain margin, correlation between time and frequency response.

**Frequency Domain Analysis:**

Introduction to frequency domain plots. Polar plots, Principle of argument, Nyquist plots and Nyquist stability criterion. Example

**Unit –V****07Hrs****Controllers and Compensators:**

Basic control actions P, PI, PD and PID controllers and their effects on the dynamic and static behavior of the system. Lag, lead and lead-lag compensators, realization using RC networks. Design of controllers (PID) using Root locus and compensators (lag-lead) using bode plots.

**Course outcomes:** On completion of the course, the student should have acquired the ability to

<b>CO1:</b>	Comprehend the different types of control systems and their building blocks
<b>CO2:</b>	Analyze the different systems by means of their transfer function
<b>CO3:</b>	Evaluate the performance of systems and assess their stability
<b>CO4:</b>	Design the system or compensator for the desired performance parameters and explain the concepts of state



space, eigen value and Eigen vectors
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**Reference Books**

1	Control System Engineering , J Nagarath and I.J.Nagarath and M Gopal, 5 <sup>th</sup> edition, 2007, New age international publishers, ISBN: 81-224-1775-2.M.Gopal , “Control systems - Principles and design”, TMH,2 <sup>nd</sup> edition,2006, ISBN: 0071231277, 9780071231275
2	K.Ogata, “Modern control engineering”, Pearson education, 2004, 4 <sup>th</sup> edition. ISBN: 1-317-1887-2
3	Modern Control Systems , R.C. Dorf and R.H.Bishop, 12 <sup>th</sup> Edition,2010, Addison Wesley, ISBN 13: 978-0136024583
4	Automatic Control Systems, Kuo B.C 9 <sup>th</sup> Edition, 2014, .. Prentice Hall of India Ltd., New Delhi, ISBN-13: 978-8126552337

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

**SEE** for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

**CO-PO Mapping**

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	1	1	1	1	1	-	2	2	-	1
CO2	2	2	2	2	1	1	1	-	2	1	-	1
CO3	3	3	2	2	2	1	1	-	2	2	-	1
CO4	3	3	2	1	1	1	1	-	2	1	-	1

**High-3 : Medium-2 : Low-1**

Semester: VI						
Cryptography and Network Security (Group C: Professional Core Elective)						
Course Code	:	18EC6C6		CIE	:	100 Marks
Credits: L:T:P	:	3:0:0		SEE	:	100 Marks
Total Hours	:	36L		SEE Duration	:	03 Hours
<b>Course Learning Objectives:</b> The students will be able to						
1	Define the fundamentals of Security and cryptography for data transmission.					
2	Explain the principles of cryptography and encryption.					
3	Analyse modern stenographic techniques and differentiate between stenography and cryptography					
4	Explain IRM features and describe DRM systems and technologies					
5	Identify the necessity of data security in various industries.					

Unit-I		07Hrs
<b>Introduction</b> Services, Mechanism and Attacks, Model for Network Security <b>Classical Encryption Techniques</b> Symmetric Cipher Model, Substitution Techniques, Transposition Techniques, Simplified DES. Problems <b>Block Ciphers and DES (Data Encryption Standards)</b> Simplified DES Block, Cipher Principles, DES and strength of DES, Block cipher design principles and modes of operation, The AES Cipher		
Unit – II		07 Hrs
<b>Public Key Cryptography and RSA</b> Principles of Public Key Cryptosystems, RSA Algorithm, Problems <b>Other Public Key Cryptosystems and Key Management</b> Key Management, Diffie-Hellman exchange, Elliptic Curve Arithmetics, Elliptic Curve Cryptography. <b>Message Authentication and Hash Functions</b> Authentication Requirements, Authentication Functions, Message Authentication Codes(MAC), Hash Functions, Security of Hash functions and MAC's		
Unit –III		07 Hrs
<b>Authentication Applications:</b> Kerberos, X-509 Authentication Service, Public-Key Infrastructure. <b>Electronic Mail security:</b> Pretty Good Privacy, S/MIME, Data Compression using ZIP, Radix-64 Conversion. <b>IP Security</b> IP Security Architecture, Authentication Header, ESP (Encapsulating Security Pay Load), Security Associations, Key		
Unit –IV		07 Hrs
<b>Transport-Level Security: Web security Issues,</b> Security Socket Layer (SSL) and Transport Layer Security, HTTPS and Secure Shell <b>Wireless network security:</b> IEEE 802.11 Wireless LAN Overview, IEEE 802.11i Wireless LAN Security, Wireless application Protocol Overview, Wireless Transport Layer Security, WAP End-End Security		
Unit –V		08 Hrs
<b>Steganography:</b> Introduction to Steganography, Modern Techniques in Steganography, Comparison between Steganography and Cryptography, Detecting Steganography, Stegoanalysis, Applications of Steganography. <b>Information Rights Management:</b> Introduction to IRM, Features, Naming conventions of IRM. <b>Digital Right Management:</b> Introduction to DRM, Environment For DRM Systems, Evaluation Criteria for DRM Systems, Common DRM techniques, DRM technologies.		

Course Outcomes: After completing the course, the students will be able to	
CO1	Identifying external and internal threats to an organization.
CO2	Master fundamentals of secret, public key cryptography and analyze advanced security issues and technologies.
CO3	Analyze cryptographic and steganographic techniques, and differentiate between them. Evaluate & Compare different encryption algorithms.
CO4	Use of modern tools for implementing different security algorithms and comparing their robustness.

Reference Books	
1	Cryptography and Network Security, Williams Stallings, 2003, Pearson Education/PHI, ISBN: 0-13-111502-2.
2	Network Security, Perlman - Kaufman Spenciner, 2002, Pearson Education/PHI, ISBN: 9971-51-345-5.
3	Cryptography & Network Security, Atul Kahate, 2003, TMH, ISBN-81-203-2186-3.
4	Investigator's Guide to Steganography, Gregory Kipper,

### Continuous Internal Evaluation (CIE); Theory (100 Marks)

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**Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

### Semester End Evaluation (SEE); Theory (100 Marks)

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	3	-	-	-	-	-	-		-	-
CO2	3	2	2	3	-	-	-	2	2		-	-
CO3	2	2	3	3	-	-	-	2	2		-	-
CO4	3	3	3	3	2	3	2	3	3	3	2	3

**High-3: Medium-2: Low-1**

<b>Semester: VI</b>						
<b>DIGITAL SIGNAL PROCESSING USING ARM CORTEX M DEVICES</b>						
<b>(Group D: Professional Core Elective)</b>						
<b>Course Code</b>	:	18EC6D1		<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:0:0		<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L		<b>SEE Duration</b>	:	03 Hours

<b>Course Learning Objectives:</b> The students will be able to	
<b>1</b>	Understand the data processing path in digital signal processing and signal representation for processing on MCUs.
<b>2</b>	Demonstrate the skill set of configuring Codecs and writing program statements to read digital and analog signals.
<b>3</b>	Realize different signal processing operations to meet the real-world requirements.
<b>4</b>	Understand the requirements of the hardware to be used in signal processing operations.
<b>5</b>	Design application software using APIs of CMSIS to perform digital signal processing operations.

<b>Unit-I</b>	<b>07 Hrs</b>
<p><b>Introduction</b> ARM Profiles, ARM Cortex M Family, Digital Signal Controller Vs Digital Signal Processor, CMSIS, TI Math and DSP Libraries</p> <p><b>Analog Input and Output</b> Digital Signal Processing System, Data Representation, Stereo Codecs Input and Output, Data communication using Polling, Interrupts, DMA</p> <p><b>Practice:</b> STM32F407 Discovery, WM5102 Codecs Programming Examples: Configuration of Codecs, Real Time Input and Output, Demonstration of Polling, Interrupts and DMA based IO. Fixed point tool box in MATLAB.</p>	

<b>Unit – II</b>	<b>08 Hrs</b>
<p>Sampling, Reconstruction and Aliasing - Time and Frequency Domains, Fast Fourier Transform - Derivation of Radix-2</p> <p><b>Practice:</b> Sampling and Aliasing – Generating Sinusoids of Arbitrary Frequency, Step Response of the WM5102 Antialiasing Filter, Discrete Fourier Transform of a Sequence of Real Numbers, FFT of A Signal in Real-Time, Spectral Leakage</p>	

<b>Unit –III</b>	<b>07 Hrs</b>
<p><b>FIR Filters</b> Introduction, Window Method of FIR Filter Design: LP, HP, BP, BS</p> <p><b>Practice:</b> The Moving Average Filter, Observation of Frequency Response Using a Sinusoidal Input Signal, Observation of Frequency Response using a Pseudo-Random Input Signal, Demonstration of Filters Demonstration using STM32F407 Discovery and WM5102 Codec.</p>	

<b>Unit –IV</b>	<b>07 Hrs</b>
<p><b>IIR Filters</b> Introduction, Different Structures, Impulse Invariant and Bilinear Transform Methods of Design, Low Pass Filters Design</p> <p><b>Practice:</b> Design of A Simple IIR Low Pass Filter, Filter Programming Using Difference Equation, Experimental Measurement of the Magnitude Frequency Response of the Filter</p>	

<b>Unit –V</b>	<b>07 Hrs</b>
<p><b>Adaptive Filters</b> Introduction, Adaptive Prediction, System Identification or Direct Modeling, Noise Cancellation, Equalization, Performance Function, LMS Algorithm</p> <p><b>Practice:</b> Adaptive Filter using C Code, Noise Cancellation using Adaptive Filter, System Identification using Adaptive Filter, Estimating WM5102 Codec Bandwidth using two Audio Cards</p>	

<b>Course Outcomes: After completing the course, the students will be able to</b>	
<b>CO1:</b>	Describe the programmer's model of ARM processor and identify requirements to realize the signal processing operations.
<b>CO2:</b>	Realize real time signal processing applications & primitive OS operations on different ARM architectures by making use of software libraries.
<b>CO3:</b>	Apply the optimization methods available for ARM architectures to design embedded software to meet given constraints with the help of modern engineering tools.
<b>CO4:</b>	Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments.

<b>Reference Books</b>	
<b>1</b>	Digital Signal Processing on using ARM Cortex M4, Donald S Reay, 2016, John Wiley & Sons, ISBN 978-1-118-85904-9.
<b>2</b>	ARM-based Digital Signal Processing Lab-in-a-Box, ARM University Program, World Wide Education Program, ISBN- 10: 9780470936863
<b>3</b>	ARM System Developers Guide, Andrew N Sloss, Dominic Symes, Chris Wright, 2008, Elsevier, Morgan Kaufman publishers, 2008, ISBN-13:9788181476463
<b>4</b>	Technical reference manual for ARM processor cores including Cortex M, Wolfson PI Codec, Keil Products, ISBN

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

<b>CO-PO Mapping</b>												
<b>CO/PO</b>	<b>PO1</b>	<b>PO2</b>	<b>PO3</b>	<b>PO4</b>	<b>PO5</b>	<b>PO6</b>	<b>PO7</b>	<b>PO8</b>	<b>PO9</b>	<b>PO10</b>	<b>PO11</b>	<b>PO12</b>
<b>CO1</b>	<b>2</b>	<b>2</b>	<b>3</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>-</b>		<b>-</b>	<b>-</b>
<b>CO2</b>	<b>3</b>	<b>2</b>	<b>2</b>	<b>3</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>2</b>	<b>2</b>		<b>-</b>	<b>-</b>
<b>CO3</b>	<b>2</b>	<b>2</b>	<b>3</b>	<b>3</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>2</b>	<b>2</b>		<b>-</b>	<b>-</b>
<b>CO4</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>2</b>	<b>3</b>	<b>2</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>2</b>	<b>3</b>

**High-3: Medium-2: Low-1**

Semester VI					
COMPUTER VISION (Group D: Professional Core Elective)					
Course Code:	:	18EC6D2		CIE Marks	100
Credits: L:T:P	:	3:0:0		SEE Marks	100
Hours:	:	39 L		SEE Duration	3Hrs
<b>Course Learning Objectives:</b>					
1	Acquire knowledge on problem solving skills in computer vision.				
2	Select appropriate techniques or methods for Filtering, Segmenting, Recognition and classification.				
3	Describe basic feature and applications of computer vision in real time applications.				
4	Develop skills to work or carry out task on multi-disciplinary domains / projects.				

Unit-I		08 Hrs
<b>Introduction to Digital Image Fundamentals</b>		
The origin of Digital Image processing, Image acquisition, Image sensors, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Image Sampling and Quantization, Some Basic Relationships between Pixels.		
<b>Intensity Transformation and spatial Filters:</b> Background, Some basic Intensity Transformation Functions, Histogram Processing, Histogram Equalization, Mechanics of spatial filtering, spatial correlation and convolution, Smoothing spatial filters.		
Unit –II		08Hrs
<b>Early vision:</b>		
Just one image: Linear Filters, Linear Filters and Convolution, Shift Invariant Linear System, Discrete Convolution, Continuous Convolution., Edge Effects in Discrete Convolution, Spatial Frequency and Fourier Transformation, Fourier Transformation, Sampling and Aliasing, Filters as Templates, Technique: Normalized correlation and Finding Patterns, Technique: Scale and Image Pyramids		
<b>Image Segmentation</b>		
Fundamentals, Point, Line Edge detection, Detection of Isolation points, Line detection, Edge Models , basic Edge detection, More Advanced Techniques for Edge Detection , Edge Linking and Boundary Detection, Thresholding : Foundation, Basic global thresholding, Region growing, Region splitting and Merging.		
Unit –III		08Hrs
<b>Image Segmentation by Clustering</b>		
Background subtraction, shot boundary detection, interactive segmentation, forming image regions.		
<b>Image segmentation by clustering pixels:</b> Basic clustering methods, watershed algorithm, K-means, Mean shift: Finding Local modes in Data, clustering and segmentation with Mean shift, terminology and facts for graphs, Agglomerative clustering with a graph, divisive clustering with a graph.		
Unit –IV		07Hrs
<b>Learning Phase to classification</b>		
Classification, error and loss: using loss to determine decisions, training error, test error and overfitting, regularization, error rate and cross validation.		
Major classification strategies: Mahalanobis distance, class conditional histograms and Naive Bayes, classification using Nearest Neighbors, Linear Support vector Machine, Kernel machines, Boosting and Adaboost. Case study with deep neural networks, Baidu, Google		
Practical methods for Building classifiers: Manipulating training data to improve performance, Building multiclass classifiers out of Binary classifiers, solving for SVMs and Kernal machines.		
Unit –V		08 Hrs
<b>Detecting Objects in images</b>		
The sliding window method, Face detection, Detecting Humans, Detecting Boundaries, Detecting deformable objects		
<b>Topics in Object Recognition</b>		
Object recognition current strategies of object recognition, categorization , Selection, improving current Image features, other kinds of Image Features, Geometrical , Semantic Questions, Attributes and unfamiliar, parts poselets and consistency, chunks of meanings		

<b>Course Outcomes: After completing the course, the students will be able to</b>	
CO1.	Explore and acquire knowledge on fundamentals of computer vision concepts.
CO2.	Analyze the inherent difficulties encountered in computer vision and its interpretation.
CO3.	Apply computer vision techniques to solve complex problems.
CO4.	Investigate and draw inferences by processing image in real time applications.

<b>Reference Books</b>	
1.	Digital Image Processing, Rafael C. Gonzalez, Richard E. Woods, 3 <sup>rd</sup> Edition; 2012, Pearson Education, ISBN- 9780131687288.
2.	Computer Vision: A Modern Approach, David Forsyth and Jean Ponce, 2nd edition, 2015, Prentice Hall, ISBN- 978-81-203-5060-1.
3.	Tinku Acharya , Ajoy K. Ray “Image Processing-Principles and Applications” John Wiley & Sons, Inc., ISBN-13 978-0-471-71998-4, Aug 2005.
4.	Computer Vision: Algorithms and Applications, Richard Szeliski, Springer Verlag, 2013 Edition, ISBN-13: 978-1848829343, ebook : <a href="http://szeliski.org/Book/">http://szeliski.org/Book/</a> .

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<b>CO1</b>	<b>2</b>	<b>1</b>	<b>-</b>	<b>-</b>	<b>2</b>	<b>-</b>	<b>1</b>	<b>1</b>	<b>2</b>	<b>1</b>	<b>-</b>	<b>1</b>
<b>CO2</b>	<b>-</b>	<b>2</b>	<b>-</b>	<b>1</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>1</b>	<b>-</b>	<b>-</b>	<b>2</b>
<b>CO3</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>-</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>2</b>	<b>1</b>	<b>2</b>	<b>-</b>	<b>2</b>
<b>CO4</b>	<b>2</b>	<b>1</b>	<b>2</b>	<b>1</b>	<b>3</b>	<b>2</b>	<b>-</b>	<b>1</b>	<b>-</b>	<b>3</b>	<b>-</b>	<b>2</b>

**High-3: Medium-2: Low-1**

**Semester: VI****DATA STRUCTURES AND ALGORITHMS****(Group C: Professional Core Elective)****(Common to EC and TC)**

<b>Course Code</b>	: 18EC6D3	<b>CIE</b>	: 100 Marks
<b>Credits: L:T:P</b>	: 3:0:0	<b>SEE</b>	: 100 Marks
<b>Total Hours</b>	: 36L	<b>SEE Duration</b>	: 03 Hours

**Course Learning Objectives:** The students will be able to

<b>1</b>	Formulate and apply object-oriented programming, using C++/Java, as a modern tool to solve engineering problems.
<b>2</b>	Demonstrate an understanding of basic data structures (such as an array-based list, linked list, stack, queue, binary search tree) and algorithms.
<b>3</b>	Demonstrate the ability to analyze, design, apply and use data structures and algorithms to solve engineering problems and evaluate their solutions.
<b>4</b>	Demonstrate an understanding of analysis of algorithms. Study an algorithm or program code segment that contains iterative constructs and analyze the asymptotic time complexity of the algorithm or code segment.

**Unit-I****07Hrs****Introduction to data structures:** Introduction to oops concepts. Introduction to data representation, Linear Lists, Linked Representation**Algorithm Analysis:** Mathematical Background, Model, What to Analyze, Running Time Calculations.**Unit – II****08 Hrs****Stack and queue:** Stack and queue implementation using linear list and linked list. Stack application- Parenthesis matching, Queue application-railroad car rearrangement.**Hashing:** Hash table representation- ideal hashing, hashing with linear open addressing, hash tables with chains**Unit –III****07 Hrs****Binary and other Trees:** Trees, Binary Trees, Properties and Representation of Binary Trees-Formula Based Representation, Linked Representation, Common Binary Tree Operations.**Binary Search Tree (BST).** Organizing data in a BST. Inserting and deleting items in a BST.**Unit –IV****07 Hrs****Priority Queues (Heaps):** Model, Simple Implementations, Binary Heap, Leftist Heaps.**Graph Algorithms:**

Definitions, Properties of graphs, Representation of Graphs, Shortest-Path Algorithms, Network Flow Problems, Minimum Spanning Tree, Depth-First Search, Breadth-First Search, Introduction to NP-Completeness

**Unit –V****07 Hrs****Searching and Sorting Techniques:**

Sorting Techniques: Bubble sort, Merge sort, Selection sort, Heap sort, Insertion Sort. Searching Techniques: Sequential Searching, Binary Searching, Search Trees.

**Algorithm Design Techniques:**

Greedy Algorithms, Divide and Conquer, Dynamic Programming, Randomized Algorithms, Backtracking Algorithms

**Course Outcomes: After completing the course, the students will be able to**

<b>CO1:</b>	Acquire the knowledge of importance of data structures in computer programs.
<b>CO2:</b>	Represent and solve data analytics problems using graph algorithms.
<b>CO3:</b>	Implement classic data structures: array lists, linked lists, stacks, queues, heaps, binary trees, hash tables.
<b>CO4:</b>	Evaluate the performance of various algorithms built using different data structures.



Reference Books	
1	Data Structures and Algorithm Analysis in C++ (3rd edition), by M. A. Weiss. Addison-Wesley, ISBN-10: 032144146X & ISBN-13: 9780321441461
2	Sartaj Sahani; "Data structures, Algorithms and applications in c++"; McGraw Hill; 2000;1 <sup>st</sup> Edition; ISBN: 10:007236226X
3	Data Structures Using C++, D.S. Malik, 2 <sup>nd</sup> Edition, 2009, Cengage Learning, ISBN- 13: 978-0-324-78201-1

### Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

### Semester End Evaluation (SEE); Theory (100 Marks)

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

### CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	3	-	-	-	-	-	-		-	-
CO2	3	2	2	3	-	-	-	2	2		-	-
CO3	2	2	3	3	-	-	-	2	2		-	-
CO4	3	3	3	3	2	3	2	3	3	3	2	3

High-3: Medium-2: Low-1

**Semester: VI**

**RADIO FREQUENCY & MILLIMETER WAVE IC DESIGN  
(Group D: Professional Core Elective)**

<b>Course Code</b>	:	18EC6D4	<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:0:0	<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L	<b>SEE Duration</b>	:	03 Hours

**Course Learning Objectives:** The students will be able to

<b>1</b>	Define and demonstrate the importance of radio frequency and millimeter wave IC design.
<b>2</b>	Analyze the functionality and design issues of RF circuits and systems.
<b>3</b>	Design of various circuit blocks in an RF transceiver.
<b>4</b>	Evaluate the different performance parameters used in RF design.

**Unit-I**

**8 Hrs**

**Basic concepts in RF design** - Units in RF design, Nonlinearity and Time Variance, Effects of nonlinearity – harmonic distortion, gain compression – 1 dB compression point, desensitization, blocking, cross modulation, intermodulation – third intercept point, cascaded nonlinear stages – IM spectra in a cascade.

**Noise in RF circuits** - Representation of noise in circuits – input referred noise, Noise figure, Noise figure of cascaded stages, Noise figure of lossy circuits, Sensitivity, dynamic range – spurious free dynamic range (SFDR).

**Unit – II**

**8 Hrs**

**Transceiver architectures** – channel selection and band selection, Heterodyne – constant LO and constant IF downconversion, problem of image, image rejection vs channel selection, dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, issues in homodyne receivers, Image Reject – Hartley & Weaver architecture. Transmitter architectures - Direct conversion and two-step transmitters.

**Review of two port parameters and their significance.**

**Nanoscale MOSFETs** - Parasitic resistances ( $R_s, R_d, R_g$ ), parasitic capacitances ( $C_{gs}, C_{gd}$ ), simplified and extrinsic small-signal models. High-frequency figures of merit:  $f_T$  and  $f_{MAX}$ .

**Unit –III**

**9 Hrs**

**Matching networks** – Passive RLC circuits, impedance transformation – Quality factor, series to parallel conversion, basic matching networks- L, Pi-match networks – design example.

**Low noise Amplifier** - Performance parameters, Problem of Input matching, CS stage with inductive load, Cascode CS stage with inductive degeneration (MOSFET circuits only), Noise figure calculation, Amplifier bandwidth extension techniques, Millimeter Wave LNAs.

**Unit –IV**

**7 Hrs**

**Mixer** - Performance parameters, Mixer noise figures, single balanced and double balanced (active and passive) – working (MOSFET circuits only), Millimeter Wave Mixers.

**Oscillators** - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, three point oscillators, (MOSFET circuits only), Ring oscillators.

**Unit –V**

**7 Hrs**

**Phase Locked Loops** - Basic concepts - Phase detector, Type I PLL, Dynamics of simple PLL, Drawbacks of simple PLL, Type II PLLs - PFD, charge pump, charge pump PLL, PFD/CP Nonidealities (concepts only) – Up and Down Skew and Width Mismatch, Charge Injection and clock feedthrough.

**Course Outcomes: After completing the course, the students will be able to**

<b>CO1:</b>	Investigate the functionality of a typical RF system.
<b>CO2:</b>	Analyze CMOS circuits and its impact on Radio frequency and Millimeter Wave IC design.
<b>CO3:</b>	Design and implement various circuit blocks for RF transceiver chain with specification.
<b>CO4:</b>	Evaluate the different performance parameters used in RF design using CAD tools.

Reference Books	
1	Behzad Razavi, "RF Microelectronics ", 2nd Edition Pearson Education, 2012, ISBN : 13: 9780137134731
2	Thomas H Lee , "The Design of CMOS Radio Frequency Integrated Circuits",2nd Edition, Cambridge University Press, 2004, ISBN : 9780511817281
3	John Rogers ,Calvin Plett, "Radio Frequency Integrated Circuits Design", Artech House, 2003, ISBN : 1-58053-502-x
4	S. Voinigescu, "High-Frequency Integrated Circuits", The Cambridge RF and Microwave Engineering Series, 1 <sup>st</sup> edition, 2013, ISBN : 978-0521873024

### Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

### Semester End Evaluation (SEE); Theory (100 Marks)

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

### CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	2
CO2	3	2	-	-	-	-	-	-	-	-	-	2
CO3	3	3	2	-	2	-	-	3	2	-	-	2
CO4	3	3	-	-	2	-	-	-	-	-	-	2

**High-3: Medium-2: Low-1**

<b>Semester: VI</b>					
<b>Deep Learning</b>					
<b>(Group D: Professional Core Elective)</b>					
<b>Course Code</b>	:	18EC6D5	<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:0:0	<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L	<b>SEE Duration</b>	:	03 Hours
<b>Course Learning Objectives:</b> The students will be able to					
<b>1</b>	Discuss the basic mathematical fundamentals for deep learning				
<b>2</b>	Identify the deep neural network architecture				
<b>3</b>	Appreciate the learning techniques for the deep neural network				
<b>4</b>	Understand the optimization and regularizations techniques.				
<b>5</b>	Analyse the deep learning models using standard models/ libraries				

<b>Unit-I</b>		<b>08 Hrs</b>
Introduction: History of Deep Learning, Deep Learning Success Stories Gradient Descent (GD), Momentum Based GD, Nesterov Accelerated GD, Stochastic GD, AdaGrad, RMSProp, Eigenvalues and eigenvectors, Eigenvalue Decomposition, Basis, Principal Component Analysis and its interpretations, Singular Value Decomposition		
<b>Unit – II</b>		<b>07 Hrs</b>
Autoencoders and relation to PCA, Regularization in autoencoders, Denoising autoencoders, Sparse autoencoders, Contractive autoencoders, Bias Variance Tradeoff, L2 regularization, Early stopping, Dataset augmentation, Parameter sharing and tying, Injecting noise at input, Ensemble methods, Dropout		
<b>Unit –III</b>		<b>07 Hrs</b>
Greedy Layerwise Pre-training, Better activation functions, Better weight initialization methods, Batch Normalization. Convolutional Neural Networks, LeNet, AlexNet, ZF-Net, VGGNet, GoogLeNet, ResNet, Object Detection, RCNN, Fast RCNN, Faster RCNN, YOLO		
<b>Unit –IV</b>		<b>07 Hrs</b>
Recurrent Neural Networks, Backpropagation Through Time (BPTT), Vanishing and Exploding Gradients, Truncated BPTT		
<b>Unit –V</b>		<b>07 Hrs</b>
Gated Recurrent Units (GRUs), Long Short Term Memory (LSTM) Cells, Solving the vanishing gradient problem with LSTMs, Autoregressive Models: NADE, MADE, PixelRNN, Generative Adversarial Networks (GANs)		

<b>Course Outcomes: After completing the course, the students will be able to</b>	
<b>CO1:</b>	Understand the fundamentals of various neural network architecture and training methods
<b>CO2:</b>	Apply the techniques for regularization and optimization of the deep learning networks
<b>CO3:</b>	Appreciate the various models of deep learning networks and its applications
<b>CO4:</b>	Engage in self-study to formulate, design, implement and analyze an application realized on relevant platform.

<b>Reference Books</b>	
<b>1</b>	Goodfellow, I., Bengio, Y., and Courville, A., Deep Learning, MIT Press, 2016. ISBN- 10: 0262035618
<b>2</b>	Bengio, Yoshua. "Learning deep architectures for AI." Foundations and trends in Machine Learning 2.1 (2009) ISBN- 978-3-642-24412-4
<b>3</b>	Bishop, C., Pattern Recognition and Machine Learning, Berlin: Springer-Verlag, 2006. ISBN- 978-0-387-31073-2
<b>4</b>	B. Yegnanarayana, Artificial Neural Networks, Printice Hall India Learning Pvt. Ltd, 2009. ISBN- 13: 978-8120312531

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

**CO-PO Mapping**

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	2
CO2	3	2	-	-	-	-	-	-	-	-	-	2
CO3	3	3	2	-	2	-	-	3	2	-	-	2
CO4	3	3	-	-	2	-	-	-	-	-	-	2

**High-3: Medium-2: Low-1**

**Semester: VI****ALGORITHMS FOR VLSI DESIGN AUTOMATION  
(Group D: Professional Core Elective)**

<b>Course Code</b>	:	18EC6D6	<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:0:0	<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L	<b>SEE Duration</b>	:	03 Hours

**Course Learning Objectives:** The students will be able to

<b>1</b>	Analyze the concept of digital systems, how they can be optimized for area, power and cost, why it is advantageous to use physical design tools.
<b>2</b>	Implement the concept of the physical design cycle and develop algorithms (tools) for each design cycle step.
<b>3</b>	Optimize the digital system at architectural level.
<b>4</b>	Synthesize a given system starting with problem requirements, identifying and designing the building blocks, and then integrating blocks designed earlier

**Unit-I****07 Hrs**

**Scheduling Algorithms:** Introduction, A model for scheduling problems, Scheduling without and with resource constraints, Scheduling algorithms for extended sequencing models, Scheduling pipelined circuits, Resource sharing and binding.

**Unit – II****07 Hrs**

**Data Structure and Basic Algorithms:** Basic Terminology, Graph Search Algorithms, Computational Geometry Algorithms, Basic Data structures. **Partitioning:** Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms

**Unit –III****07Hrs**

**Floor Planning and Pin Assignment:** Problem formulation, classification, Constraint based, Integer programming based, rectangular Dualization, simulated evolution floor planning algorithms. **Placement:** Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms

**Unit –IV****08 Hrs**

**Global Routing: Problem** formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path-based Algorithms, Steiner tree-based Algorithms **Detailed Routing:** Problem formulation, Classification single Layer routing, General river routing, Single row routing

**Unit –V****07 Hrs**

**Channel, Clock and Power Routing:** Two-layer channel routing Algorithms, Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms, Introduction to compaction, shadow propagation algorithm.

**Course Outcomes: After completing the course, the students will be able to**

<b>CO1:</b>	Analyze each stage of VLSI design flow to develop a CAD tool for physical design.
<b>CO2:</b>	Apply design knowledge to develop algorithms for VLSI design automation.
<b>CO3:</b>	Evaluate the algorithms for optimizing VLSI design with respect to speed, power and area.
<b>CO4:</b>	Create an optimized VLSI IC design technique using various algorithms.

**Reference Books**

1	Synthesis and Optimization of Digital Circuit, 1994, Giovanni De Micheli, McGraw- Hill, ISBN: 10-0070163332
2	Algorithms for VLSI Physical Design Automation, N.A. Sherwani, 2002, Kluwar Academic Publishers, ISBN: 0-7923-8393-1
3	An Introduction to VLSI Physical Design, M Sarraf Zadeh, C K Wong, 1996, McGraw Hill, ISBN:0070571945
4	Algorithms for VLSI Design Automation , S.H. Gerez, 1998, John Wiley & Sons, ISBN: 978-0-471-98489-4

**Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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**Semester End Evaluation (SEE); Theory (100 Marks)**

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

**CO-PO Mapping**

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CO2	3	2	3	1	3	-	1	1	2	2	3	3
CO3	3	2	3	3	3	1	-	-	1	1	3	3
CO4	3	3	3	1	3	-	-	1	2	1	1	3

**High-3: Medium-2: Low-1**

**Semester: VI****Wearable Electronics  
(Group E: Global Elective)**

<b>Course Code</b>	:	18G6E05	<b>CIE</b>	:	100 Marks
<b>Credits: L:T:P</b>	:	3:0:0	<b>SEE</b>	:	100 Marks
<b>Total Hours</b>	:	36L	<b>SEE Duration</b>	:	03 Hours

**Course Learning Objectives:** The students will be able to

<b>1</b>	Explain the types and application of wearable sensor.
<b>2</b>	Describe the working of sensitivity, conductivity and energy generation in wearable devices.
<b>3</b>	Explain the various facets of wearable application, advantage & challenges.
<b>4</b>	Understand different testing and calibration in wearable devices.

**Unit-I****08 Hrs**

**Introduction:** world of wearable (WOW), Role of wearable, The Emerging Concept of Big Data, The Ecosystem Enabling Digital Life, Smart Mobile Communication Devices, Attributes of Wearables, Taxonomy for Wearables, Advancements in Wearables, Textiles and Clothing, Applications of Wearables. [Ref 1: Chapter 1.1]

**Unit – II****08 Hrs**

**Wearable Bio and Chemical Sensors:** Introduction, System Design, Microneedle Technology, Sampling Gases, Types of Sensors, Challenges in Chemical Biochemical Sensing, Sensor Stability, Interface with the Body, Textile Integration, Power Requirements, Applications: Personal Health, Sports Performance, Safety and Security, Case studies. [Ref 1: Chapter 2.1]

**Unit –III****07 Hrs**

**Smart Textile:** Conductive fibres for electronic textiles: an overview, Types of conductive fibre, Applications of conductive fibres, Bulk conductive polymer yarn, Bulk conductive polymer yarn, Techniques for processing CPYs, Wet-spinning technique, Electrospinning technique, case studies, Hands on project in wearable textile: Solar Backpack, LED Matrix wallet. [Ref 2: Chapter 1,2] & [Ref 3: Chapter 6,9]

**Unit –IV****08 Hrs**

**Energy Harvesting Systems:** Introduction, Energy Harvesting from Temperature Gradient, Thermoelectric Generators, Dc-Dc Converter Topologies, Dc-Dc Converter Design for Ultra-Low Input Voltages, Energy Harvesting from Foot Motion, Ac-Dc Converters, Wireless Energy Transmission, Energy Harvesting from Light, Case studies. [Ref 1: Chapter 4.1]

**Unit –V****08 Hrs**

**Wearable antennas for communication systems:** Introduction, Background of textile antennas, Design rules for embroidered antennas, Integration of embroidered textile surfaces onto polymer substrates, Characterizations of embroidered conductive, textiles at radio frequencies, RF performance of embroidered textile antennas, Applications of embroidered antennas. [Ref 2: Chapter 10]

**Course Outcomes: After completing the course, the students will be able to**

<b>CO1:</b>	Describe the different types and wearable sensors, textile, energy harvesting systems and antenna
<b>CO2:</b>	Analysis measurable quantity and working of wearable electronic devices.
<b>CO3:</b>	Determine & interpret the outcome of the wearable devices and solve the design challenges
<b>CO4:</b>	Analyse and Evaluate the wearable device output parameter in real time scenario or given problem statement.



Reference Books	
1	Wearable Sensors: Fundamentals, Implementation and Applications, Edward Sazonov, Michael R. Neuman Academic Press, 1 <sup>st</sup> Edition, 2014, ISBN-13: 978-0124186620.
2	Electronic Textiles: Smart Fabrics and Wearable Technology, Tilak Dias, Woodhead Publishing; 1 edition, ISBN-13: 978-0081002018.
3	Make It, Wear It: Wearable Electronics for Makers, Crafters, and Cosplayers, McGraw-Hill Education, 1st Edition, ISBN-13: 978-1260116151.
4	Flexible and Wearable Electronics for Smart Clothing: Aimed to Smart Clothing, Gang Wang, Chengyi Hou, Hongzhi Wang, Wiley, 1st Edition, ISBN-13: 978-3527345342
5	Printed Batteries: Materials, Technologies and Applications, Senentxu Lanceros-Méndez, Carlos Miguel Costa, Wiley, 1 edition, ISBN-13: 978-1119287421

#### Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and Experiential Learning (EL). A minimum of three quizzes are conducted and each quiz is evaluated for 10 marks adding up to 30 marks. All quizzes are conducted online. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three also. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50. The marks component for experiential learning is 20. **Total CIE is 30(Q) +50(T) +20(EL) =100 Marks.**

#### Semester End Evaluation (SEE); Theory (100 Marks)

SEE for 100 marks is executed by means of an examination. The Question paper for the course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the complete syllabus. Part – B consists of five main questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have sub questions. The question from Units I, IV and V have no internal choice. Units II and III have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

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CO3	2	2	3	3	-	-	-	2	2		-	-
CO4	3	3	3	3	2	3	2	3	3	3	2	3

High-3: Medium-2: Low-1

## VI Semester

## Professional Practice – II

## Employability Skills and Professional Development of Engineers

<b>Course Code</b>	:	18HSE68	<b>CIE Marks</b>	:	50 Marks
<b>Credits: L:T:P</b>	:	0:0:1	<b>SEE Marks</b>	:	50 Marks
<b>Hours</b>	:	18 L	<b>CIE Duration</b>	:	02 Hrs

**Course Learning Objectives: The students will be able to**

<b>1</b>	Improve qualitative and quantitative problem solving skills.
<b>2</b>	Apply critical and logical thinking process to specific problems.
<b>3</b>	Ability to verbally compare and contrast words and arrive at relationships between concepts, based on verbal reasoning.
<b>4</b>	Applying good mind maps that help in communicating ideas as well as in technical documentation

**UNIT-I****06 Hrs**

Aptitude Test Preparation- Importance of Aptitude tests, Key Components, Quantitative Aptitude – Problem Solving, Data Sufficiency, Data Analysis - Number Systems, Math Vocabulary, fraction decimals, digit places etc. Reasoning and Logical Aptitude, - Introduction to puzzle and games organizing information, parts of an argument, common flaws, arguments and assumptions. Analytical Reasoning, Critical Reasoning.

**UNIT-II****06 Hrs**

Verbal Analogies - What are Analogies, How to Solve Verbal Analogies & developing Higher Vocabulary, Grammar, Comprehension and Application, Written Ability. Non- Verbal Reasoning, Brain Teasers. Creativity Aptitude. Group Discussion- Theory & Evaluation : Understanding why and how is the group discussion conducted, The techniques of group discussion, Discuss the FAQs of group discussion, body language during GD.

**UNIT-III.A****06 Hrs**

Resume Writing- Writing Resume, how to write effective resume, Understanding the basic essentials for a resume, Resume writing tips Guidelines for better presentation of facts.

**UNIT-III.B****06 Hrs**

**Technical Documentation** - Introduction to technical writing- Emphasis on language difference between general and technical writing, Contents in a technical document, Report design overview & format Headings, list & special notes, Writing processes, Translating technical information, Power revision techniques, Patterns & elements of sentences, Common grammar, usage & punctuation problems.

**UNIT-IV****06 Hrs**

Interview Skills -a) Personal Interviews , b) Group Interviews , c) Mock Interviews - Questions asked & how to handle them, Body language in interview, Etiquette, Dress code in interview, Behavioral and technical interviews, Mock interviews - Mock interviews with different Panels. Practice on stress interviews, technical interviews, General HR interviews etc.

**UNIT-V****06 Hrs**

Interpersonal Relations - Optimal Co-existence, Cultural Sensitivity, Gender sensitivity Adapting to the Corporate Culture- Capability & Maturity Model, Decision Making Analysis, Brain Storm. Adapting to the Corporate Culture.

**Course Outcomes: After completing the course, the students will be able to**

CO1:	Inculcate employability skill to suit the industry requirement.
CO2:	Analyze problems using quantitative and reasoning skills
CO3:	Exhibit verbal aptitude skills with appropriate comprehension and application.
CO4:	Focus on Personal Strengths and Competent to face interviews and answer

**Reference Books**

<b>1.</b>	The 7 Habits of Highly Effective People, Stephen R Covey Free Press, 2004 Edition, ISBN: 0743272455
<b>2.</b>	How to win friends and influence people, Dale Carnegie General Press, 1 <sup>st</sup> Edition, 2016, ISBN: 9789380914787

3.	Crucial Conversation: Tools for Talking When Stakes are High, Kerry Patterson, Joseph Grenny, Ron Mcmillan 2012 Edition, McGraw-Hill Publication ISBN: 9780071772204
4.	Ethnus, Aptimithra: Best Aptitude Book ,2014 Edition, Tata McGraw Hill ISBN: 9781259058738

**Scheme of Continuous Internal Examination and Semester End Examination**

Phase	Activity	Weightage
Phase I V Sem	CIE will be conducted during the 5 <sup>th</sup> semester and evaluated for 50 marks. The test will have two components. The Quiz is evaluated for 15 marks and second component consisting of questions requiring descriptive answers is evaluated for 35 marks. The test & quiz will assess the skills acquired through the training module. SEE is based on the test conducted at the end of the 5 <sup>th</sup> semester The test will have two components a Quiz evaluated for 15 marks and second component consisting of questions requiring descriptive answers is evaluated for 35 marks.	50%
Phase II VI Sem	During the 6 <sup>th</sup> semester a test will be conducted and evaluated for 50 marks. The test will have two components a Short Quiz and Questions requiring descriptive answers. The test & quiz will assess the skills acquired through the training module. SEE is based on the test conducted at the end of the 6 <sup>th</sup> semester The test will have two components. The Quiz evaluated for 15 marks and second component consisting of questions requiring descriptive answers is evaluated for 35 marks	50%
Phase III At the end of VI Sem	At the end of the VI Sem Marks of CIE (5 <sup>th</sup> Sem and 6 <sup>th</sup> Sem) is consolidated for 50 marks (Average of Test1 and Test 2 (CIE 1+CIE2)/2). At the end of the VI Sem Marks of SEE (5 <sup>th</sup> Sem and 6 <sup>th</sup> Sem) is consolidated for 50 marks (Average of CIE 1 and CIE 2 (CIE 1+CIE2)/2).	