



# RV COLLEGE OF ENGINEERING<sup>®</sup>

(Autonomous Institution Affiliated to VTU, Belagavi)

R.V. Vidyaniketan Post, Mysore Road

Bengaluru – 560 059



**Scheme and Syllabus of I & II Semesters**  
(Autonomous System of 2018 Scheme)

**Master of Technology (M.Tech)**

**in**

**VLSI DESIGN & EMBEDDED  
SYSTEMS**

**DEPARTMENT OF  
ELECTRONICS &  
COMMUNICATION ENGINEERING**

**INNER FRONT COVER PAGE**

**College Vision & Mission  
(To be included from our side)**

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**COMMUNICATION ENGINEERING**

# Department Vision & Mission

## VISION

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering

## MISSION

- To impart quality technical education to produce industry-ready engineers with a research outlook.
- To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.
- To create centers of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.
- To develop entrepreneurial skills among the graduates to create new employment opportunities

**ABBREVIATIONS**

Sl. No.	Abbreviation	Meaning
1.	VTU	Visvesvaraya Technological University
2.	BS	Basic Sciences
3.	CIE	Continuous Internal Evaluation
4.	SEE	Semester End Examination
5.	CE	Professional Core Elective
6.	GE	Global Elective
7.	HSS	Humanities and Social Sciences
8.	CV	Civil Engineering
9.	ME	Mechanical Engineering
10.	EE	Electrical & Electronics Engineering
11.	EC	Electronics & Communication Engineering
12.	IM	Industrial Engineering & Management
13.	EI	Electronics & Instrumentation Engineering
14.	CH	Chemical Engineering
15.	CS	Computer Science & Engineering
16.	TE	Telecommunication Engineering
17.	IS	Information Science & Engineering
18.	BT	Biotechnology
19.	AS	Aerospace Engineering
20.	PHY	Physics
21.	CHY	Chemistry
22.	MAT	Mathematics

**INDEX**

<b>I Semester</b>			
Sl. No.	Course Code	Course Title	Page No.
1.	18MVE11	Digital System Design using Verilog	9
2.	18MVE12	Advanced Embedded System Design	11
3.	18MVE13	Digital IC Design	14
4.	18HSS14	Professional Skill Development	16
5.	18MVE1AX	Elective – A	18 – 23
6.	18MVE1BX	Elective – B	24 – 29
<b>GROUP A: CORE ELECTIVES</b>			
1.	18MVE1A1	Advanced Computer Architecture	18
2.	18MVE1A2	ASIC Design	20
3.	18MVE1A3	Algorithms for VLSI Design	22
<b>GROUP B: CORE ELECTIVES</b>			
1.	18MVE1B1	MEMS and Smart Systems	24
2.	18MVE1B2	System On Chip Design	26
3.	18MVE1B3	Advanced VLSI Devices	28

<b>II Semester</b>			
<b>Sl. No.</b>	<b>Course Code</b>	<b>Course Title</b>	<b>Page No.</b>
1.	18MVE21	Analog IC Design	30
2.	18MVE22	System Verilog for Design & Verification	32
3.	18IM23	Research Methodology	34
4.	18MVE24	Minor Project	36
5.	18MVE2CX	Elective – C	37 – 42
6.	18MVE2DX	Elective – D	43 – 47
7.	18XX2GX	Global Elective	49 – 68
<b>GROUP C: CORE ELECTIVES</b>			
1.	18MVE2C1	VLSI Testing	37
2.	18MCS2C2	Machine Learning	39
3.	18MVE2C3	High speed VLSI Design	41
<b>GROUP D: CORE ELECTIVES</b>			
1.	18MVE2D1	Low Power VLSI Design	43
2.	18MVE2D2	Advanced Embedded Processors	45
3.	18MVE2D3	VLSI Digital Signal Processing Systems	47
<b>GROUP G: GLOBAL ELECTIVES</b>			
1.	18CS2G01	Business Analytics	49
2.	18CV2G02	Industrial & Occupational Health and Safety	51
3.	18IM2G03	Modeling using Linear Programming	53
4.	18IM2G04	Project Management	55
5.	18CH2G05	Energy Management	57
6.	18ME2G06	Industry 4.0	59
7.	18ME2G07	Advanced Materials	61
8.	18CHY2G08	Composite Materials Science and Engineering	63
9.	18PHY2G09	Physics of Materials	65
10.	18MAT2G10	Advanced Statistical Methods	67

**R V COLLEGE OF ENGINEERING, BENGALURU-560 059**  
 (Autonomous Institution Affiliated to VTU, Belagavi)  
**DEPARTMENT OF ELECTRONICS &**  
**COMMUNICATION ENGINEERING**  
**M.Tech in VLSI DESIGN & EMBEDDED SYSTEMS**

<b>FIRST SEMESTER CREDIT SCHEME</b>							
Sl. No.	Course Code	Course Title	BoS	Credit Allocation			
				L	T	P	Total Credits
1	18MVE11	Digital System Design using Verilog	EC	4	0	0	4
2	18MVE12	Advanced Embedded System Design	EC	3	1	1	5
3	18MVE13	Digital IC Design	EC	3	1	1	5
4	18HSS14	Professional Skill Development	HSS	0	0	0	0
5	18MVE1AX	Elective – A	EC	4	0	0	4
6	18MVE1BX	Elective – B	EC	4	0	0	4
<b>Total number of Credits</b>				18	2	2	22
<b>Total Number of Hours / Week</b>				18	4	6	28

<b>SECOND SEMESTER CREDIT SCHEME</b>							
Sl. No.	Course Code	Course Title	BoS	Credit Allocation			
				L	T	P	Total Credits
1	18MVE21	Analog IC Design	EC	3	1	1	5
2	18MVE22	System Verilog for Design & Verification	EC	3	1	0	4
3	18IM23	Research Methodology	IM	3	0	0	3
4	18MVE24	Minor Project	EC	0	0	2	2
5	18MVE2C X	Elective – C	EC	4	0	0	4
6	18MVE2D X	Elective – D	EC	4	0	0	4
7	18XX2GX	Global Elective	Respective boards	3	0	0	3
<b>Total number of Credits</b>				20	2	3	25
<b>Total Number of Hours / Week</b>				20	4	9	33

<b>I Semester</b>		
<b>GROUP A: CORE ELECTIVES</b>		
<b>Sl. No.</b>	<b>Course Code</b>	<b>Course Title</b>
1.	18MVE1A1	Advanced Computer Architecture
2.	18MVE1A2	ASIC Design
3.	18MVE1A3	Algorithms for VLSI Design
<b>GROUP B: CORE ELECTIVES</b>		
1.	18MVE1B1	MEMS and Smart Systems
2.	18MVE1B2	System On Chip Design
3.	18MVE1B3	Advanced VLSI Devices
<b>II Semester</b>		
<b>GROUP C: CORE ELECTIVES</b>		
1.	18MVE2C1	VLSI Testing
2.	18MCS2C2	Machine Learning
3.	18MVE2C3	High speed VLSI Design
<b>GROUP D: CORE ELECTIVES</b>		
1.	18MVE2D1	Low Power VLSI Design
2.	18MVE2D2	Advanced Embedded Processors
3.	18MVE2D3	VLSI Digital Signal Processing Systems

<b>GROUP E: GLOBAL ELECTIVES</b>				
<b>Sl. No.</b>	<b>Host Dept</b>	<b>Course Code</b>	<b>Course Title</b>	<b>Credits</b>
1.	CS	18CS2G01	Business Analytics	3
2.	CV	18CV2G02	Industrial & Occupational Health and Safety	3
3.	IM	18IM2G03	Modelling using Linear Programming	3
4.	IM	18IM2G04	Project Management	3
5.	CH	18CH2G05	Energy Management	3
6.	ME	18ME2G06	Industry 4.0	3
7.	ME	18ME2G07	Advanced Materials	3
8.	CHY	18CHY2G08	Composite Materials Science and Engineering	3
9.	PHY	18PHY2G09	Physics of Materials	3
10.	MAT	18MAT2G10	Advanced Statistical Methods	3



<b>Semester I</b>				
<b>DIGITAL SYSTEM DESIGN USING VERILOG</b>				
<b>Course Code</b>	:	<b>18MVE11</b>	<b>CIE Marks</b>	: <b>100</b>
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>	<b>SEE Marks</b>	: <b>100</b>
<b>Hrs</b>	:	<b>48L</b>	<b>SEE Duration</b>	: <b>3 Hrs</b>
<b>Unit – I</b>				<b>10 Hrs</b>
<p><b>Introduction to Verilog and Design Methodology:</b>  <b>Introduction to Verilog:</b> Verilog IEEE standards, Application Areas and Abstraction levels, Need of verification of HDL design, Simulation and Synthesis, Test-benches,  Verilog Data Types: Net, Register and Constant. Verilog Operators: Logical, Arithmetic, Bitwise, Reduction, Relational, Concatenation and Conditional, Number representation and Verilog ports.  <b>Verilog Primitives. Logic Simulation, Design Verification, and Test Methodology:</b> Four-Value Logic and Signal Resolution in Verilog, Test Methodology Signal Generators for Test benches, Event-Driven Simulation, Sized Numbers. Propagation Delay.  <b>Introduction to Design Methodology:</b>  Digital Systems and Embedded Systems, Real-world circuits. Design Methodology: Design Flow-Architecture, Functional design and verification, Synthesis, Physical design. Design Optimization-Area, Timing and Power, System representation.</p>				
<b>Unit – II</b>				<b>10 Hrs</b>
<p><b>Number Basics and Verilog Modelling Styles:</b>  <b>Number Basics:</b> Unsigned and Signed Integers, Fixed-point and Floating-point Numbers. Boolean Functions and Boolean Algebra, Verilog models for Boolean switching function, Binary Coding.  <b>Behavioural Modelling:</b> Latches and Level-Sensitive Circuits in Verilog, Cyclic Behavioural Models of Flip-Flops and Latches, Cyclic Behaviour and Edge Detection. A Comparison of Styles for Behavioural modelling, Behavioural Models of Multiplexers, Encoders, Decoders and Arithmetic circuits.  <b>Dataflow Modelling:</b> Boolean Equation-Based Models of Combinational Logic, Propagation Delay and Continuous Assignments. Dataflow Models of a Linear-Feedback Shift Register. Modelling Digital Machines with Repetitive Algorithms Machines with Multicycle Operations. Tasks &amp; Functions.  <b>Structural Modelling:</b> Design of Combinational Logic, Verilog Structural Models, Module Ports, Top-Down Design and Nested Modules. Gate level modelling.</p>				
<b>Unit – III</b>				<b>10 Hrs</b>
<p><b>Synthesis of Digital Sub-systems:</b>  <b>Synthesis of Combinational Sub-systems:</b> Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Three-state Devices and Bus Interfaces.  <b>Synthesis of Sequential Sub-systems:</b> Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines, Registered Logic, State Encoding, Synthesis of Implicit State Machines, Registers and Counters.</p>				
<b>Unit – IV</b>				<b>9 Hrs</b>
<p><b>System Implementation Fabrics and Accelerators:</b> Introduction of Programmable Logic Array (PLA), Programmable Array Logic (PAL), Programmability of PLDs. Complex PLDs (CPLDs), Field-Programmable Gate Arrays (Artix-7 and Virtex-5) The Role of FPGAs in the ASIC Market, FPGA Technologies. Verilog-Based Design Flows for FPGAs and ASICs. Comparison of design implementation using CPLDs, FPGA and ASIC.  <b>System Accelerators:</b> Concepts, Case study: Video Edge detection, Verification of accelerators.  <b>User-Defined Primitives:</b> Combinational Primitives: Basic Features of User-Defined Primitives, Describing Combinational Logic Circuits. Sequential Primitives: Level-Sensitive Primitives, Edge-Sensitive Primitives.</p>				
<b>Unit – V</b>				<b>9 Hrs</b>
<p><b>Processor Design and System Development:</b>  <b>Design of Processor Architectures:</b> Functional Units for Addition, Subtraction and Multiplication (overview). Design: Hierarchical Decomposition STG-Based Controller Design, Efficient STG-Based</p>				

Sequential Binary Multiplier. <b>Interfacing Concepts:</b> Embedded Computer Organization, Instruction and Data, Memory Interfacing. I/O Interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission.	
<b>Course Outcomes:</b> After taking up this course, the student will be able to: CO1: Understand the digital system designs skills using VERILOG HDL based on IEEE-1364 standards and managed by Open Verilog International (OVI). CO2: Demonstrate the skill on cost-effective system designs through proper selection of implementation fabrics for the desired application. CO3: Analyze complete systems and build small scale applications using Interfacing concepts. CO4: Design and implement complete digital systems using VERILOG HDL and demonstrate the innovation skills.	
<b>Reference Books:</b>	
1.	Michael D. Ciletti, “Advanced Digital Design With the Verilog HDL,” 2E, PHI, ISBN: 978-0-07-338054-4 2015.
2.	Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using VERILOG”, Elsevier, ISBN: 978-0-12-369527-7, 2010.
3.	Charles Roth, Lizy K. John, Byeong Kil Lee, “Digital Systems Design Using Verilog,” Cengage Learning, ISBN-10: 1285051076, 2015.
4.	Stephen Brown and Zvonko Vranesic, “Fundamentals of Digital Logic with Verilog Design,” 6E, McGraw Hill publication, ISBN: 978-0-07-338054-4, 2014.
5.	J. Bhasker, “Verilog HDL Synthesis - A Practical Primer,” Star Galaxy Publishing, ISBN: 0-9650391-5-3, 1998.

**Continuous Internal Evaluation (CIE): Total marks: 100****Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100****Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester I</b>					
<b>ADVANCED EMBEDDED SYSTEM DESIGN (Theory and Practice)</b>					
<b>Course Code</b>	<b>:</b>	<b>18MVE12</b>		<b>CIE Marks</b>	<b>:</b> 100 + 50
<b>Credits : L:T:P</b>	<b>:</b>	<b>3:1:1</b>		<b>SEE Marks</b>	<b>:</b> 100 + 50
<b>Hrs</b>	<b>:</b>	<b>48L +36 P</b>		<b>SEE Duration</b>	<b>:</b> 3 Hrs +3 Hrs
<b>Unit – I</b>					<b>10 Hrs</b>
<b>Introduction to Embedded System Design</b>					
Introduction, Characteristics of Embedding Computing Applications, Concept of Real time Systems, Challenges in Embedded System Design, Design Process: Requirements, Specifications, Hardware Software Partitioning, Architecture Design, Designing of Components, System Integration					
<b>Embedded System Architecture</b>					
Instruction Set Architectures with examples, Memory system Architecture: Von Neumann, Harvard, caches, Virtual Memory, Memory Management, I/O sub system: Busy wait I/O,DMA, Interrupt Driven I/O, Co-Processor & Hardware Accelerators, Processor performance Enhancement: Pipelining, Superscalar Execution, Multi Core CPUs, CPU Power Consumption, Benchmarking Standards: MIPS, MFLOPS, MMACS, Coremark					
<b>Unit – II</b>					<b>10 Hrs</b>
<b>Designing Embedded System Hardware –I</b>					
CPU Bus: Bus Protocols, Bus Organisation, Memory Devices and their Characteristics: RAM, EEPROM, Flash Memory, DRAM; I/O Devices: Timers and Counters, Watchdog Timers, Interrupt, Controllers, DMA Controllers, A/D and D/A Converters, Displays, Keyboards, Infrared devices					
<b>Unit – III</b>					<b>10 Hrs</b>
<b>Designing Embedded System Hardware –II</b>					
Component Interfacing: Memory interfacing with case study; I/O Device Interfacing with case Study: Programmed IO, Memory Mapped IO, Interfacing Protocols: SPI, I2C, CAN, USB, Reset Circuits, Designing with Processors: System Architecture, FPGA based Design, Processor Selection Criteria					
<b>Unit – IV</b>					<b>9 Hrs</b>
<b>Designing Embedded System Software –I</b>					
Application Software, System Software, Use of High Level Languages: C,C++,Java, Programming & Integrated Development Environment tools: Editor, Compiler, Linker, Automatic Code Generators, Debugger, Board Support Library, Chip Support Library, Analysis and Optimization: Execution Time, Energy & Power, Program Size; Program Validation & Verification, Embedded System Coding Standards: MISRA C 2012/CERT, Standards in Automobiles, Aerospace &Biomedical Applications.					
<b>Unit – V</b>					<b>9 Hrs</b>
<b>Designing Embedded System Software –II</b>					
OS based Design, Real Time Kernel, Process& Thread, Inter Process Communications, Synchronization, Case Study: RTX-ARM, Evaluating and Optimising Operating System Performance: Response time Calculation, Interrupt Latency, Time Loading, Memory Loading, Case Study: Embedded Control Applications-Software Coding of a PID Controller, PID Tuning, IoT based Resource Monitoring					
<b>LAB COMPONENT</b>					
<b>Experiments on bare metal programming</b>					
1. Write application program to interface LEDs and push buttons to GPIOs of LPC 1857 cortex M3 evaluation board and demonstrate polling-based IO operation.					
2. Write SysTick_handler to accurately control the delay between toggling of LEDs to support interrupt driven IO.					
3. Write driver for ADC0 in LPC 1857 MCU. Display digital value on GLCD and demonstrate analog sensor interface. Write driver functions for ADC initialization, ADC start of conversion, reading digital value output. Develop main function using APIs of ADC driver to test the functionality.					
4. Write I2C driver for LPC1857. Develop following APIs to support I2C.					

```

uint32_t I2C_Init (void);
uint32_t I2C_Start (void);
uint32_t I2C_Stop (void);
uint32_t I2C_Addr (uint8_t adr, uint8_t dir);
uint32_t I2C_Write (uint8_t byte);
uint32_t I2C_Read (uint32_t ack, uint8_t *byte);

```

5. Write driver to support LM75a digital temperature sensor through I2C. Make use of APIs developed in experiment 4 to interface LM75a to LPC 1857 MCU. Test the functionality by displaying temperature values on GLCD.

6. Write application program to realize FIR filter on STM32F4 cortex M4 development board. Test the filtering operation on signal generated from function generator and interfaced to STM32F4 development board through WolfsonPI codec.

### Experiments using RTOS

1. Create a multitasking application program to demonstrate creation of tasks. Task1 is expected to control the blinking two LEDs and Task2 is to change font and colour of the textual display on GLCD concurrently. Use APIs of RL-RTX/Freertos real time kernel. Configure systick timer to generate tick interval.

2. Create multitasking program to demonstrate task synchronization. Task1 is expected to display LED blinking pattern and Task2 display textual message on GLCD. Synchronize the access of GLD using mutex/semaphore using APIs of RL-RTX/Freertos.

3. Create a multitasking program to demonstrate event flags to synchronize task execution. Create four tasks to simulate the operation of stepper motor driver. Use four LEDs blinking to simulate the activation of the four output driver stages. Create another concurrently executing task to display text on GLCD. The stepper motor driver tasks are expected to run sequentially.

4. Create multitasking program to demonstrate IPC using mailbox. Create a task to read a digital value from ADC and send to another task executing concurrently through mailbox. Synchronize the execution of tasks. Use APIs of RL-ARM/Freertos real time kernel.

5. Create a ‘Blinky’ project using RL-ARM real time Kernel to simulate the operations of step-motor driver. Use four LEDs blinking to simulate the activation of the four output driver stages. Create other two tasks executing concurrently and competing for GLCD. The first task displays status of LEDs blinking on GLCD and second task displays a string with changing colour of font and background. Use suitable mechanism to protect shared resource.

### Expected Course Outcomes:

After going through this course the student will be able to:

CO1: Describe hardware & software of an embedded systems for real time applications with suitable processor architecture, memory and communication interface.

CO2: Design embedded software & hardware to meet given constraints with the help of modern engineering tools.

CO3: Demonstrate compliance of prescribed safety norms through implementation of the identified engineering problems pertaining to automobiles, aerospace & biomedical applications.

CO4: Engage in self study to design, implement and demonstrate open ended problem

### Reference Books:

1.	James K Peckol, “Embedded Systems – A contemporary Design Tool”, John Wiley, 2008, ISBN: 0-444-51616-6
2.	Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2009, ISBN: 10: 0070678790
3.	David E.Simon, “Embedded Software Primer”, Addison Wesley, ISBN-13: 978-0201615692
4.	Barry B.Brey, “The Intel Micro-processors, Architecture, Programming and Interfacing”, 6 <sup>th</sup> Edition,

	Pearson Education.
5.	Steve Heath, “Embedded System Design”, Elsevier, 2nd Edition, 2004.
6.	Reference Manuals: RTX-ARM, MISRA C 2012, CERT, IS26262, DO-178B, IEC 62304

**Continuous Internal Evaluation (CIE): Total marks: 100+50=150**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Scheme of Continuous Internal Evaluation (CIE) for Practicals: ( 50 Marks)**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

**Semester End Evaluation (SEE): Total marks: 100+50=150**

**Theory (100 Marks) + Practical (50 Marks) = Total Marks (150)**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

**Scheme of Semester End Examination (SEE); Practical (50 Marks)**

SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

<b>Semester I</b>						
<b>DIGITAL IC DESIGN (Theory and Practice)</b>						
<b>Course Code</b>	:	<b>18MVE13</b>		<b>CIE Marks</b>	:	100+50
<b>Credits : L:T:P</b>	:	<b>3:1:1</b>		<b>SEE Marks</b>	:	100+50
<b>Hrs</b>	:	<b>48L+36P</b>		<b>SEE Duration</b>	:	<b>3 Hrs + 3 Hrs</b>
<b>Unit – I</b>						<b>10 Hrs</b>
<p><b>Introduction:</b> Issues in Digital IC Design, Design abstraction levels in digital circuits, Quality Metrics of a Digital Design</p> <p><b>MOS Transistor:</b> Device structure, MOSFET- static &amp; dynamic behavior, secondary effects, technology scaling</p> <p><b>Implementation strategies for Digital ICs:</b> Digital circuit implementation approaches- overview Custom circuit design, cell based design methodology, semicustom design flow.</p>						
<b>Unit – II</b>						<b>10 Hrs</b>
<p><b>CMOS inverter:</b> Static CMOS Inverter: static and dynamic Behavior, Components of Energy and Power</p> <p><b>CMOS Combinational Logic Circuit Design:</b> Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic. Dynamic CMOS Design: Dynamic Logic Design Considerations. Speed and Power Dissipation of Dynamic logic, Signal integrity issues, Cascading Dynamic gates.</p>						
<b>Unit – III</b>						<b>10 Hrs</b>
<p><b>CMOS Sequential Logic Circuit Design:</b> Static Latches and Registers. Dynamic Latches and Registers. Pulse Based Registers. Sense Amplifier based registers. Pipelining concepts.</p> <p><b>Memory &amp; Array structures design:</b> Memory core – ROM, SRAM, DRAM, Sense amplifiers, CAM</p>						
<b>Unit – IV</b>						<b>9 Hrs</b>
<p><b>Interconnects:</b> Resistive, Capacitive and Inductive Parasitics (basics)</p> <p><b>Timing Issues:</b> Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and Impact on Performance. Clock Distribution techniques, Latch based clocking.</p>						
<b>Unit – V</b>						<b>9 Hrs</b>
<p><b>Arithmetic building blocks design:</b> Data paths in digital processor architectures – Adder, binary adder, static adder, mirror adder, TG based adder, carry bypass adder, linear and square root carry select adder, carry lookahead adder, Multiplier- array, carry save multiplier</p> <p><b>Manufacturing CMOS Integrated Circuits:</b> Silicon wafer, Photolithography, Process steps, CMOS process flow.</p>						
<b>Lab Component</b>						<b>30 Hrs</b>
<ol style="list-style-type: none"> <li>1. Introduction to Cadence environment; setup Linux environment; create schematic and symbol, introduction to netlist, technology library.</li> <li>2. Inverter static characteristics</li> <li>3. Inverter dynamic characteristics</li> <li>4. Design and Analysis of NAND, NOR and complex gates</li> <li>5. Layout, DRC, LVS, RCX and post-layout simulation of CMOS Inverter</li> <li>6. Layout of CMOS NAND, NOR Inverter static characteristics</li> <li>7. LEF file generation</li> <li>8. LIB file generation</li> <li>9. Synthesis of combinational logics</li> <li>10. Case study: Synthesis of serial adder and PAR using Encounter tool.</li> </ol>						

**Expected Course Outcomes:**

After taking up this course, the graduate will be able to:

CO1: Investigate device, circuit & system aspects of digital IC design

CO2: Analyze the functionality of digital integrated circuits & systems

CO3: Design and implement digital integrated circuit & systems

CO4: Evaluate the different performance parameters of a digital integrated circuits & systems

**Reference Books:**

1.	Jan M.Rabaey, Anantha Chadrakasan, Borivoje Nikolic, “Digital Integrated Circuits: A Design Perspective”, (2/e), Pearson 2016, ISBN-13: 978-0130909961
2.	Erik Brunvand, “Digital VLSI Chip Design with Cadence and Synopsys CAD Tools”, Pearson 2009, ISBN-13: 9780321547743
3.	David A Hodges, Horace G Jackson and Resve A Saleh, “Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology” TMH.2005, ISBN-13: 978-0072283655
4.	Sung MO Kang, Yousuf Leblebici, “CMOS Digital Integrated Circuits”; Tata McGrawHill, (3/e), ISBN: 0-7923-7246-8
5.	Neil H.E. Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design”, Pearson Education, (3/e), 2006, ISBN: 0321149017

**Continuous Internal Evaluation (CIE): Total marks: 100+50=150**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Scheme of Continuous Internal Evaluation (CIE) for Practicals: ( 50 Marks)**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

**Semester End Evaluation (SEE): Total marks: 100+50=150**

**Theory (100 Marks) + Practical (50 Marks) = Total Marks (150)**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

**Scheme of Semester End Examination (SEE); Practical (50 Marks)**

SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

<b>Semester I</b>		
<b>Professional Skill Development</b>		
<b>Course Code: 18HSS14</b>		<b>CIE Marks: 50</b>
<b>Credits: L: T:P 3:0:0</b>		<b>SEE Marks: Audit Course</b>
<b>Hours: 18L</b>		

<b>Unit – I</b>	<b>03 Hrs</b>
<b>Communication Skills:</b> Basics of Communication, Personal Skills & Presentation Skills – Introduction, Application, Simulation, Attitudinal Development, Self Confidence, SWOC analysis. <b>Resume Writing:</b> Understanding the basic essentials for a resume, Resume writing tips Guidelines for better presentation of facts. Theory and Applications.	
<b>Unit - II</b>	<b>08 Hrs</b>
<b>Quantitative Aptitude and Data Analysis:</b> Number Systems, Math Vocabulary, fraction decimals, digit places etc. Simple equations – Linear equations, Elimination Method, Substitution Method, Inequalities. <b>Reasoning – a. Verbal</b> - Blood Relation, Sense of Direction, Arithmetic & Alphabet. <b>b. Non- Verbal reasoning</b> - Visual Sequence, Visual analogy and classification. <b>Analytical Reasoning</b> - Single & Multiple comparisons, Linear Sequencing. <b>Logical Aptitude</b> - Syllogism, Venn-diagram method, Three statement syllogism, Deductive and inductive reasoning. Introduction to puzzle and games organizing information, parts of an argument, common flaws, arguments and assumptions. <b>Verbal Analogies/Aptitude</b> – introduction to different question types – analogies, Grammar review, sentence completions, sentence corrections, antonyms/synonyms, vocabulary building etc. Reading Comprehension, Problem Solving	
<b>Unit - III</b>	<b>03 Hrs</b>
<b>Interview Skills:</b> Questions asked & how to handle them, Body language in interview, and Etiquette – Conversational and Professional, Dress code in interview, Professional attire and Grooming, Behavioral and technical interviews, Mock interviews - Mock interviews with different Panels. Practice on Stress Interviews, Technical Interviews, and General HR interviews	
<b>Unit - IV</b>	<b>02 Hrs</b>
<b>Interpersonal and Managerial Skills:</b> Optimal co-existence, cultural sensitivity, gender sensitivity; capability and maturity model, decision making ability and analysis for brain storming; Group discussion(Assertiveness) and presentation skills	
<b>Unit - V</b>	<b>07 Hrs</b>
<b>Motivation:</b> Self-motivation, group motivation, Behavioral Management, Inspirational and motivational speech with conclusion. (Examples to be cited). <b>Leadership Skills:</b> Ethics and Integrity, Goal Setting, leadership ability.	

<b>Course Outcomes: After going through this course the student will be able to:</b>	
<b>CO1</b>	Develop professional skill to suit the industry requirement.
<b>CO2</b>	Analyze problems using quantitative and reasoning skills
<b>CO3</b>	Develop leadership and interpersonal working skills.
<b>CO4</b>	Demonstrate verbal communication skills with appropriate body language.



<b>Reference Books:</b>	
1.	The 7 Habits of Highly Effective People, Stephen R Covey, 2004 Edition, Free Press, ISBN: 0743272455
2.	How to win friends and influence people, Dale Carnegie, 1 <sup>st</sup> Edition, 2016, General Press, ISBN: 9789380914787
3.	Crucial Conversation: Tools for Talking When Stakes are High, Kerry Patterson, Joseph Grenny, Ron Mcmillan 2012 Edition, McGraw-Hill Publication ISBN: 9780071772204
4.	Ethnus, Aptimithra: Best Aptitude Book, 2014 Edition, Tata McGraw Hill ISBN: 9781259058738

### **Scheme of Continuous Internal Examination (CIE)**

Evaluation of CIE will be carried out in TWO Phases.

<b>Phase</b>	<b>Activity</b>
<b>I</b>	After 9 hours of training program, students are required to undergo a test set for a total of 50 marks. The structure of the test will have two parts. Part A will be quiz based evaluated for 15 marks and Part B will be of descriptive type, set for 50 Marks and reduced to 35 marks. The total marks for this phase will be 50 ( 15 + 35).
<b>II</b>	Similarly students will have to take up another test after the completion 18 hours of training. The structure of the test will have two parts. Part A will be quiz based evaluated for 15 marks and Part B will be of descriptive type, set for 50 Marks and reduced to 35 marks. The total marks for this phase will be 50 (15 + 35).
<b>FINAL CIE COMPUTATION</b>	
Continuous Internal Evaluation for this course will be based on the average of the score attained through the two tests. The CIE score in this course, which is a mandatory requirement for the award of degree, must be greater than 50%. Needless to say the attendance requirement will be the same as in any other course.	

<b>Semester I</b>					
<b>ADVANCED COMPUTER ARCHITECTURE (Group A: Core Elective)</b>					
<b>Course Code</b>	:	<b>18MVE1A1</b>		<b>CIE Marks</b>	: 100
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>		<b>SEE Marks</b>	: 100
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	: <b>3 Hrs</b>
<b>Unit – I</b>					<b>10 Hrs</b>
<b>Fundamentals Of Computer Design</b>					
Introduction; Classes of computers; Defining computer architecture; Trends in Technology, Power in Integrated Circuits and cost; Dependability; Measuring, reporting and summarizing Performance; Quantitative Principles of computer design. Pipeline and its hazards; Implementation of pipeline; Parallel Computer Models- The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMP Computers, PRAM and VLSI Models.					
<b>Unit – II</b>					<b>9 Hrs</b>
<b>Processors and Memory Hierarchy</b>					
Advanced Processor Technology - Design Space of Processors, Instruction-Set Architectures CISC Scalar Processors RISC Scalar Processors. Superscalar and Vector Processors Superscalar Processors - The VLIW Architecture , Vector and Symbolic Processors. Memory Hierarchy Technology - Hierarchical Memory Technology, Inclusion, Coherence, and Locality Memory Capacity Planning; Virtual Memory Technology- Virtual Memory Models, TLB, Paging, and Segmentation Memory Replacement Policies Cache Memory Organizations - Cache Addressing Models, Direct Mapping and Associative Cache, Set-Associative and Sector Caches and Cache Performance Issues . Shared-Memory Organizations- Interleaved Memory Organization , Bandwidth and Fault Memory Allocation Schemes					
<b>Unit – III</b>					<b>9 Hrs</b>
<b>Multiprocessors and Multicomputer</b>					
Multiprocessor System Interconnects - Hierarchical Bus Systems, Crossbar Switch and Multiport Memory, Multistage and Combining Networks. Cache Coherence and Synchronization Mechanisms- The Cache Coherence Problem, Snoopy Bus Protocols, Directory-Based Protocols, Hardware Synchronization Mechanisms. Three Generations of Multicomputer - Design Choices in the Past , Present and Future Development , The Intel Paragon System. Message-Passing Mechanisms- Message-Routing Schemes, Deadlock and Virtual Channels Flow Control Strategies, Multicast Routing Algorithms.					
<b>Unit – IV</b>					<b>9 Hrs</b>
<b>Multivector and SIMP Computers</b>					
Vector Processing Principles- Vector Instruction Types , Vector-Access Memory Schemes Past and Present Supercomputers, Multivector Multiprocessors , Performance-Directed Design Rules Mainframes and Mini supercomputers, Compound Vector Processing -Compound Vector Operations , Vector Loops and Chaining , Multi pipeline Networking. SIMP Computer Organizations					
<b>Unit – V</b>					<b>9 Hrs</b>
<b>Scalable, Multithreaded and Dataflow Architectures</b>					
Latency-Hiding Techniques - Shared Virtual Memory , Prefetching Techniques, Distributed Coherent Caches , Scalable Coherence Interface, Relaxed Memory Consistency , Principles of Multithreading, Multithreading Issues and Solutions , Multiple-Context Processor, Multidimensional Architectures, Scalable and Multithreaded Architectures, Dataflow and Hybrid Architectures.					

**Expected Course Outcomes:**

After taking up this course, the graduate will be able to:

- CO1: Understand pipelining concepts, the performance metrics of microprocessors, Multithreading, multivector and dataflow architectures.
- CO2: Identify the factors affecting performance in superscalar processors and the key components, options and tradeoffs that a designer has to consider when designing such processors
- CO3: Evaluate the performance and efficiency in advanced multiple-issue processors.
- CO4: Design various architectures and techniques for building high performance scalable multithreaded and multiprocessor systems.

**Reference Books:**

1.	Kai Hwang, " <i>Advanced Computer Architecture: Parallelism, Scalability, Programmability</i> ", McGraw-Hill, first edition, 1992.
2.	Kai Hwang, Faye A. Briggs, " <i>Computer Architecture and parallel processing</i> " McGraw-Hill, first edition, 1984.
3.	Patterson, D.A., and Hennessy, J.L. , " <i>Computer Architecture : A Quantitative Approach</i> ", Morgan Kaufmann Publishers, 5th Edition, Inc.2011
4.	Dezso Sima, Peter Kacsuk, Terence Fountain, " <i>Advanced Computer Architectures : A Design Space Approach</i> ", Pearson Education India, 1997
5.	Michael J Flynn, " <i>Computer Architecture: Pipelined and Parallel Processor Design</i> ", Narosa Publishing India, 2003

**Continuous Internal Evaluation (CIE): Total marks: 100****Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100****Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester I</b>					
<b>ASIC DESIGN (Group A: Core Elective)</b>					
<b>Course Code</b>	:	<b>18MVE1A2</b>		<b>CIE Marks</b>	: 100
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>		<b>SEE Marks</b>	: 100
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	: <b>3 Hrs</b>
<b>Unit – I</b>					<b>10 Hrs</b>
<b>Introduction to ASICs</b>					
<b>Types of ASICs:</b> Full Custom ASIC, Semi-custom based ASICs, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channelless gate array, Structured gate array, Programmable logic devices, FPGA.					
<b>Design flow.</b>					
<b>Unit – II</b>					<b>10 Hrs</b>
<b>CMOS Logic</b>					
<b>Combinational logic cells Sequential logic cells:</b> Latch, flipflop, clocked inverter.					
<b>Data logic cells:</b> Data Path Elements, Adders, Multipliers, Arithmetic operator.(Practical approach).					
<b>I/O Cell, Cell Compilers</b>					
<b>Unit – III</b>					<b>9 Hrs</b>
<b>ASIC Library Design</b>					
<b>Logical effort:</b> predicting delay, logical area and logical efficiency, logical paths, multi stage cells, optimum delay, optimum no. of stages.					
Library cell design.					
<b>Programmable ASICs:</b> The Antifuse, Static RAM, EPROM and EEPROM technology.					
<b>Unit – IV</b>					<b>9 Hrs</b>
<b>Programmable ASICs logic cells</b>					
<b>Actel ACT:</b> ACT1 logic module, Shannon’s expansion theorem, Multiplexer logic as function generators, Timing models and critical path, speed gating, worst case timing.					
<b>Programmable ASIC Design Software:</b> Design System, logic synthesis, Introduction to Synthesis and Simulation. (Practical analysis of the design parameters for speed, area & power optimization).					
<b>Low-Level Design Entry:</b> Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC’S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation.					
<b>Unit – V</b>					<b>9 Hrs</b>
<b>ASIC Construction Floor Planning and Placement &amp; Routing</b>					
Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods.					
Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.					
<b>Expected Course Outcomes:</b>					
After taking up this course, the graduate will be able to:					
CO1: Learn the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test.					
CO2: Apply & analyze the design parameters for speed, area & power optimization.					
CO3: Develop the algorithms required for the design of ASIC.					
CO4: Apply the back-end physical design flow, including floorplanning, placement, and Routing techniques,					
<b>Reference Books:</b>					
1.	M.J.S .Smith, - “Application - Specific Integrated Circuits” – Pearson Education, 2003, ISBN:978-817758-408-0				

2.	H. Bhatnagar, - “Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime”, 2nd edition, 2001, ISBN:0792385373
3.	Farzad Nekoogar Farak Nekooga From ASICs-to-SOCs: A Practical Approach ISBN: 0-13-033857-5.
4.	P. Kurup, T. Abbasi, "Logic Synthesis Using Synopsys", ISBN 0-7923-9582-4
5.	D. J. Smith, "HDL Chip Design", ISBN 0-9651934-3-8

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester I</b>					
<b>ALGORITHMS FOR VLSI DESIGN (Group A: Core Elective)</b>					
<b>Course Code</b>	<b>:</b>	<b>18MVE1A3</b>		<b>CIE Marks</b>	<b>: 100</b>
<b>Credits : L:T:P</b>	<b>:</b>	<b>4:0:0</b>		<b>SEE Marks</b>	<b>: 100</b>
<b>Hrs</b>	<b>:</b>	<b>48L</b>		<b>SEE Duration</b>	<b>: 3 Hrs</b>
<b>Unit – I</b>					<b>10 Hrs</b>
<b>High Level Synthesis:</b> Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations. <b>VLSI Simulation:</b> Gate-level modelling and simulation - Switch-level modelling and simulation - Combinational Logic Synthesis - Binary Decision Diagram.					
<b>Unit – II</b>					<b>10 Hrs</b>
<b>Data Structure and Basic Algorithms :</b> Basic Terminology, Graph Search Algorithms Computational Geometry Algorithms. <b>VLSI partitioning&amp; floor planning:</b> Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms. Problem formulation, classification, Constraint based, Integer programming based, rectangular dualization, simulated evolution floor planning algorithms.					
<b>Unit – III</b>					<b>9 Hrs</b>
<b>Placement and Routing :</b> Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms. <b>Global Routing :</b> Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path based Algorithms, Steiner tree based Algorithms <b>Detailed Routing:</b> Problem formulation, Classification single Layer routing, General river routing, Single row routing.					
<b>Unit – IV</b>					<b>9 Hrs</b>
<b>Clock and Power Routing :</b> Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms. <b>Compaction:</b> Classification of Compaction Algorithms, One-Dimensional Compaction, Two-Dimensional Compaction, Hierarchical Compaction.					
<b>Unit – V</b>					<b>9 Hrs</b>
<b>Genetic algorithm and its application in VLSI physical design:</b> Terminologies – Simple Genetic algorithms ,steady state algorithm – Genetic operators-types of GA-Genetic algorithms vs Conventional algorithms – GA example – GA for VLSI design. Genetic algorithm in partitioning , placement and routing.					
<b>Expected Course Outcomes:</b> After taking up this course, the graduate will be able to: CO1. Understand each stage of VLSI design flow. CO2. Apply design knowledge to develop algorithms for VLSI design automation. CO3. Investigate the algorithms for optimizing VLSI design with respect to speed, power and area. CO4. Create an optimized VLSI cell using various algorithms.					
<b>Reference Books:</b>					
1.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 1998, ISBN: 978-0-471-98489-4				
2.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002, ISBN: 0-7923-8393-1				
3.	Pinaki mazumder and Elizabeth M Rudnick, “Genetic algorithms for VLSI design layout and test automation”, Pearson Edition, 2011.				

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester I</b>						
<b>MEMS AND SMART SYSTEMS</b> <b>(Group B: Core Elective)</b> <b>(Common to VLSI &amp; ES and CS)</b>						
<b>Course Code</b>	:	<b>18MVE1B1</b>		<b>CIE Marks</b>	:	100
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>		<b>SEE Marks</b>	:	100
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	:	<b>3 Hrs</b>
<b>Unit – I</b>						<b>10 Hrs</b>
<b>Introduction to MEMS and principle of operation.</b> Introduction, History of evolution, Definition of MEMS in a broader sense. Components of a smart system. Commercial products. Microsystems and Miniaturization. Evolution of micro-manufacturing. Design Aspects. Application and future scope of MEMS devices, Market trends. Definitions and salient features of sensors, actuators and systems. Working principles of Microsystems. Sensors: silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, Actuators: silicon micro-mirror arrays, piezo-electric based inkjet printhead, electrostatic comb-drive and micromotor, magnetic micro relay.						
<b>Unit – II</b>						<b>10 Hrs</b>
<b>Micro and Smart Devices and Systems: Materials and Processing</b> <b>Materials</b> Introduction, Substrates and Wafers, Active substrate materials, Si as a substrate material, Si compounds, Si Piezoresistors, Gallium Arsenide, Quartz, Piezoelectric Crystals and Polymers. <b>Processing</b> Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization, Silicon micromachining: surface and bulk, bonding based process flows. Thick-film processing: Smart material processing, Emerging trends.						
<b>Unit – III</b>						<b>9 Hrs</b>
<b>Mechanical modelling and Scaling laws in Microsystems Modelling</b> Simplest deformable element: a bar, Transversely deformable element: a beam, Bimorph effect, Mechanical vibration: general formulation, Resonant Vibration, Design theory of accelerometers and damping coefficients. Basics of fluid mechanics in macro and mesoscales, Capillary effect, electro-phoresis and Dielectrophoresis. <b>Scaling laws in Miniaturization</b> Importance of scaling in MEMS- Scaling in geometry, Scaling in rigid body dynamics, scaling in electrostatic forces, scaling in electromagnetic forces, scaling in electricity, scaling in fluid dynamics. scaling effects in the optical domain, scaling in biochemical phenomena.						
<b>Unit – IV</b>						<b>9 Hrs</b>
<b>RF MEMS</b> Introduction to RF MEMS, Static Analysis of RF MEMS devices: Spring Constant of Low-k Beams, Spring Constant of Cantilever Beams, Spring Constant of Circular Diaphragms, Beam Curvature due to Stress Gradients. Electrostatic Actuation, Shape of the Deformed Beam Under Electrostatic Actuation, DC Hold-Down Voltage of MEMS Beams and Cantilevers, Forces on MEMS Beams, Self-Actuation of MEMS Capacitive Switches, RF Hold-Down Voltage of MEMS Capacitive Switches.						
<b>Unit – V</b>						<b>9 Hrs</b>
<b>Case study of devices:</b> Pressure sensors, accelerometers, micro pump, micro heater. Introduction to CAD tool for simulation of devices. <b>Packaging :</b> Integration of Microsystems and microelectronics, Packaging Introduction, Micro Systems Packaging, Objectives, Issues in packaging, Special issues in micro system packaging, Types of Microsystem Packages, Packaging Technologies.						
<b>Expected Course Outcomes:</b> After going through this course the student will be able to:						



CO1 :Explain the technology to fabricate advanced micro- and smart systems  
 CO2: Analyse different methods to fabricate MEMS devices.  
 CO3: Apply the basics of implementation of MEMS into products.  
 CO4: Evaluate the principles and processes involved in the implementation of MEMS devices

**Reference Books:**

1.	Dr. A.K.Aatre, Ananth Suresh, K.J.Vinoy, S. Gopala krishna, K.N.Bhat., “Micro and Smart Systems”, John Wiley Publications, 2002, ISBN: 1118213904, 9781118213902
2.	Tai-Ran Tsu, “MEMS & Microsystems: Design and Manufacture”, Tata Mc-Graw-Hill.2002.8th reprint, ISBN-13:978-0-07-048709-3. ISBN-10:0-07-048709-X
3.	RF MEMS Theory, Design and Technology GABRIEL M. REBEIZ. 2003A JOHN WILEY & SONS PUBLICATION. ISBN: 978-0-471-20169-4
4.	S. D. Senturia, “Microsystems Design”, Kluwer Academic Publishers, Boston, USA, 2001, ISBN 0-7923-7246-8

**Continuous Internal Evaluation (CIE): Total marks: 100****Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100****Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester I</b>					
<b>SYSTEM ON CHIP DESIGN (Group B: Core Elective)</b>					
<b>Course Code</b>	:	<b>18MVE1B2</b>		<b>CIE Marks</b>	: 100
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>		<b>SEE Marks</b>	: 100
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	: 3 Hrs
<b>Unit – I</b>					<b>10 Hrs</b>
<p><b>Motivation for SoC Design:</b> Introduction to SoC, SoB, SiP, Benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap.</p> <p><b>System On Chip Design Process:</b> Canonical SoC Design, SoC Design flow - waterfall vs spiral, Top-down vs Bottom up, Specification requirement, Types of Specification, System Design process, System level design issues- Soft IP vs Hard IP, Design for timing closure, Logic design issues- Verification strategy, On-chip buses and interfaces, Low Power, Manufacturing test strategies.</p>					
<b>Unit – II</b>					<b>10 Hrs</b>
<p><b>Macro Design Process:</b> Overview of IP Design, Key Features, Planning and Specification, Macro design and Verification.</p> <p><b>Developing Hard Macros:</b> Overview, Design Issues for Hard Macros, The Hard Macro Design Process, Productization of Hard Macros.</p>					
<b>Unit – III</b>					<b>9 Hrs</b>
<p><b>SoC Verification:</b>-Verification technology options, Verification methodology, Verification languages, Verification IP Reuse, approaches. Verification and Device Test, Verification Plans.</p> <p><b>VLSI Packaging:</b> Introduction, Packaging, Power Distribution, Input/Output, Chip-Package Co-design.</p>					
<b>Unit – IV</b>					<b>9 Hrs</b>
<p><b>Interconnect architectures for SoC.</b> Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole routing.</p>					
<b>Unit – V</b>					<b>9 Hrs</b>
<p><b>MPSoCs:</b> What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design: The limitations of traditional ASIC design, General Purpose Processor, The impact of SoC integration.</p>					
<b>Expected Course Outcomes:</b>					
After going through this course the student will be able to:					
CO1: Learn about the system on chip design and macro design process.					
CO2: Analyze the design flow, IP cores, routing used in system on chip .					
CO3: Exposure the concepts of verification methodology and interconnection methods in SoC					
CO4: Design & Develop the algorithms required for the design of IP and SoC and Exposure to the concept of MPSoCs.					
<b>Reference Books:</b>					
1	Michael Keating, Pierre Bricaud, Reuse Methodology manual for System-On-A-Chip Designs, Kluwer Academic Publishers, second edition, 2001.				
2	Prakash Rashinkar, Peter Paterson and Leena Singh, SoC Verification-Methodology and Techniques, Kluwer Academic Publishers, 2001.				
3	A.A.Jerraya, W.Wolf, Multiprocessor Systems-on-chips, 1st Edition, Morgan Kaufmann, 2004				

4	Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.
5	Rao R. Tummala, Madhavan Swaminathan, "Introduction to system on package sop- Miniaturization of the Entire Syste", McGraw-Hill, 2008.
6	Neil H E Weste, David Harris, Ayan Banerjee, " CMOS VLSI Design", Third edition Pearson Education, ISBN: 0321149017

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester I</b>						
<b>ADVANCED VLSI DEVICES</b>						
<b>(Group B: Core Elective)</b>						
<b>Course Code</b>	:	<b>18MVE1B3</b>		<b>CIE Marks</b>	:	<b>100</b>
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>		<b>SEE Marks</b>	:	<b>100</b>
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	:	<b>3 Hrs</b>
<b>Unit – I</b>					<b>10 Hrs</b>	
MOSFET Device Metrics, Transistors to Circuits, Energy Band View of Transistors, Traditional IV Theory, The "Virtual Source Model". <b>MOS Electrostatics:</b> Introduction, Depletion Approximation. Gate Voltage and Surface Potential, Flatband Voltage, Mobile Charge: Bulk MOS, Mobile Charge: ETSOI, 2D Electrostatics, The VS Model Revisited						
<b>Unit – II</b>					<b>10 Hrs</b>	
<b>Short Channel Effects and Challenges to CMOS:</b> Short channel effects, scaling theory, processing challenges to further CMOS miniaturization						
<b>Unit – III</b>					<b>10 Hrs</b>	
<b>Beyond CMOS:</b> Evolutionary advances beyond CMOS, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing						
<b>Unit – IV</b>					<b>9 Hrs</b>	
<b>Ballistic Nanotransistor:</b> Introduction, Landauer Approach, More on Landauer, The Ballistic MOSFET, The Velocity at the VS Model, Revisiting the VS Model <b>The Transmission Theory of the MOSFET:</b> Introduction, Transmission, MFP and Diffusion Coefficient, Transmission Theory of the MOSFET, Connection to the VS Model, Analysis of the Experiments, Limits and Limitations						
<b>Unit – V</b>					<b>9 Hrs</b>	
<b>Advanced CMOS:</b> New Materials and Device Structures (CMOS circuits, SOI MOSFETs, Heterostructure FETs, Nanotube FETs, Nanowire FETs, Novel steep subthreshold slope devices, Alternative devices (Excitons, Spin, Phase Transitions)						
<b>Expected Course Outcomes:</b> After going through this course the student will be able to:						
<ol style="list-style-type: none"> <li>1. Describe the physics of semiconductor, basic theory of Metal Semiconductor Contacts and PN junction, MOS &amp; transport mechanism</li> <li>2. Apply the VLSI device parameters and calculate the device performance</li> <li>3. Analyze various modern VLSI devices &amp; compare its performances with MOS devices</li> <li>4. Evaluate or design the transport mechanism and modelling for emerging devices</li> </ol>						
<b>Reference Books:</b>						
1.	Advanced Semiconductor Fundamentals, 2nd Edition, R. F. Pierret, Prentice Hall, ISBN No. 0-13-061792-X.					
2.	Fundamentals of Modern VLSI Devices, 2nd Edition, Yuan Taur and Tak H. Ning, Cambridge University Press, 2009, ISBN No. 9780521832946.					
3.	Kevin F Brennan, "Introduction to Semiconductor Devices: For Computing and Telecommunications Applications", Cambridge University Press; 1 edition, ISBN No. 978-0521831505					
4.	Y.P. Tsividis, Colin McAndrew "Operation and Modeling of the MOS Transistor", 3 <sup>rd</sup> Edition, Oxford Univ Press, 2014, ISBN:978-0195170153					

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester II</b>					
<b>ANALOG IC DESIGN (Theory &amp; Practice)</b>					
<b>Course Code</b>	:	<b>18MVE21</b>	<b>CIE Marks</b>	:	100+50
<b>Credits : L:T:P</b>	:	<b>3:1:1</b>	<b>SEE Marks</b>	:	100+50
<b>Hrs</b>	:	<b>48L+36P</b>	<b>SEE Duration</b>	:	<b>3 Hrs</b>
<b>Unit – I</b>					<b>10 Hrs</b>
<b>MOS transistors:</b> Components available in a CMOS process, MOS small signal models, concept of $f_T$ , noise model.					
<b>Single stage Amplifiers:</b> Basic concepts, dc analysis, small signal analysis and noise analysis of common source and common gate stage, power, bandwidth, impedance and frequency scaling of circuits, Frequency response of CS amplifier, Cascode stage- Folded Cascode.					
<b>Current Mirror:</b> Basic Current Mirrors, Cascode current Mirrors, amplifiers biased at constant currents.					
<b>Unit – II</b>					<b>9 Hrs</b>
<b>Differential Amplifiers:</b> Single ended and differential operation, Common mode response, differential pair with active loads, Gilbert cell					
<b>Operational Amplifier:</b> One stage op-amp, two stage op-amp, Telescopic Cascode opamp, Telescopic Cascode opamp frequency response, Folded Cascode opamp-dc gain, Telescopic and folded Cascode opamp-noise, mismatch, slew rate, Two stage opamp-topology, frequency response, gain boosting, common mode feedback.					
<b>Unit – III</b>					<b>10 Hrs</b>
<b>Noise:</b> Resistors, MOSFET, Input and output referred noise, noise scaling, basic amplifier stages – CS and CG stage					
<b>Feedback:</b> Non-idealities- finite dc gain, effect of additional poles & zeros, feedback topologies, sense and return mechanisms, effect of loading, effect of feedback on noise, feedback circuit analysis using return ratio – closed loop gain and impedance using return ratio					
<b>Unit – IV</b>					<b>9 Hrs</b>
<b>Stability analysis and Frequency compensation:</b> Stability of Feedback: Basic Concepts, Instability and the Nyquist Criterion. Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation					
<b>Band gap reference:</b> Band gap reference, Constant current and constant gm bias generators, reducing supply sensitivity					
<b>Low dropout regulators:</b> Basic requirements and constraints					
<b>Unit – V</b>					<b>9Hrs</b>
<b>Phase Locked Loops :</b> Simple Phase locked loop, Charge pump PLL, Non-ideal effects - Jitter & Phase noise, Applications					
<b>Analog Layout techniques:</b> General layout considerations – design rules, antenna effect, layout techniques for multi finger transistors, symmetry, reference distribution, passive devices, interconnects, Electro static discharge (ESD) protection, substrate coupling					
<b>Lab Component</b>					
<ol style="list-style-type: none"> <li>1. Study of DC and small signal models of a MOS Transistor</li> <li>2. Design of MOS current sources and mirrors</li> <li>3. Design of single stage amplifiers – CS Amplifier with different loads</li> <li>4. Design of a MOS Differential amplifier with an active load</li> <li>5. Design of a cascode amplifier , double cascode and triple cascode amplifier</li> <li>6. Design of Telescopic opamp</li> <li>7. Design of a 2-stage CMOS Op-Amp</li> </ol>					

8. Design of Band Gap Reference circuit 9. Post-layout simulation of any two circuits	
<b>Expected Course Outcomes:</b> After going through this course the student will be able to:  CO1: Define & demonstrate device, circuit & system aspects of analog IC design CO2: Analyze the functionality of analog circuits & systems CO3: Design and implement analog integrated circuits & systems CO4: Evaluate the different performance parameters of analog integrated circuits & systems using CAD tools.	
<b>Reference Books:</b>	
1.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Mc GrawHill Edition, 2002, ISBN: 0-07-238032-2
2.	R. Jacob Baker, Harry W. Li and David E. Boyce, “CMOS Circuit Design, Layout and Simulation”, IEEE Press, 2002, ISBN: 81-203-1682-7
3.	Gray, Hurst, Lewis, and Meyer: “Analysis and design of Analog Integrated Circuits”, (4/e), John Wiley & Sons, ISBN-10: 0470245999
4.	Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, (2/e) Oxford University Press, February 2002, ISBN: 9780199765072
5.	David Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, Inc.,1997, ISBN-10: 0470770104

**Continuous Internal Evaluation (CIE): Total marks: 100+50=150****Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Scheme of Continuous Internal Evaluation (CIE) for Practicals: ( 50 Marks)**

The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

**Semester End Evaluation (SEE): Total marks: 100+50=150**

**Theory (100 Marks) + Practical (50 Marks) = Total Marks (150)**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

**Scheme of Semester End Examination (SEE); Practical (50 Marks)**

SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

<b>Semester II</b>						
<b>SYSTEM VERILOG FOR DESIGN AND VERIFICATION</b>						
<b>Course Code</b>	:	<b>18MVE22</b>		<b>CIE Marks</b>	:	<b>100</b>
<b>Credits : L:T:P</b>	:	<b>3:1:0</b>		<b>SEE Marks</b>	:	<b>100</b>
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	:	<b>3 Hrs</b>
<b>Unit – I</b>						<b>10 Hrs</b>
<b>Introduction to SystemVerilog:</b>						
SystemVerilog standards, Key SystemVerilog enhancements for hardware design. Advantages of System Verilog over Verilog, Data Types: Verilog data types, System Verilog data types, 2 - State Data types, Bit, byte, shortint, int, longint. 4 - State data types. Logic, Enumerated data types, User Defined data types, Struct data types, Strings, Packages, Type Conversion: Dynamic casting, Static Casting, Memories: Arrays, Dynamic Arrays, Multidimensional Arrays, Packed Arrays, Associative Arrays, Queues, Array Methods, Tasks and Functions: Verilog Tasks and Functions, Enhancements in S.V, Void Functions, Return Statement, Passing Arguments, Arguments Passing by Name, Default Arguments, Passing Arguments by Value, Passing Arguments by Reference.						
<b>Unit – II</b>						<b>10 Hrs</b>
<b>Connecting the Testbench and Design:</b>						
Verilog interface signals - Limitations of Verilog interface signals, SystemVerilog interfaces, SystemVerilog port connections, Interface instantiation 2.4. Interfaces Arguments, Interface Modports, Interface References, Tasks and functions in interface, Verilog Event Scheduler, SystemVerilog Event Scheduler, Clocking Block, Input and Output Skews, Typical Testbench Environment, Verification plan						
<b>Unit – III</b>						<b>9 Hrs</b>
<b>OOPs Basics and Advanced OOPs concepts:</b>						
<b>Basic OOP Concepts</b>						
Overview of Classes, Properties and Methods in the Classes, Instance/Object Creation, New Constructor, Null Object handles, Accessing Members, this Keyword, Creating an Object, Objects Assignments, Copying an Object: Shallow Copy, Deep Copy						
<b>Advanced OOP Concepts</b>						
Inheritance: Concept of Inheritance, Super Keyword, Static properties, Overriding Methods, Polymorphism - \$cast, Virtual Classes, Parameterized Classes						
<b>Unit – IV</b>						<b>9 Hrs</b>
<b>Constrained Randomization, Threads and Inter-process Communication:</b>						
<b>Constrained Randomization</b>						
Random Variables - rand and randc, Randomize( ) Method - Pre/Post Randomize( ) methods, Constraints in the class, Rand_mode and constraint_mode, Constraint and Inheritance, Constraint Overriding, Set Membership, Distribution Constraints, Conditional Constraints - .implication (->), .if/else, Inline Constraints						
<b>Threads and Inter-process Communication</b>						
Threads, Fork-Join/Join_any/Join_none, Communication – Mailbox, Semaphore, Events, Building a Testbench with Threads and IPC						
<b>Unit – V</b>						<b>9 Hrs</b>
<b>Functional Coverage and Assertion Based Verification:</b>						
<b>Functional Coverage</b>						
Coverage Definition, Code Coverage, Functional Coverage: Cover Group, Creating Cover Group Instances,						



<p>Coverpoints, Bins - . implicit bins, . Explicit bins, Bin creation, Vector and Scalar bins, Cross products, Intersect, Select Expressions, Conditional Expression (iff), Illegal bins, Ignore bins, Coverage Analysis, Covergroup Built-in Methods - . Sample(), . get_coverage(), .get_instance_coverage(), .set_instance_name(string), .start(), . stop()</p> <p><b>Assertion Based Verification</b></p> <p>Introduction, Types of Assertions - . Immediate, . Concurrent, Assertion Properties- . Writing Properties, Sequences- . Sequence Composition, . and, or, intersect, Advanced SVA Features - Expect, Binding, Assertion Coverage</p>	
<p><b>Expected Course Outcomes:</b></p> <p>After taking up this course, the graduate will be able to:</p> <p>CO1: Demonstrate the use of System Verilog data types for digital system design and functional verification.</p> <p>CO2: Demonstrate the skill on writing test-benches for design of digital systems and connecting them with the design.</p> <p>CO3: Verify and Analyze the complete systems through robust verification methods such as assertion based verification.</p> <p>CO4: Design and verify the digital systems such as FIFOs, memories, ATM interfaces, etc. using the learnt methods and demonstrate the skills.</p>	
<p><b>Reference Books:</b></p>	
1.	Stuart Sutherland, Simon Davidmann and Peter Flake, “SystemVerilog for Design - A Guide to Using SystemVerilog for Hardware Design and Modeling,” 2E, Springer Science, ISBN-13: 978-0387-3339-91, 2006.
2.	C Spear, “SystemVerilog for Verification-A Guide to Learning the Testbench Language Features,” Springer Science, IEEE press, ISBN-13: 978-0387-2703-64,2006.
3.	Doulos, “SystemVerilog golden reference guide-A concise guide to SystemVerilog IEEE Standard-1800-2009,” Version 5.0,ISBN: 0-9547345-9-9, 2012.
4.	Sasan Iman, “Step-by-Step Functional Verification with SystemVerilog and OVM,” Hansen Brown Publishing Company,ISBN-13: 978-0-9816-5621-2, 2008.
5.	IEEE Computer Society, “IEEE Standard for SystemVerilog-Unified Hardware Design, Specification and Verification,” IEEE Press, ISBN: 978-0-7381-6129-7, 2009

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester II</b>						
<b>RESEARCH METHODOLOGY</b>						
<b>Course Code</b>	:	<b>18IM23</b>		<b>CIE Marks</b>	:	<b>100</b>
<b>Credits : L:T:P</b>	:	<b>3:0:0</b>		<b>SEE Marks</b>	:	<b>100</b>
<b>Hrs</b>	:	<b>36L</b>		<b>SEE Duration</b>	:	<b>3 hours</b>
<b>Unit – I</b>					<b>07 Hrs</b>	
<b>Overview of Research:</b> Research and its types, identifying and defining research problem and introduction to different research designs. Essential constituents of Literature Review. Basic principles of experimental design, completely randomized, randomized block, Latin Square, Factorial.						
<b>Unit – II</b>					<b>08 Hrs</b>	
<b>Data and data collection:</b> Overview of probability and data types Primary data and Secondary Data, methods of primary data collection, classification of secondary data, designing questionnaires and schedules. <b>Sampling Methods:</b> Probability sampling and Non-probability sampling						
<b>Unit – III</b>					<b>07 Hrs</b>	
<b>Processing and analysis of Data:</b> Statistical measures of location, spread and shape, Correlation and regression, Hypothesis Testing and ANOVA. Interpretation of output from statistical software tools						
<b>Unit – IV</b>					<b>07 Hrs</b>	
<b>Advanced statistical analyses:</b> Non parametric tests, Introduction to multiple regression, factor analysis, cluster analysis, principal component analysis. Usage and interpretation of output from statistical analysis software tools.						
<b>Unit-V</b>					<b>07 Hrs</b>	
<b>Essentials of Report writing and Ethical issues:</b> Significance of Report Writing , Different Steps in Writing Report, Layout of the Research Report , Ethical issues related to Research, Publishing, Plagiarism. <b>Case studies:</b> Discussion of case studies specific to the domain area of specialization						
<b>Course Outcomes:</b> After going through this course the student will be able to						
CO1: Explain the principles and concepts of research types, data types and analysis procedures.						
CO2: Apply appropriate method for data collection and analyze the data using statistical principles.						
CO3: Present research output in a structured report as per the technical and ethical standards.						
CO4: Create research design for a given engineering and management problem situation.						
<b>Reference Books:</b>						
1) Kothari C.R., Research Methodology Methods and techniques by, New Age International Publishers, 4th edition, ISBN: 978-93-86649-22-5						
2) Krishnaswami, K.N., Sivakumar, A. I. and Mathirajan, M., Management Research Methodology, Pearson Education: New Delhi, 2006. ISBN: 978-81-77585-63-6						
3) Levin, R.I. and Rubin, D.S., Statistics for Management, 7th Edition, Pearson Education: New Delhi.						

**Continuous Internal Evaluation (CIE): Total marks: 100****Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Semester: II						
MINOR PROJECT						
Course Code	:	18MVE24		CIE Marks	:	100
Credits L: T: P	:	0:0:4		SEE Marks	:	100
Credits	:	02		SEE Duration	:	3 hrs

GUIDELINES	
1.	Each project group will consist of maximum of two students.
2.	Each student / group has to select a contemporary topic that will use the technical knowledge of their program of study after intensive literature survey.
3.	Allocation of the guides preferably in accordance with the expertise of the faculty.
4.	The number of projects that a faculty can guide would be limited to four.
5.	The minor project would be performed in-house.
6.	The implementation of the project must be preferably carried out using the resources available in the department/college.

Course Outcomes: After completing the course, the students will be able to	
CO1	Conceptualize, design and implement solutions for specific problems.
CO2	Communicate the solutions through presentations and technical reports.
CO3	Apply resource managements skills for projects.
CO4	Synthesize self-learning, team work and ethics.

#### Scheme of Continuous Internal Examination

Evaluation will be carried out in 3 phases. The evaluation committee will comprise of 4 members: Guide, Two Senior Faculty Members and Head of the Department.

Phase	Activity	Weightage
I	Synopsys submission, Preliminary seminar for the approval of selected topic and objectives formulation	20%
II	Mid term seminar to review the progress of the work and documentation	40%
III	Oral presentation, demonstration and submission of project report	40%

\*\* Phase wise rubrics to be prepared by the respective departments

#### CIE Evaluation shall be done with weightage / distribution as follows:

- Selection of the topic & formulation of objectives 10%
- Design and simulation/ algorithm development/ experimental setup 25%
- Conducting experiments/ implementation / testing 25%
- Demonstration & Presentation 15%
- Report writing 25%

#### Scheme of Semester End Examination (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

- Brief write up about the project 05%
- Presentation / Demonstration of the Project 20%
- Methodology and Experimental results & Discussion 25%
- Report 20%
- Viva Voce 30%

<b>Semester II</b>						
<b>VLSI TESTING</b>						
<b>(Group C: Core Elective)</b>						
<b>Course Code</b>	:	<b>18MVE2C1</b>		<b>CIE Marks</b>	:	<b>100</b>
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>		<b>SEE Marks</b>	:	<b>100</b>
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	:	<b>3 Hrs</b>
<b>Unit – I</b>					<b>9 Hrs</b>	
<b>Introduction to Testing:</b> Role of testing VLSI circuits, VLSI trends affecting testing, Physical Faults, Stuck-at Faults, Stuck open Faults, Permanent, Intermittent and Pattern Sensitive Faults, Delay Faults. <b>Fault Modeling-</b> Functional Testing, Structural Testing, Types of Fault Models, Stuck-at Faults, Bridging Faults, cross point faults, Fault Equivalence, Fault Dominance						
<b>Unit – II</b>					<b>9 Hrs</b>	
<b>Testability Measure</b> – Controllability, Observability, SCOAP measures for combinational and sequential circuits. <b>ATPG for Combinational Circuits:</b> Path Sensitization Methods, Roth’s D- Algorithm, Boolean Difference, PODEM Algorithm. Complexity of Sequential ATPG, Time Frame Expansion.						
<b>Unit – III</b>					<b>10 Hrs</b>	
<b>Design for Testability-</b> Ad-hoc, Structured DFT- Scan method, Scan Design Rules, Overheads of Scan Design, partial scan methods, multiple chain scan methods. <b>Fault Simulation-</b> Fault Simulation algorithm- Serial, Parallel, Deductive and Concurrent Fault Simulation. <b>Boundary Scan Standard</b> - TAP Controller, Test Instructions.						
<b>Unit – IV</b>					<b>10 Hrs</b>	
<b>Self test And Test Algorithms</b> Built-In self-Test, test pattern generation for BIST, response compaction - Parity checking, Ones counting, Transition Count, Signature analyzer.Circular BIST,BIST Architectures. Testable Memory Design Test Algorithms, Reduced Functional Faults-MARCH and MAT+ algorithm. Test generation for Embedded RAMs.						
<b>Unit – V</b>					<b>10 Hrs</b>	
<b>Fault Diagnosis</b> Logical Level Diagnosis, Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits, Self-checking design, System Level Diagnosis.						
CO1. Acquire knowledge about fault modeling & collapsing. CO2. Analyse various combinational ATPG techniques CO3. Evaluate the significance of sequential test pattern generation CO4. Develop fault simulation techniques & fault diagnosis methods						
<b>Reference Books:</b>						
1.	CO5. Michael L.Bushnell, Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuits”, Kluwer Academic Publications, 1999.					
2.	CO6. MironAbramovici, Melvin A. Breuer, Arthur D. Friedman, “ Digital Systems Testing and Testable Design”, 3rd Edition, Jaico Publishing House, 2004					
3.	CO7. Hideo Fujiwara, “ Logical testing & design for testability”, The MIT Press.					
4.	CO8. Parag.K.Lala "Digital Circuit Testing and Testability" Academic Press.					

**Continuous Internal Evaluation (CIE): Total marks: 100**

#### **Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

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seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester II</b>			
<b>MACHINE LEARNING</b> <b>(Group C: Core Elective)</b> <b>(Common to VLSI &amp; ES, CS, CNE, DCE, BMI, SE)</b>			
<b>Course Code</b>	<b>:</b>	<b>18MCS2C2</b>	<b>CIE Marks : 100</b>
<b>Credits : L:T:P</b>	<b>:</b>	<b>4:0:0</b>	<b>SEE Marks : 100</b>
<b>Hrs</b>	<b>:</b>	<b>48L</b>	<b>SEE Duration : 3 Hrs</b>
<b>Unit – I</b>			<b>9 Hrs</b>
<b>Introduction:</b> Overview of Probability Theory, Model Selection, Introduction to Machine learning. Linear Regression – Basis Function models, Bias Variance Decomposition, Bayesian linear Regression; Stochastic gradient Descent, Discriminant Functions, Bayesian Logistic regression. Examples on linear regression, logistic regression			
<b>Unit – II</b>			<b>10 Hrs</b>
<b>Supervised Learning</b> Kernel Methods: Dual representations, Construction of a kernel, Radial Basis Function Networks, Gaussian Process, Tree Based methods Sparse Kernel Machines: Maximum margin classifiers (SVM), RVM. Examples on spam, mixer and k nearest neighbour			
<b>Unit – III</b>			<b>10 Hrs</b>
<b>Unsupervised Learning:</b> <b>Mixture Models:</b> K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, The EM Algorithm in General, Principal Component Analysis, Probabilistic PCA, Examples on Market booklet analysis			
<b>Unit – IV</b>			<b>10 Hrs</b>
<b>Random Forests:</b> Introduction, Definition of Random Forests, Details of Random ,Out of Bag Samples , Variable Importance, Proximity Plots, Random Forests and Over-fitting, Analysis of Random Forests, Variance and the De-Correlation Effect, Bias, Adaptive Nearest Neighbors.			
<b>Unit – V</b>			<b>9 Hrs</b>
<b>Ensemble Learning:</b> Introduction, Boosting and Regularization Paths, Penalized Regression, The “Bet on Sparsity” Principle, Regularization Paths, Over-fitting and Margins, Learning Ensembles, Learning a Good Ensemble, Rule Ensembles			
<b>Expected Course Outcomes:</b> After going through this course the student will be able to: CO1: Explore the basics of Probability, data distributions and neural networks Algorithms. CO2: Apply the various dimensionality reduction techniques and learning models for the given Application. CO3: Analyze the different types of supervised and unsupervised learning models. CO4: Evaluate the classification and regression algorithms for given data set.			
<b>Reference Books:</b>			
1.	Christopher M Bishop: Pattern Recognition and Machine Learning, Springer, <b>February 2006 ISBN-10: 0-387-31073-8, ISBN-13: 978-0387-31073-2.</b>		
2.	Trevor Hastie, Robert Tibshirani, and Jerome Friedman: The Elements of Statistical Learning, Springer, 2008.		
3.	Jiawei Han and Micheline Kamber: Data Mining – Concepts and Techniques, Third Edition, Morgan Kaufmann, 2006, ISBN 1-55860-901-6		
4.	Zumel, N., & Mount, J. “Practical data science with R”, Manning Publications, 2014, ISBN 9781617291562		

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.



<b>Semester II</b>					
<b>HIGH SPEED VLSI DESIGN (Group C: Core Elective)</b>					
<b>Course Code</b>	:	<b>18MVE2C3</b>	<b>CIE Marks</b>	:	<b>100</b>
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>	<b>SEE Marks</b>	:	<b>100</b>
<b>Hrs</b>	:	<b>48L</b>	<b>SEE Duration</b>	:	<b>3 Hrs</b>
<b>Unit – I</b>					<b>10 Hrs</b>
<b>Introduction to high speed digital design:</b> Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.					
<b>Unit – II</b>					<b>10 Hrs</b>
<b>Power distribution and Noise:</b> Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference. Power distribution on chips.					
<b>Unit – III</b>					<b>9 Hrs</b>
<b>Signaling convention and circuits:</b> Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.					
<b>Unit – IV</b>					<b>9 Hrs</b>
<b>Clocked &amp; non clocked Logics:</b> <b>Non clocked Logic Styles:</b> Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families <b>Clocked Logic Styles:</b> Single-Rail Domino Logic, Dual-Rail Domino Structures					
<b>Unit – V</b>					<b>10 Hrs</b>
<b>Latching Strategies:</b> Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques, DDR memories.					
<b>Expected Course Outcomes:</b> After taking up this course, the graduate will be able to: CO1 Investigate the special requirements that are imposed on high speed digital design. CO2 Analyze the characteristics of transmission lines and high speed latches and circuits. CO3 Analyze the Signaling convention in transmission media and high speed digital logics. CO4 Evaluate the performance of various transmission lines and high speed digital circuits.					
<b>Reference Books:</b>					
1.	William S. Dally & John W. Poulton, “Digital Systems Engineering”, Cambridge University Press, 1998. ISBN 0-521-59292-5				
2.	Kerry Bernstein, Keith M. Carrig, Christopher M. Durham, Patrick R. Hansen, David Hogenmiller, Edward J. Nowak, Norman J. Rohrer., “High Speed CMOS Design Styles”, Kluwer Academic Publishers in 1999, ISBN 978-1-4613-7549-4.				
3.	Masakazu Shoji, “High Speed Digital Circuits”, Addison Wesley Publishing Company, 1996. ISBN 978-0201634839.				
4.	Howard Johnson & Martin Graham, “High Speed Digital Design” A Handbook of Black Magic, Prentice Hall PTR, 1993.				
5.	Jan M.Rabaey, Anantha Chadrakasan, Borivoje Nikolic, “Digital Integrated Circuits: A Design Perspective”, (2/e), Pearson 2016, ISBN-13: 978-0130909961.				

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester II</b>				
<b>LOW POWER VLSI DESIGN (Group D : Core Elective)</b>				
<b>Course Code</b>	<b>:</b>	<b>18MVE2D1</b>	<b>CIE Marks</b>	<b>:</b> <b>100</b>
<b>Credits : L:T:P</b>	<b>:</b>	<b>4:0:0</b>	<b>SEE Marks</b>	<b>:</b> <b>100</b>
<b>Hrs</b>	<b>:</b>	<b>48L</b>	<b>SEE Duration</b>	<b>:</b> <b>3 Hrs</b>
<b>Unit – I</b>				<b>10 Hrs</b>
<b>Introduction and Algorithm Level Low power Methods:</b>				
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.				
Algorithm Level low power Methods: Introduction, design flow, Algorithmic level analysis & optimization.				
<b>Unit – II</b>				<b>10 Hrs</b>
<b>Device &amp; Technology Impact on Low Power:</b>				
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.				
<b>Unit – III</b>				<b>9 Hrs</b>
<b>Power estimation methods</b>				
Simulation Power analysis:				
SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.				
Probabilistic power analysis:				
Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.				
<b>Unit – IV</b>				<b>9 Hrs</b>
<b>Low Power Design at Circuit level and Logic Level:</b>				
Low Power Design at Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.				
Low Power Design at Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.				
<b>Unit – V</b>				<b>10 Hrs</b>
<b>Low power Design at Architecture/System Level and Clock distribution:</b>				
Low power Architecture & Systems: Architectural level estimation & synthesis, Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.				
Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.				
<b>Course Outcomes:</b>				
After going through this course the student will be able to:				
<b>CO1:</b> Acquire the knowledge of the device physics, principles of analysis tools, circuits levels, logic levels and clock distribution techniques for low power designs.				
<b>CO2:</b> Identify, formulate, and solve engineering system design problems using low power VLSI design approaches and engineering tools.				
<b>CO3:</b> Use the techniques and skills in system designing through modern engineering tools such as logic works SPICE and description languages such as VHDL and Verilog.				
<b>CO4:</b> Design digital systems, components or processes to meet the desired low power needs within realistic constraints and create a research oriented platform in thrust areas such as Energy recovery, Quantum computation, Adiabatic computation, etc.				
<b>Reference Books:</b>				

1.	Jan M. Rabaey and MassoudPedram, “Low Power Design Methodologies” Kluwer Academic Publishers, 5th reprint, ISBN 978-1-46 13-5975-3, 2002.
2.	Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic Publishers, ISBN 978-1-4613-7778-8, 2002.
3.	Kaushik Roy and Sharat Prasad, “Low-Power CMOS VLSI Circuit Design”, John Wiley, 2000. ISBN 13 9788126520237
4.	Ajit Pal, “Low-Power VLSI Circuits and Systems,” Springer publications, ISBN: ISBN 978-81-322-1936-1, 2015
5.	A. P. Chandrakasan & R. W. Broderson: “Low power digital CMOS design”, KAP, 1996.
6.	Robert Aitken, Alan Gibbons, Kaijian Shi, Michael Keating, David Flynn, Michael Keating, “Low Power Methodology Manual For System-on-Chip Design” Springer, ISBN 978-0-387-71818-7, 2007.

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester II</b>			
<b>ADVANCED EMBEDDED PROCESSORS</b>			
<b>(Group D : Core Elective)</b>			
<b>Course Code</b>	: <b>18MVE2D2</b>	<b>CIE Marks</b>	: <b>100</b>
<b>Credits : L:T:P</b>	: <b>4:0:0</b>	<b>SEE Marks</b>	: <b>100</b>
<b>Hrs</b>	: <b>48L</b>	<b>SEE Duration</b>	: <b>3 Hrs</b>
<b>Unit – I</b>			<b>10 Hrs</b>
<b>Introduction</b> Embedded Processor Selection, PowerPC, ARM Cortex, SoC, Digital Signal Processors			
<b>ARM Cortex-M Series Technical Overview</b> Cortex-M Processor Family, Product Portfolio, Advantages, Applications, Cortex Microcontroller Software Interface Standard (CMSIS), General Information, Features			
<b>Unit – II</b>			<b>10 Hrs</b>
<b>Architecture of ARM Cortex-M Processor</b> Programmer's Model, Application Program Status Register (APSR), Memory System, Exceptions & Interrupts, System Control Block, Debug, Reset & Reset Sequence			
<b>Instruction Set-I</b> Assembly Language Syntax, Suffixes for Assembly Instructions, Unified Assembly Language, Assembly Instructions			
<b>Unit – III</b>			<b>9 Hrs</b>
<b>Instruction Set-II</b> Cortex-M4/M7 Specific Instructions, Barrel Shifter			
<b>Memory System</b> Memory Map, Connecting Cortex-M3/M4 with Memory & Peripherals, Endianness, Data Alignment & Unaligned Data Access Support, Bit Band Operations, Memory Access Attributes, Exclusive Access, Memory Barriers, Memory System in a MCU.			
<b>Unit – IV</b>			<b>9 Hrs</b>
<b>Exceptions &amp; Interrupts</b> Overview of Exceptions and Interrupts, Exception Types, Interrupt Management, Vector Table & Vector Table Relocation, Interrupts Inputs & Pending Behaviours, Exceptions Sequence Overview, Details of NVIC Registers for Interrupt Control, SCB Registers for Exceptions & Interrupt Control, Special Registers for Exceptions Masking, Procedures in Setting up Interrupts, Software Interrupts. Exception Handler in C, Stack Frames, Exception Sequences.			
<b>Unit – V</b>			<b>10 Hrs</b>
<b>Low Power and System Control Features</b> Low Power Designs, Low Power Features, Using WFI & WFE Instructions in for Programming, Developing Low Power Applications, The SysTick Timer, Self-Reset, CPU ID Base Register, Configuration Control Register, Auxiliary Control Registers, Co-Processor Access Control Register.			
<b>OS Support Features</b> Shadowed Stack Pointer, SVC Exception, PendSV Exception, Context Switching in Action, Exclusive Accesses.			
<b>Expected Course Outcomes:</b> After going through this course the student will be able to: CO1. Understand the architecture, instruction set, memory organization and addressing modes of the embedded processors. CO2. Realize real time signal processing applications & primitive OS operations on different ARM architectures by making use of software libraries. CO3. Perform market survey of available embedded processors & arrive at the required processor for			

solving the given problem statement.	
CO4. Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments.	
<b>Reference Books:</b>	
1.	Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3& M4 Processors”, 3 <sup>rd</sup> Edition, Newnes (Elsevier), 2014, ISBN:978-93-5107-175-4
2.	Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developers Guide”, Elsevier, Morgan Kaufman publishers, 2008, ISBN-13:9788181476463
3.	Steve Furber, “ARM System on Chip Architecture”, Pearson Education Limited, 2nd Edition,2000, ISBN-13:9780201675191
4.	Technical reference manual for ARM processor cores, including Cortex M3, M4, M7 processor families.

**Continuous Internal Evaluation (CIE): Total marks: 100****Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100****Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester II</b>						
<b>VLSI DIGITAL SIGNAL PROCESSING SYSTEMS</b> (Group D : Core Elective) (Common to VLSI & ES and CS)						
<b>Course Code</b>	:	<b>18MVE2D3</b>		<b>CIE Marks</b>	:	<b>100</b>
<b>Credits : L:T:P</b>	:	<b>4:0:0</b>		<b>SEE Marks</b>	:	<b>100</b>
<b>Hrs</b>	:	<b>48L</b>		<b>SEE Duration</b>	:	<b>3 Hrs</b>
<b>Unit – I</b>					<b>10Hrs</b>	
<b>Introduction to digital Signal Processing systems</b> Introduction, Typical DSP algorithms, DSP Application demands and scaled CMOS technologies, Representations of DSP algorithms.						
<b>Unit – II</b>					<b>10Hrs</b>	
<b>Pipelining and parallel processing</b> Introduction, Pipelining of FIR Digital filters, parallel processing, pipelining and parallel processing for low power.						
<b>Unit – III</b>					<b>10Hrs</b>	
<b>Algorithmic strength reduction in filters and transforms</b> Introduction, parallel FIR filters, Discrete Cosine transform and inverse DCT, Parallel architectures for Rank-Order Filters.						
<b>Unit – IV</b>					<b>9 Hrs</b>	
<b>Pipelined and parallel Recursive and Adaptive Filters</b> Introduction, Pipeline interleaving in digital Filters, pipelining in 1 <sup>st</sup> order IIR digital filters, Pipelining in higher order IIR Digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low power IIR digital Filter Design using Pipelining and parallel processing, Pipelined Adaptive Digital Filters.						
<b>Unit – V</b>					<b>9 Hrs</b>	
<b>Programmable digital Signal Processor</b> Introduction, evolution of programmable Digital Signal processors, Important feature of DSP processors, DSP Processors for Mobile and wireless communication, Processor for multimedia signal Processing.						
<b>Expected Course Outcomes:</b> After going through this course the student will be able to: CO1: Develop a strong grounding in the fundamentals of VLSI digital signal processing , CO2: Understand DSP architectures and CMOS technologies to describe, analyze, and solve problems in VLSI digital signal processing. CO3: Evaluate and test the modern VLSI digital signal processing systems using simulation tool. CO4: Design suitable algorithm for specific applications & Develop applications using general purpose digital signal processors						
<b>Reference Books:</b>						
1	Keshab K. Parthi , “VLSI Digital Signal processing systems :Design and implementation” Wiley 1999,ISBN: 81-265-1098-6.					
2	Rulph chasseur, “Digital Signal Processing and applications “ with C6713 and C6416 DSK, Wiley 2005.					
3.	Nasser Kehtarnavaz, ” digital Signal Processing System Design: Lab view based hybrid programming,Academic press 2008.					

**Continuous Internal Evaluation (CIE): Total marks: 100**

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.



<b>Semester: II</b>					
<b>BUSINESS ANALYTICS</b>					
<b>(Group G: Global Elective)</b>					
<b>Course Code</b>	<b>:</b>	<b>18CS2G01</b>		<b>CIE Marks</b>	<b>:</b> <b>100</b>
<b>Credits L: T: P</b>	<b>:</b>	<b>3:0:0</b>		<b>SEE Marks</b>	<b>:</b> <b>100</b>
<b>Hours</b>	<b>:</b>	<b>36L</b>		<b>SEE Duration</b>	<b>:</b> <b>3 hrs</b>

**Course Learning Objectives:**

Graduates shall be able to

1. Formulate and solve business problems to support managerial decision making.
2. Explore the concepts, processes needed to develop, report, and analyze business data.
3. Use data mining techniques concepts to identify specific patterns in the data
4. Interpret data appropriately and solve problems from various sectors such as manufacturing, service, retail, software, banking and finance.

<b>Unit – I</b>	
Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling.	<b>07 Hrs</b>
<b>Unit – II</b>	
Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.	<b>07 Hrs</b>
<b>Unit – III</b>	
Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, Predictive Analytics, Predicative Modelling, Predictive analytics analysis.	<b>07 Hrs</b>
<b>Unit – IV</b>	
Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.	<b>08 Hrs</b>
<b>Unit –V</b>	
Decision Analysis: Formulating Decision Problems, Decision Strategies with and without Outcome, Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.	<b>07 Hrs</b>

**Course Outcomes: After going through this course the student will be able to:**

<b>CO1</b>	Explore the concepts, data and models for Business Analytics.
<b>CO2</b>	Analyze various techniques for modelling and prediction.
<b>CO3</b>	Design the clear and actionable insights by translating data.
<b>CO4</b>	Formulate decision problems to solve business applications

<b>Reference Books:</b>	
1	Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Business analytics Principles, Concepts, and Applications FT Press Analytics, 1 <sup>st</sup> Edition, 2014, ISBN-13: 978-0133989403, ISBN-10: 0133989402
2	Evan Stubs , The Value of Business Analytics: Identifying the Path to Profitability, John Wiley & Sons, ISBN:9781118983881  DOI:10.1002/9781118983881,1 <sup>st</sup> edition 2014
3	James Evans, Business Analytics, Pearsons Education 2 <sup>nd</sup> edition, ISBN-13: 978-0321997821 ISBN-10: 0321997824
4	Gary Cokins and Lawrence Maisel, Predictive Business Analytics Forward Looking Capabilities to Improve Business, Wiley; 1 <sup>st</sup> edition, 2013.

#### **Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.

**Total CIE is 20+50+30=100 Marks.**

#### **Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester: II</b>		
<b>INDUSTRIAL AND OCCUPATIONAL HEALTH AND SAFETY</b>		
<b>(Group G :Global Elective)</b>		
<b>Course Code: 18CV 2G 02</b>		<b>CIE Marks:100</b>
<b>Credits : L: T: P : 3:0:0</b>		<b>SEE Marks :100</b>
<b>Hours : 36L</b>		<b>SEE Duration:3Hrs</b>
<b>Course Learning Objectives :</b>		
1	To understand the Industrial and Occupational health and safety and its importance.	
2	To understand the different materials, occupations to which the employee can exposed to.	
3	To know the characteristics of materials and effect on health.	
4	To evaluate the different processes and maintenance required in the industries to avoid accidents.	
<b>UNIT – I</b>		<b>7Hrs</b>
<b>Industrial safety:</b> Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and fire fighting, equipment and methods.		
<b>UNIT – II</b>		<b>7Hrs</b>
<b>Occupational health and safety:</b> Introduction, Health, Occupational health: definition, Interaction between work and health, Health hazards, workplace, economy and sustainable development, Work as a factor in health promotion. Health protection and promotion Activities in the workplace: National governments, Management, Workers, Workers’ representatives and unions, Communities, Occupational health professionals. Potential health hazards: Air contaminants, Chemical hazards, Biological hazards, Physical hazards, Ergonomic hazards, Psychosocial factors, Evaluation of health hazards: Exposure measurement techniques, Interpretation of findings recommended exposure limits. Controlling hazards: Engineering controls, Work practice controls, Administrative controls. Occupational diseases: Definition, Characteristics of occupational diseases, Prevention of occupational diseases.		
<b>UNIT – III</b>		<b>8Hrs</b>
<b>Hazardous Materials characteristics and effects on health:</b> Introduction, Chemical Agents, Organic Liquids, Gases, Metals and Metallic Compounds, Particulates and Fibers, Alkalies and Oxidizers, General Manufacturing Materials, Chemical Substitutes, Allergens, Carcinogens, Mutagens, Reproductive Hazards, Sensitizers and Teratogens, Recommended Chemical Exposure Limits. Physical Agents, Noise and Vibration, Temperature and Pressure, Carcinogenicity, Mutagenicity and Teratogenicity. Ergonomic Stresses: Stress-Related Health Incidents, Eyestrain, Repetitive Motion, Lower Back Pain, Video Display Terminals.		
<b>UNIT – IV</b>		<b>7Hrs</b>
<b>Wear and Corrosion and their prevention:</b> Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.		
<b>UNIT – V</b>		<b>7Hrs</b>
<b>Periodic and preventive maintenance:</b> Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, over hauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.		

<b>Expected Course Outcomes:</b>	
After successful completion of this course the student will be able to:	
CO1	Explain the Industrial and Occupational health and safety and its importance.
CO2	Demonstrate the exposure of different materials, occupational environment to which the employee can expose in the industries.
CO3	Characterize the different type materials, with respect to safety and health hazards of it.
CO4	Analyze the different processes with regards to safety and health and the maintenance required in the industries to avoid accidents.
<b>Reference Books:</b>	
1.	Maintenance Engineering Handbook, Higgins & Morrow, SBN 10: 0070432015 / ISBN 13: 9780070432017, Published by McGraw-Hill Education. Da Information Services.
2.	H. P. Garg, Maintenance Engineering Principles, Practices & Management, 2009, S. Chand and Company, New Delhi, ISBN:9788121926447
3.	Fundamental Principles of Occupational Health and Safety, Benjamin O. ALLI, Second edition, 2008 International Labour Office – Geneva: ILO, ISBN 978-92-2-120454-1
4.	Foundation Engineering Handbook, 2008, Winterkorn, Hans, Chapman & Hall London. ISBN:8788111925428.

**Continuous Internal Evaluation (CIE): Total marks: 100****Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.

**Total CIE is 20+50+30=100 Marks.**

**Semester End Evaluation (SEE): Total marks: 100****Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester: II</b>					
<b>MODELING USING LINEAR PROGRAMMING</b>					
<b>(Group G: Global Elective)</b>					
<b>Course Code</b>	<b>:</b>	<b>18IM2G03</b>		<b>CIE Marks</b>	<b>:</b> <b>100</b>
<b>Credits L: T: P</b>	<b>:</b>	<b>3:0:0</b>		<b>SEE Marks</b>	<b>:</b> <b>100</b>
<b>Hours</b>	<b>:</b>	<b>36L</b>		<b>SEE Duration</b>	<b>:</b> <b>3 hrs</b>

<b>Unit – I</b>	
<b>Linear Programming:</b> Introduction to Linear Programming problem <b>Simplex methods:</b> Variants of Simplex Algorithm – Use of Artificial Variables	<b>07 Hrs</b>
<b>Unit – II</b>	
<b>Advanced Linear Programming :</b> Two Phase simplex techniques, Revised simplex method <b>Duality:</b> Primal-Dual relationships, Economic interpretation of duality	<b>07 Hrs</b>
<b>Unit – III</b>	
<b>Sensitivity Analysis:</b> Graphical sensitivity analysis, Algebraic sensitivity analysis - changes in RHS, Changes in objectives, Post optimal analysis - changes affecting feasibility and optimality	<b>07 Hrs</b>
<b>Unit – IV</b>	
<b>Transportation Problem:</b> Formulation of Transportation Model, Basic Feasible Solution using North-West corner, Least Cost, Vogel's Approximation Method, Optimality Methods, Unbalanced Transportation Problem, Degeneracy in Transportation Problems, Variants in Transportation Problems.	<b>08 Hrs</b>
<b>Unit – V</b>	
<b>Assignment Problem:</b> Formulation of the Assignment problem, solution method of assignment problem-Hungarian Method, Variants in assignment problem, Travelling Salesman Problem (TSP).	<b>07 Hrs</b>

<b>Course Outcomes: After going through this course the student will be able to:</b>	
<b>CO1</b>	Explain the various Linear Programming models and their areas of application.
<b>CO2</b>	Formulate and solve problems using Linear Programming methods.
<b>CO3</b>	Develop models for real life problems using Linear Programming techniques.
<b>CO4</b>	Analyze solutions obtained through Linear Programming techniques.

<b>Reference Books:</b>	
<b>1</b>	Taha H A, Operation Research An Introduction, PHI, 8 <sup>th</sup> Edition, 2009, ISBN: 0130488089.
<b>2</b>	Philips, Ravindran and Solberg - Principles of Operations Research – Theory and Practice, John Wiley & Sons (Asia) Pvt Ltd, 2 <sup>nd</sup> Edition, 2000, ISBN 13: 978-81-265-1256-0
<b>3</b>	Hiller, Liberman, Nag, Basu, Introduction to Operation Research, Tata McGraw Hill 9 <sup>th</sup> Edition, 2012, ISBN 13: 978-0-07-133346-7
<b>4</b>	J K Sharma, Operations Research Theory and Application, Pearson Education Pvt Ltd, 4 <sup>th</sup> Edition, 2009, ISBN 13: 978-0-23-063885-3.

#### **Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester: II</b>					
<b>PROJECT MANAGEMENT</b>					
<b>(Group G: Global Elective)</b>					
<b>Course Code</b>	<b>:</b>	<b>18IM2G04</b>		<b>CIE Marks</b>	<b>:</b> <b>100</b>
<b>Credits L: T: P</b>	<b>:</b>	<b>3:0:0</b>		<b>SEE Marks</b>	<b>:</b> <b>100</b>
<b>Hours</b>	<b>:</b>	<b>36L</b>		<b>SEE Duration</b>	<b>:</b> <b>3 hrs</b>

<b>Unit – I</b>	
<b>Introduction:</b> Project Planning, Need of Project Planning, Project Life Cycle, Roles, Responsibility and Team Work, Project Planning Process, Work Breakdown Structure (WBS), Introduction to Agile Methodology.	<b>07 Hrs</b>
<b>Unit – II</b>	
<b>Capital Budgeting:</b> Capital Investments: Importance and Difficulties, phases of capital budgeting, levels of decision making, facets of project analysis, feasibility study – a schematic diagram, objectives of capital budgeting	<b>07 Hrs</b>
<b>Unit – III</b>	
<b>Project Costing:</b> Cost of Project, Means of Finance, Cost of Production, Working Capital Requirement and its Financing, Profitability Projections, Projected Cash Flow Statement, Projected Balance Sheet, Multi-year Projections, Financial Modeling, Social Cost Benefit Analysis	<b>08 Hrs</b>
<b>Unit – IV</b>	
<b>Tools &amp; Techniques of Project Management:</b> Bar (GANTT) chart, bar chart for combined activities, logic diagrams and networks, Project evaluation and review Techniques (PERT) Critical Path Method (CPM), Computerized project management	<b>07Hrs</b>
<b>Unit-V</b>	
<b>Project Management and Certification:</b> An introduction to SEI, CMMI and project management institute USA – importance of the same for the industry and practitioners. PMBOK 6 - Introduction to Agile Methodology, Themes / Epics / Stories, Implementing Agile. <b>Domain Specific Case Studies on Project Management:</b> Case studies covering project planning, scheduling, use of tools & techniques, performance measurement.	<b>07 Hrs</b>

<b>Course Outcomes: After going through this course the student will be able to:</b>	
CO1	Explain project planning activities that accurately forecast project costs, timelines, and quality.
CO2	Evaluate the budget and cost analysis of project feasibility.
CO3	Analyze the concepts, tools and techniques for managing projects.
CO4	Illustrate project management practices to meet the needs of Domain specific stakeholders from multiple sectors of the economy (i.e. consulting, government, arts, media, and charity organizations).

<b>Reference Books:</b>	
1	Prasanna Chandra, Project Planning Analysis Selection Financing Implementation & Review, Tata McGraw Hill Publication, 8 <sup>th</sup> Edition, 2010, ISBN 0-07-007793-2.
2	Project Management Institute, A Guide to the Project Management Body of Knowledge (PMBOK Guide), 5 <sup>th</sup> Edition, 2013, ISBN: 978-1-935589-67-9
3	Harold Kerzner, Project Management A System approach to Planning Scheduling & Controlling, John Wiley & Sons Inc., 11 <sup>th</sup> Edition, 2013, ISBN 978-1-118-02227-6.
4	Rory Burke, Project Management – Planning and Controlling Techniques, John Wiley & Sons, 4 <sup>th</sup> Edition, 2004, ISBN: 9812-53-121-1

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.



<b>II Semester</b>		
<b>ENERGY MANAGEMENT (Group G: Global Elective)</b>		
<b>Course Code: 18CH2G05</b>		<b>CIE Marks: 100</b>
<b>Credits: L:T:P: 3:0:0</b>		<b>SEE Marks: 100</b>
<b>Hours: 36L</b>		<b>SEE Hrs: 3</b>

**Course Learning Objectives(CLO):**

Students are able to:

1. Explain the importance of energy conservation and energy audit.
2. Understand basic principles of renewable sources of energy and technologies.
3. Outline utilization of renewable energy sources for both domestics and industrial application.
4. Analyse the environmental aspects of renewable energy resources.

<b>Unit-I</b>	<b>08 Hrs</b>
<b>Energy conservation:</b> Principles of energy conservation, Energy audit and types of energy audit, Energy conservation approaches, Cogeneration and types of cogeneration, Heat Exchangers and classification.	
<b>Unit-II</b>	<b>07 Hrs</b>
<b>Wet Biomass Gasifiers:</b> Introduction, Classification of feedstock for biogas generation, Biomass conversion technologies: Wet and dry processes, Photosynthesis, Biogas generation, Factors affecting bio-digestion, Classification of biogas plants, Floating drum plant and fixed dome plant their advantages and disadvantages.	
<b>Unit -III</b>	<b>07 Hrs</b>
<b>Dry Biomass Gasifiers :</b> Biomass energy conversion routes, Thermal gasification of biomass, Classification of gasifiers, Fixed bed systems: Construction and operation of up draught and down draught gasifiers.	
<b>Unit -IV</b>	<b>07 Hrs</b>
<b>Solar Photovoltaic:</b> Principle of photovoltaic conversion of solar energy, Types of solar cells and fabrication. <b>Wind Energy:</b> Classification, Factors influencing wind, WECS & classification.	
<b>Unit -V</b>	<b>07 Hrs</b>
<b>Alternative liquid fuels:</b> Introduction, Ethanol production: Raw materials, Pre-treatment, Conversion processes with detailed flow sheet. Gasification of wood: Detailed process, Gas purification and shift conversion, Biofuel from water hyacinth.	

**Course outcomes (CO):**

On completion of the course, the student should have acquired the ability to	
CO1: Understand the use alternate fuels for energy conversion	
CO2: Develop a scheme for energy audit	
CO3: Evaluate the factors affecting biomass energy conversion	
CO4: Design a biogas plant for wet and dry feed	
<b>Reference Books:</b>	
1	Nonconventional energy, Ashok V Desai, 5 <sup>th</sup> Edition, 2011, New Age International (P) Limited, ISBN 13: 9788122402070.
2	Biogas Technology - A Practical Hand Book, Khandelwal K C and Mahdi S S, Vol. I & II, 1986, McGraw-Hill Education, ISBN-13: 978-0074517239.
3	Biomass Conversion and Technology, Charles Y Wereko-Brobby and Essel B Hagan, 1 <sup>st</sup> Edition, 1996, John Wiley & Sons, ISBN-13: 978-0471962465.
4	Solar Photovoltaics: Fundamental Applications and Technologies, C. S. Solanki, 2 <sup>nd</sup> Edition, 2009, Prentice Hall of India, ISBN:9788120343863.

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks):**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/ field work 4) mini project.

**Total CIE is 20+50+30 = 100 marks.**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester: II</b>						
<b>INDUSTRY 4.0</b>						
<b>(Group G: Global Elective)</b>						
<b>Course Code</b>	<b>:</b>	<b>18ME2G06</b>		<b>CIE Marks</b>	<b>:</b>	<b>100</b>
<b>Credits L: T: P</b>	<b>:</b>	<b>3:0:0</b>		<b>SEE Marks</b>	<b>:</b>	<b>100</b>
<b>Hours</b>	<b>:</b>	<b>36L</b>		<b>SEE Duration</b>	<b>:</b>	<b>3 hrs</b>

<b>Unit – I</b>	
<b>Introduction:</b> Industrial, Internet, Case studies, Cloud and Fog, M2M Learning and Artificial Intelligence, AR, Industrial Internet Architecture Framework (IIAF), Data Management.	<b>07 Hrs</b>
<b>Unit – II</b>	
<b>The Concept of the IIoT:</b> Modern Communication Protocols, Wireless Communication Technologies, Proximity Network Communication Protocols, TCP/IP, API: A Technical Perspective, Middleware Architecture.	<b>07 Hrs</b>
<b>Unit – III</b>	
<b>Data Analytics in Manufacturing:</b> Introduction, Power Consumption in manufacturing, Anomaly Detection in Air Conditioning, Smart Remote Machinery Maintenance Systems with Komatsu, Quality Prediction in Steel Manufacturing. Internet of Things and New Value Proposition, Introduction, Internet of Things Examples, IoTs Value Creation Barriers: Standards, Security and Privacy Concerns. Advances in Robotics in the Era of Industry 4.0, Introduction, Recent Technological Components of Robots, Advanced Sensor Technologies, Artificial Intelligence, Internet of Robotic Things, Cloud Robotics.	<b>08 Hrs</b>
<b>Unit – IV</b>	
<b>Additive Manufacturing Technologies and Applications:</b> Introduction, Additive Manufacturing (AM) Technologies, Stereo lithography, 3DP, Fused Deposition Modeling, Selective Laser Sintering, Laminated Object Manufacturing, Laser Engineered Net Shaping, Advantages of Additive Manufacturing, Disadvantages of Additive Manufacturing. Advances in Virtual Factory Research and Applications, The State of Art, The Virtual Factory Software , Limitations of the Commercial Software	<b>07 Hrs</b>
<b>Unit –V</b>	
<b>Augmented Reality:</b> The Role of Augmented Reality in the Age of Industry 4.0, Introduction, AR Hardware and Software Technology, Industrial Applications of AR, Maintenance , Assembly, Collaborative Operations , Training. Smart Factories: Introduction, Smart factories in action, Importance, Real world smart factories, The way forward. A Roadmap: Digital Transformation, Transforming Operational Processes, Business Models, Increase Operational Efficiency, Develop New Business Models.	<b>07 Hrs</b>

<b>Course Outcomes: After going through this course the student will be able to:</b>	
<b>CO1</b>	Understand the opportunities, challenges brought about by Industry 4.0 for benefits of organizations and individuals
<b>CO2</b>	Analyze the effectiveness of Smart Factories, Smart cities, Smart products and Smart services
<b>CO3</b>	Apply the Industrial 4.0 concepts in a manufacturing plant to improve productivity and profits
<b>CO4</b>	Evaluate the effectiveness of Cloud Computing in a networked economy

<b>Reference Books:</b>	
1	Alasdair Gilchrist, INDUSTRY 4.0 THE INDUSTRIAL INTERNET OF THINGS, Apress Publisher, ISBN-13 (pbk): 978-1-4842-2046-7
2	Alp Ustundag, Emre Cevikcan, Industry 4.0: Managing The Digital Transformation, Springer, 2018 ISBN 978-3-319-57869-9.
3	Ovidiu Vermesan and Peer Friess, Designing the industry - Internet of things connecting the physical, digital and virtual worlds, Rivers Publishers, 2016 ISBN 978-87-93379-81-7
4	Christoph Jan Bartodziej, The concept Industry 4.0- An Empirical Analysis of Technologies and Applications in Production Logistics, Springer Gabler, 2017 ISBN 978-3-6581-6502-4.

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Semester: II						
ADVANCED MATERIALS (Group G: Global Elective)						
Course Code	:	18ME2G07		CIE Marks	:	100
Credits L: T: P	:	3:0:0		SEE Marks	:	100
Hours	:	36L		SEE Duration	:	3 hrs

Unit – I	
<b>Classification and Selection of Materials:</b> Classification of materials. Properties required in Engineering materials, Criteria of selection of materials. Requirements / needs of advance materials.	<b>07 Hrs</b>
Unit – II	
<b>Non Metallic Materials:</b> Classification of non metallic materials, Rubber : Properties, processing and applications. Plastics : Thermosetting and Thermoplastics, Applications and properties. Ceramics : Properties and applications. Adhesives: Properties and applications. Optical fibers : Properties and applications. Composites : Properties and applications.	<b>07 Hrs</b>
Unit – III	
<b>High Strength Materials:</b> Methods of strengthening of alloys, Materials available for high strength applications, Properties required for high strength materials, Applications of high strength materials	<b>08 Hrs</b>
Unit – IV	
<b>Low &amp; High Temperature Materials</b> Properties required for low temperature applications, Materials available for low temperature applications, Requirements of materials for high temperature applications, Materials available for high temperature applications, Applications of low and high temperature materials.	<b>07 Hrs</b>
Unit –V	
<b>Nanomaterials:</b> Definition, Types of nanomaterials including carbon nanotubes and nanocomposites, Physical and mechanical properties, Applications of nanomaterials	<b>07 Hrs</b>

Course Outcomes: After going through this course the student will be able to:	
<b>CO1</b>	Describe metallic and non metallic materials
<b>CO2</b>	Explain preparation of high strength Materials
<b>CO3</b>	Integrate knowledge of different types of advanced engineering Materials
<b>CO4</b>	Analyse problem and find appropriate solution for use of materials.

Reference Books:	
1	Donald R. Askeland, and Pradeep P. Fulay, The Science & Engineering of Materials, 5th Edition, Thomson, 2006, ISBN-13-978-0534553968
2	Gregory L. Timp, Nanotechnology 1999th Editionmm Springer, 1999 ISBN-13: 978-0387983349
3	Dr. VD Kodgire and Dr. S V Kodgire, Material Science and Metallurgym 42nd Edition 2018, Everest Publishing House ISBN NO: 81 86314 00 8
4	N Bhatnagar, T S Srivatsan, Processing and Fabrication of Advanced Materials, 2008, IK International, ISBN: 978819077702

### Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>Semester: II</b>	
<b>COMPOSITE MATERIALS SCIENCE AND ENGINEERING</b> (Common to AS, BT, CH, CV, IM, ME)	
<b>Course Code:</b> 18CHY2G08	<b>CIE Marks:</b> 100
<b>Credits: L:T:P:S:</b> 3:1:0:0	<b>SEE Marks:</b> 100
<b>Hours:</b> 36L +12T	<b>SEE Duration:</b> 3Hrs
<b>Course Learning Objectives:</b>	
<b>1</b>	Understand the properties of composite materials.
<b>2</b>	Apply the basic concepts of Chemistry to develop futuristic composite materials for high-tech applications in the area of Engineering.
<b>3</b>	Impart knowledge in the different fields of material chemistry so as to apply it to the problems in engineering field.
<b>4</b>	Develop analytical capabilities of students so that they can characterize, transform and use materials in engineering and apply knowledge gained in solving related engineering problems.
<b>Unit-I</b>	
<b>Introduction to composite materials</b> Fundamentals of composites – need for composites – Enhancement of properties – Classification based on matrix- Polymer matrix composites (PMC), Metal matrix composites (MMC), Ceramic matrix composites (CMC) – Constituents of composites, Interfaces and Interphases, Distribution of constituents, Types of Reinforcements, Particle reinforced composites, Fibre reinforced composites. Fiber production techniques for glass, carbon and ceramic fibers Applications of various types of composites.	<b>07 Hrs</b>
<b>Unit – II</b>	
<b>Polymer matrix composites ( PMC)</b> Polymer resins – Thermosetting resins, Thermoplastic resins & Elastomers, Reinforcement fibres-Types, Rovings, Woven fabrics. PMC processes – Hand Layup Processes, Spray up processes – Compression Moulding – Injection Moulding – Resin Transfer Moulding – Pultrusion – Filament winding – Injection moulding. Glass fibre and carbon fibre reinforced composites (GFRP & CFRP). Laminates- Balanced Laminates, Symmetric Laminates, Angle Ply Laminates, Cross Ply Laminates. Mechanical Testing of PMC- Tensile Strength, Flexural Strength, ILSS, Impact Strength- As per ASTM Standard. Applications of PMC in aerospace, automotive industries.	<b>08 Hrs</b>
<b>Unit -III</b>	
<b>Ceramic matrix composites and special composites</b> Engineering ceramic materials – properties – advantages – limitations – monolithic ceramics – need for CMC – ceramic matrix – various types of ceramic matrix composites- oxide ceramics – non oxide ceramics – Aluminium oxide – silicon nitride – reinforcements – particles- fibres- whiskers. Sintering – Hot pressing – Cold Isostatic Pressing (CIPing) – Hot isostatic pressing (HIPing). Applications of CMC in aerospace, automotive industries- Carbon /carbon composites – advantages of carbon matrix – limitations of carbon matrix carbon fibre – chemical vapour deposition of carbon on carbon fibre perform. Sol-gel technique- Processing of Ceramic Matrix composites.	<b>07 Hrs</b>
<b>Unit –IV</b>	
<b>Metal matrix composites</b> Characteristics of MMC, various types of metal matrix composites alloy vs. MMC, advantages of MMC, limitations of MMC, Reinforcements – particles – fibres. Effect of reinforcement – volume fraction – rule of mixtures. Processing of MMC – powder metallurgy process – diffusion bonding – stir casting – squeeze casting, a spray process, Liquid infiltration In-situ reactions-Interface-measurement of interface properties- applications of MMC in aerospace, automotive industries.	<b>07 Hrs</b>
<b>Unit –V</b>	
<b>Polymer nano composites</b> Introduction and Significance of polymer Nano composites. Intercalated And Exfoliated Nanocomposites. Classification of Nano fillers- nanolayers, nanotubes, nanoparticles.	<b>07 Hrs</b>

Preparation of Polymer Nano composites by Solution, In-situ Polymerization and melt mixing techniques. Characterization Of polymer nanocomposites- XRD, TEM, SEM and AFM. Mechanical and Rheological properties of Polymer Nano composites. Gas barrier, Chemical-Resistance, Thermal and Flame retardant properties of polymer nanocomposites. Optical properties and Biodegradability studies of Polymer nanocomposites, Applications of polymer nano-composites.	
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<b>Course Outcomes: After completing the course, the students will be able to</b>	
<b>CO1:</b>	Understand the purpose and the ways to develop new materials upon proper combination of known materials.
<b>CO2:</b>	Identify the basic constituents of a composite materials and list the choice of materials available
<b>CO3:</b>	Will be capable of comparing/evaluating the relative merits of using alternatives for important engineering and other applications.
<b>CO4:</b>	Get insight to the possibility of replacing the existing macro materials with nano-materials.

<b>Reference Books</b>	
<b>1</b>	Composite Materials Science and Engineering, Krishan K Chawla, 3 <sup>rd</sup> Edition Springer-verlag Gmbh, , ISBN: 9780387743646, 0387743642
<b>2</b>	The Science and Engineering of Materials, K Balani, Donald R Askeland,6 <sup>th</sup> Edition-Cengage, Publishers, ISBN: 9788131516416
<b>3</b>	Polymer Science and Technology, Joel R Fried , 2 <sup>nd</sup> Edition, Prentice Hall, ISBN: 9780137039555
<b>4</b>	Nanomaterials and nanocomposites, Rajendra Kumar Goyal , 2 <sup>nd</sup> Edition, CRC Press-Taylor & Francis, ISBN: 9781498761666, 1498761666

#### **Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.

**Total CIE is 20+50+30=100 Marks.**

#### **Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.



<b>Semester : II</b>		
<b>PHYSICS OF MATERIALS</b> <b>(Group G: Global Elective)</b>		
<b>Course Code: 18PHY2G09</b>		<b>CIE Marks: 100</b>
<b>Credits: L:T:P:: 3:0:0</b>		<b>SEE Marks: 100</b>
<b>Hours: 36</b>		<b>SEE Duration: 3Hrs</b>

<b>Course Learning Objectives (CLO):</b>
<p>Student are able to</p> <ol style="list-style-type: none"> <li>1. Classify the crystals based on lattice parameters.</li> <li>2. Explain the behavior of Dielectrics with change in frequency.</li> <li>3. Classify the magnetic materials based on Quantum theory as well understand superconductors.</li> <li>4. Explain direct and indirect bandgap semiconductors, polymer semiconductors and Photoconductive polymers.</li> <li>5. Describe the behavior of Smart materials and its phases and apply to Engineering applications.</li> </ol>

<b>Unit-I</b>	<b>07 Hrs</b>
<b>Crystal Structure :</b> Symmetry elements-seven crystals systems-Reciprocal lattice-Packing fraction, Lattice Vibration-Brillouin zones, Analysis of Crystal structure using XRD, Thermal properties.	
<b>Unit-II</b>	<b>07 Hrs</b>
<b>Dielectric Materials:</b> Basic concepts-Langevin's Theory of Polarisation-Clausius-Mossotti Relation-Ferro electricity-Piezoelectricity-Properties of Dielectric in alternating fields-The complex Dielectric Constant and Dielectric Loss, Polarizability as a function of frequency-Complex dielectric constant of non-polar solids-Dipolar relaxation, Applications.	
<b>Unit -III</b>	<b>07Hrs</b>
<b>Magnetic Materials :</b> Dia and Paramagnetic materials-Quantum theory of paramagnetic materials-Paramagnetic susceptibility of conduction electrons-Ferro-anti ferromagnetic materials-Superconductors and Applications..	
<b>Unit -IV</b>	<b>07 Hrs</b>
<b>Semiconducting Materials</b> Semiconductor-Direct and Indirect bonding characteristics-Importance of Quantum confinement-quantum wires and dots-Ferro electric semiconductors-applications-Polymer semiconductors-Photo conductive polymers, Applications.	
<b>Unit -V</b>	<b>08 Hrs</b>
<b>Novel Materials</b> Smart materials-shape memory alloys-shape memory effects-Martensitia Transformation functional properties-processing-texture and its nature.	

<b>Reference Books:</b>	
1.	Solid State Physics, S O Pillai, 6 <sup>th</sup> Edition, New Age International Publishers, ISBN 10-8122436978.
2.	Introduction to Solid State Physics, C.Kittel, 7 <sup>th</sup> Edition, 2003, John Wiley & Sons, ISBN 9971-51-180.
3.	Material Science, Rajendran V and Marikani, 1 <sup>st</sup> Edition, Tata McGraw Hill, ISBN 10-0071328971.
4.	The Science and Engineering of Materials, Askeland, Fulay, Wright, Balanai, 6 <sup>th</sup> Edition, Cengage Learning, ISBN-13:978-0-495-66802-2.

<b>Course Outcomes (CO's):</b>
CO1: Analyse crystals using XRD technique. CO2: Explain Dielectric and magnetic materials. CO3: Integrate knowledge of various types of advanced engineering Materials. CO4: Use materials for novel applications.

**Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks):**

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/ field work 4) mini project.

**Total CIE is 20+50+30 = 100 marks.**

**Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

<b>II Semester</b>		
<b>ADVANCED STATISTICAL METHODS</b> (Global Elective)		
<b>Course Code: 18MAT2G10</b>		<b>CIE Marks: 100</b>
<b>Credits: L:T:P:: 3:0:0</b>		<b>SEE Marks: 100</b>
<b>Hours: 36</b>		<b>SEE Duration: 3Hrs</b>

<b>Course Learning Objectives (CLO):</b>
Students are able to:
1. Adequate exposure to learn sampling techniques, random phenomena for analyzing data for solving real world problems.
2. To learn fundamentals of estimation and problems used in various fields of engineering and science.
3. Explore the fundamental principles of statistical inference and tests of hypothesis.
4. Apply the concepts of regression and statistical models to solve the problems of engineering applications.

<b>Unit-I</b>	<b>07 Hrs</b>
<b>Sampling Techniques:</b> Random numbers, Concepts of random sampling from finite and infinite populations, Simple random sampling (with replacement and without replacement). Expectation and standard error of sample mean and proportion.	
<b>Unit-II</b>	<b>07 Hrs</b>
<b>Estimation:</b> Point estimation, Estimator and estimate, Criteria for good estimates - unbiasedness, consistency, efficiency and sufficiency, Method of moment's estimation and maximum likelihood estimation, Properties of maximum likelihood estimator (no proofs), Confidence intervals-population mean (large sample), population proportion.	
<b>Unit -III</b>	<b>07Hrs</b>
<b>Tests of Hypothesis:</b> Principles of Statistical Inference, Formulation of the problems with examples, Simple and composite hypothesis, Null and alternative hypothesis, Tests - type I and type II error, Testing of mean and variance of normal population (one sample and two samples), Chi squared test for goodness of fit.	
<b>Unit -IV</b>	<b>07 Hrs</b>
<b>Linear Statistical Models:</b> Definition of linear model and types, One way ANOVA and two way ANOVA models-one observation per cell, multiple but equal number of observation per cell.	
<b>Unit -V</b>	<b>08 Hrs</b>
<b>Linear Regression:</b> Simple linear regression, Estimation of parameters, Properties of least square estimators, Estimation of error variance, Multivariate data, Multiple linear regressions, Multiple and partial correlation, Autocorrelation-introduction and plausibility of serial dependence, sources of autocorrelation, Durbin-Watson test for auto correlated variables.	

<b>Reference Books:</b>	
1	Fundamentals of Statistics (Vol. I and Vol. II), A. M. Goon, M. K. Gupta and B. Dasgupta, 3 <sup>rd</sup> Edition, 1968, World Press Private Limited, ISBN-13: 978-8187567806.
2	Applied Statistics and Probability for Engineers, John Wiley & Sons, Inc., 3 <sup>rd</sup> Edition, 2003, ISBN 0-471-20454-4.
3	S.C. Gupta, V.K. Kapoor, Fundamentals of Mathematical Statistic, D. C. Montgomery and G. C. Runger, 10 <sup>th</sup> Edition, 2000, A Modern Approach, S Chand Publications, ISBN 81-7014-791-3.
4	Regression Analysis: Concepts and Applications , F. A. Graybill and H. K. Iyer, Belmont, Calif, 1994, Duxbury Press, ISBN-13: 978-0534198695.

<b>Course outcomes (CO's):</b>
<p>On completion of the course, the student should have acquired the ability to</p> <p>CO1: Identify and interpret the fundamental concepts of sampling techniques, estimates and types, hypothesis, linear statistical models and linear regression arising in various fields engineering.</p> <p>CO2: Apply the knowledge and skills of simple random sampling, estimation, null and alternative hypotheses, errors, one way ANOVA, linear and multiple linear regressions.</p> <p>CO3: Analyze the physical problem to establish statistical/mathematical model and use appropriate statistical methods to solve and optimize the solution.</p> <p>CO4: Distinguish the overall mathematical knowledge gained to demonstrate the problems of sampling techniques, estimation, tests of hypothesis, regression and statistical model arising in many practical situations.</p>

#### **Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks):**

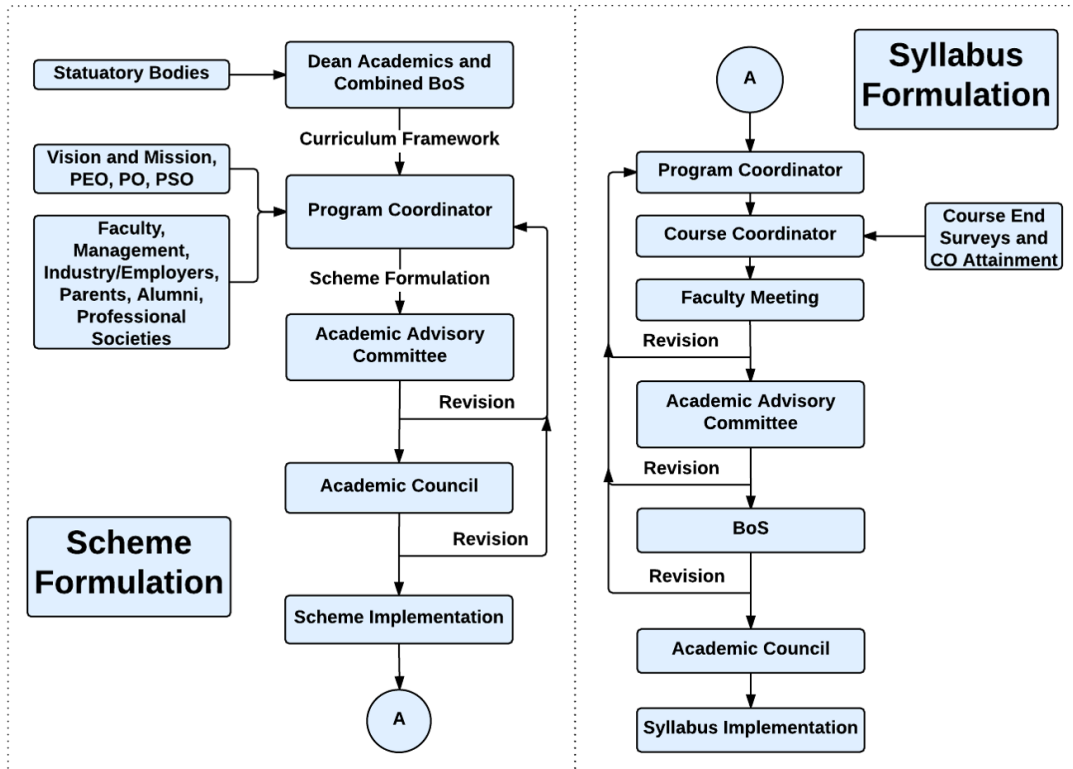
CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/ field work 4) mini project.

**Total CIE is 20+50+30 = 100 marks.**

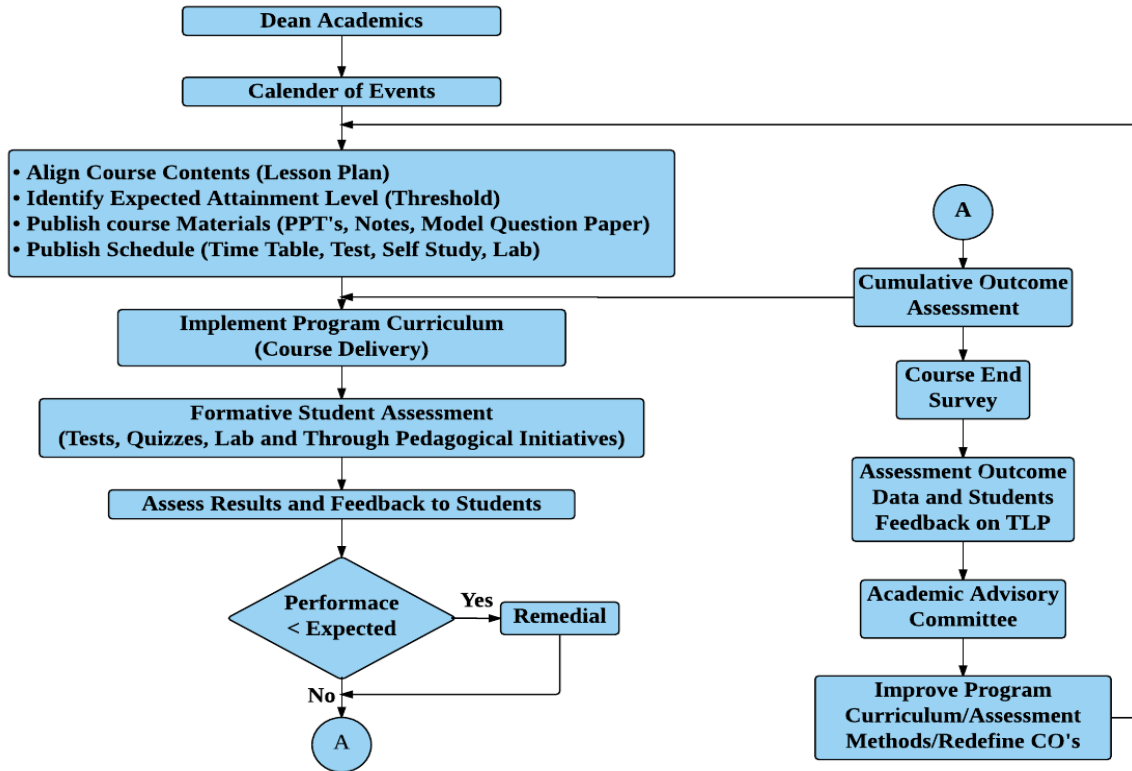
#### **Scheme of Semester End Examination (SEE) for 100 marks:**

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

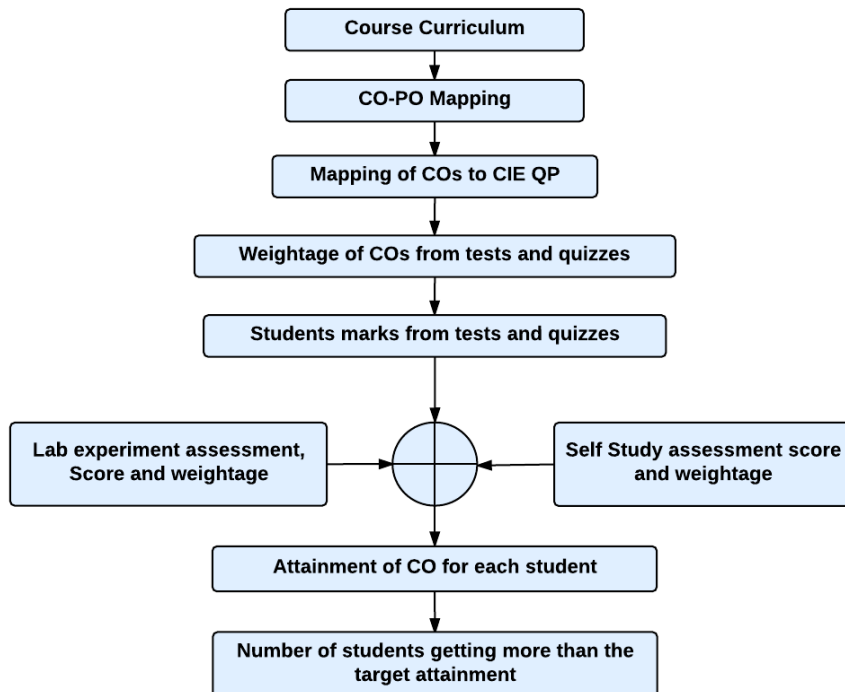
## Curriculum Design Process



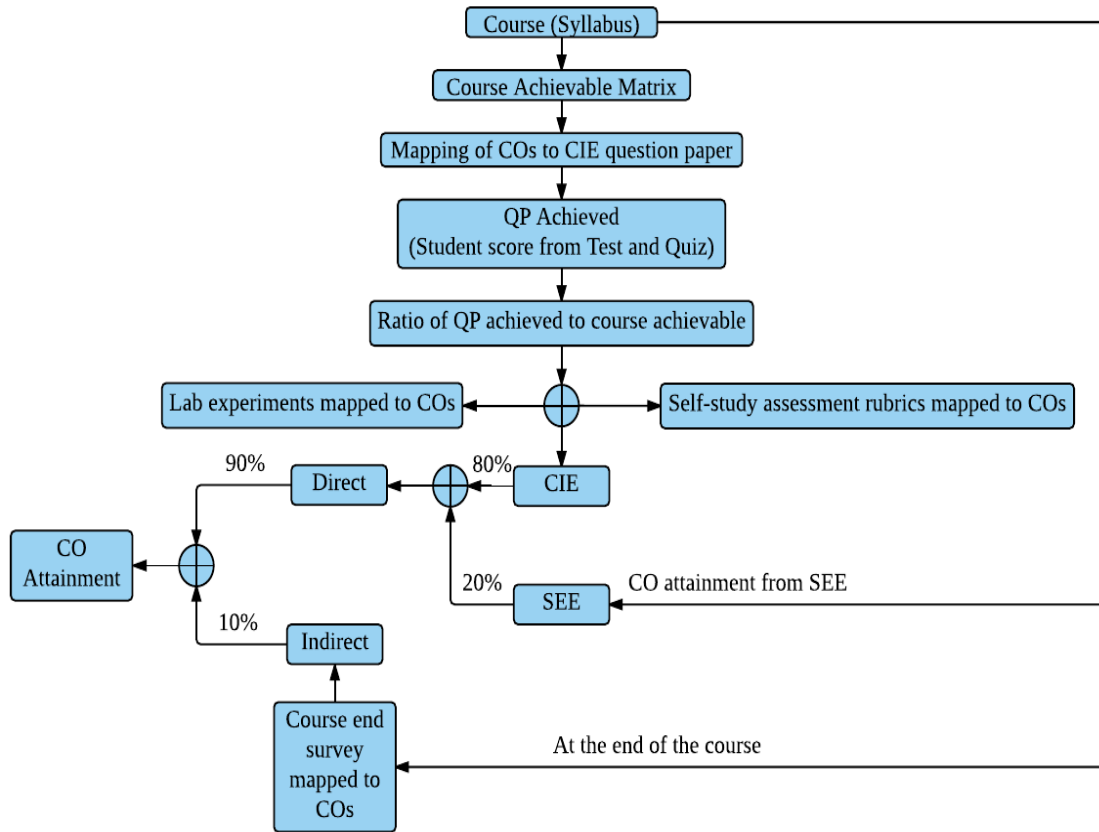
## Academic Planning And Implementation



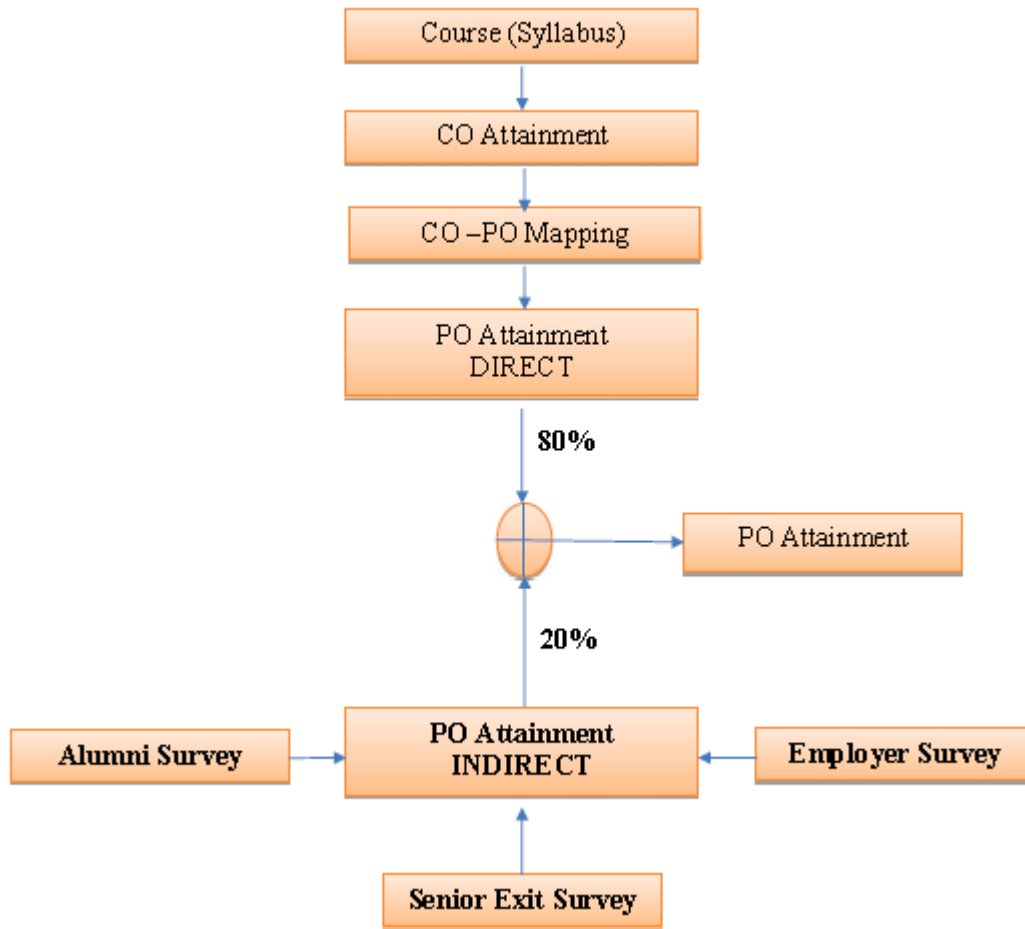
### Process For Course Outcome Attainment



### Final CO Attainment Process



### Program Outcome Attainment Process





**PROGRAM OUTCOMES (PO)**

M. Tech. in VLSI Design and Embedded Systems Program graduates will be able to:

PO1: Independently carry out research /investigation and development work to solve practical problems related to VLSI Design & Embedded Systems

PO2: Write and present a substantial technical report/document in the field of VLSI Design & Embedded Systems

PO3: Demonstrate a degree of mastery over the areas of VLSI Design & Embedded Systems. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.

PO4: Conceptualize and solve VLSI design and Embedded system problems and propose optimal solutions.

PO5: Analyze, learn and apply appropriate techniques, resources and modern engineering/IT tools in core and allied areas.

PO6: Acquire professional and intellectual integrity and ethics of research and execute projects efficiently.