RV COLLEGE OF ENGINEERING®

(Autonomous Institution Affiliated to VTU, Belagavi)
R.V. Vidyaniketan Post, Mysore Road
Bengaluru – 560 059

Scheme and Syllabus of III & IV Semesters
(Autonomous System of 2018 Scheme)

Master of Technology (M.Tech)
in
VLSI DESIGN & EMBEDDED SYSTEMS

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

ABBREVIATIONS

Sl. No.	Abbreviation	Meaning
1.	VTU	Visvesvaraya Technological University
2.	BS	Basic Sciences
3.	CIE	Continuous Internal Evaluation
4.	SEE	Semester End Examination
5.	CE	Professional Core Elective
6.	GE	Global Elective
7.	HSS	Humanities and Social Sciences
8.	CV	Civil Engineering
9.	ME	Mechanical Engineering
10.	EE	Electrical & Electronics Engineering
11.	EC	Electronics & Communication Engineering
12.	IM	Industrial Engineering & Management
13.	EI	Electronics & Instrumentation Engineering
14.	CH	Chemical Engineering
15.	CS	Computer Science & Engineering
16.	TE	Telecommunication Engineering
17.	IS	Information Science & Engineering
18.	BT	Biotechnology
19.	AS	Aerospace Engineering
20.	PHY	Physics
21.	CHY	Chemistry
22.	MAT	Mathematics
23.	MCS	Communication Systems
24.	MVE	VLSI Design & Embedded Systems

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M.Tech in VLSI DESIGN & EMBEDDED SYSTEMS

THIRD SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Total Credits**
1	18MVE31	Synthesis & Optimization of Digital Circuits	EC	4	1	0	**5**
2	18MVE3EX	Elective -E	EC	4	0	0	**4**
3	18MVE33	Internship	EC	0	0	5	**5**
4	18MVE34	Dissertation Phase I	EC	0	0	5	**5**
Total number of Credits				**8**	**1**	**10**	**19**
Total Number of Hours / Week				**8**	**2**	**20**	**30**

FOURTH SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Total Credits**
1	18MVE41	Dissertation Phase II	EC	0	0	20	20
2	18MVE42	Technical Seminar	EC	0	0	2	2
Total number of Credits				**0**	**0**	**22**	**22**
Total Number of Hours / Week						**22**	**22**

III Semester		
GROUP E: CORE ELECTIVES		
Sl. No.	**Course Code**	**Course Title**
1.	18MVE3E1	Radio Frequency IC Design
2.	18MVE3E2	ARM Programming and Optimization
3.	18MVE3E3	Static Timing Analysis

Semester: III						
SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS (Theory)						
Course Code	**:**	18MVE31		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	4:1:0		**SEE**	**:**	**100 Marks**
Total Hours	**:**	50L+26T		**SEE Duration**	**:**	**03 Hours**

Unit-I	**10 Hrs**
Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization. **Graphs**: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.	
Unit – II	**10 Hrs**
Schedule Algorithms: A model for scheduling problems, Scheduling wither source and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. **Hardware Modeling**: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, dataflow and sequencing graphs, compilation and optimization techniques.	
Unit –III	**10 Hrs**
Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.	
Unit –IV	**10 Hrs**
Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.	
Unit –V	**10 Hrs**
Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models. **Cell Library Binding**: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table FPGAs and Anti fuse based FPGAs), rule based library binding.	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Understand and apply the various algorithms and graphs to synthesis and optimization of different digital circuit.
CO2:	Analyze the performance of standard algorithm used for synthesis and optimization of two level, multiple level and sequential logic circuits
CO3:	Demonstrate the improvement of optimization techniques used for digital circuits
CO4:	Develop an algorithm for synthesis and optimization

Reference Books	
1	Giovanni De Micheli, “Synthesis and Optimization of Digital Circuits”, Tata McGraw-Hill, 2003.
2	SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer, “Logic Synthesis”, McGraw-Hill, USA, 1994.
3	NeilWeste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, 2nd edition, Pearson Education (Asia) Pte.Ltd., 2000.

Continuous Internal Evaluation (CIE): Total marks: 100

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.

Total CIE is 20+50+30=100 Marks.

Semester End Evaluation (SEE): Total marks: 100

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Semester: III						
RADIO FREQUENCY IC DESIGN (Theory)						
Course Code	**:**	18MVE3E1		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	4:0:0		**SEE**	**:**	**100 Marks**
Total Hours	**:**	52L		**SEE Duration**	**:**	**03 Hours**

Unit-I	**10 Hrs**
Basic concepts in RF design - Nonlinearity and Time Variance, Effects of nonlinearity – harmonic distortion, gain compression, desensitization, cross modulation, intermodulation, cascaded nonlinear stages – level diagram. Noise in RF circuits – Noise figure, Noise figure of cascaded and lossy circuits, Sensitivity and dynamic range.	
Unit – II	**10 Hrs**
RF Systems Design - Receiver architectures - Heterodyne - dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, Image Reject – Hartley architecture, Transmitter architectures - Direct conversion and two-step transmitters.	
Unit –III	**11 Hrs**
RF Circuits Design (MOSFET circuits only) **Low noise Amplifier -** Performance parameters, Problem of Input matching, LNA topologies – Variants of common source only, design examples. **Mixer -** Mixer fundamentals, Performance parameters, Nonlinear systems as linear mixers, two port example –square law mixers, multiplier based mixers – Single balanced and double balanced (active and passive) - working and implementation, (MOSFET circuits only).	
Unit –IV	**11 Hrs**
Oscillator - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, VCO characteristics, Phase noise – basic concepts and effects of phase noise (no analysis). **Phase Locked Loop Design -** Type-II PLL: design equations, phase margin, and closed-loop PLL response, Design methodology for a Type-II 3rd –order PLL, charge pump design issues, Charge Pump design techniques: charge-injection, clock feed-through.	
Unit –V	**10 Hrs**
Frequency Synthesizers: General considerations, Basic Integer N synthesizer, settling behavior, spur reduction techniques, PLL based modulation, Divider design – Pulse swallow divider, dual modulus divider, divider logic styles – current steering, CML latch, true single phase clocking. Fractional N synthesizers- basic concepts only.	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Apply the knowledge of RF circuits & systems in IC design
CO2:	Analyze CMOS circuits and its impact on Radio frequency IC design.
CO3:	Design and implement RF transceiver chain with specification.
CO4:	Evaluate the different performance parameters used in RF design using CAD tools.

Reference Books	
1	RF Microelectronics , Behzad Razavi, 2nd Edition Pearson Education, 2012
2	"Radio Frequency Integrated Circuits Design", John Rogers ,Calvin Plett, Artech House, 2003
3	The Design of CMOS Radio Frequency Integrated Circuits",Thomas H Lee , "2nd Edition, Cambridge University Press, 2004
4	"VLSI for Wireless Communications", Bosco Leung, Pearson Education, 2004

Continuous Internal Evaluation (CIE): Total marks: 100

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.

Total CIE is 20+50+30=100 Marks.

Semester End Evaluation (SEE): Total marks: 100

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Semester: III						
ARM PROGRAMMING AND OPTIMIZATION (Theory)						
Course Code	**:**	18MVE3E2		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	4:0:0		**SEE**	**:**	**100 Marks**
Total Hours	**:**	50L		**SEE Duration**	**:**	**03 Hours**

Unit-I	**10 Hrs**
Introduction, Data Path Architecture, Registers, Modes, Exceptions **Programming in C for ARM** Overview of C Compilers and optimization, basic C data types, C looping structures, register allocation, function calls, pointer aliasing, structure arrangement, bit fields, unaligned Data and Endianess, division, floating point, inline functions and inline assembly, portability issues.	
Unit – II	**10 Hrs**
Writing and Optimizing ARM Assembly Code Writing assembly code, profiling and cycle counting, instruction scheduling, register allocation, conditional execution, looping constructs, Bit manipulation, efficient switches. Handling unaligned data.	
Unit –III	**10 Hrs**
Digital Signal Processing on ARM Representing a digital signal, Introduction to DSP on the ARM, FIR filters: Realization of filters on ARM7 and Cortex M3, IIR Filters: Realization of filters on ARM7 and Cortex M3, CMSIS DSP Library.	
Unit –IV	**10 Hrs**
Firmware : Firmware and Boot loader **Embedded Operating Systems :** Fundamental Components, Simple Operating System.	
Unit –V	**10 Hrs**
Memory Protection Unit Over view of the MPU's, MPU registers, setting up the MPU, Memory barrier and memory configuration, Using sub-region disable, Consideration when using MPU, Other usages of MPU.	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Describe the programmer's model of ARM processor and analyse the instruction set architecture to realize complex operations.
CO2:	Apply the optimization methods available for ARM architectures to design embedded software to meet given constraints with the help of modern engineering tools.
CO3:	Realize real time signal processing applications & primitive OS operations on different ARM architectures by making use of software libraries.
CO4:	Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments.

Reference Books	
1	ARM System Developers Guide, Andrew N Sloss, Dominic Symes, Chris Wright, Elsevier, Morgan Kaufman publishers, 2008, ISBN-13:9788181476463
2	The definitive Guide to the ARM Cortex- M3 & M4 Processors ,Joseph Yiu, 3rd Edition, Newnes (Elsevier), 2014, ISBN: 978-93-5107-175-4
3	ARM System on Chip Architecture, Steve Furber, Pearson Education Limited,2nd Edition, ISBN-13:9780201675191
4	Technical reference manual for ARM processor cores, including Cortex M series, ARM 11, ARM 9 & ARM 7 processor families.
5	User guides and reference manuals for ARM software development and modeling tools.

Continuous Internal Evaluation (CIE): Total marks: 100

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.
Total CIE is 20+50+30=100 Marks.

Semester End Evaluation (SEE): Total marks: 100
Scheme of Semester End Examination (SEE) for 100 marks:
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Semester: III						
STATIC TIMING ANALYSIS (Theory)						
Course Code	**:**	18MVE3E3		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	4:0:0		**SEE**	**:**	**100 Marks**
Total Hours	**:**	52L		**SEE Duration**	**:**	**03 Hours**

Unit-I	**11 Hrs**
Introduction: Basics of timing concepts- Propagation delay, slew, timing arcs, min and max timing paths, clock domains. **Delay Concepts for Digital Designing:** Types of Delays in Digital Circuits, Different Cause for Delay **Timing parameters of digital circuits:** Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design,Clock Concepts **The STA Environment**- timing path groups, modeling of external attributes, virtual clocks, refining the timing analysis, point-to-point specification	
Unit – II	**10 Hrs**
Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitics, Interconnects, Parasitic Extraction Formats, linear v/s. non-linear delay model. **Clock Network Optimization**: Metrics, clock skew-scheduling, handling variability. **Parallel Timing Optimization**: Circuit partitioning for independent timing regions. **Post-Silicon Timing Validation**: Introduction, sources of post-silicon timing failure, post-silicon tuning	
Unit –III	**10 Hrs**
Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design: Cause for Crosstalk on Integrated Circuits, Crosstalk Prevention Methods	
Unit –IV	**10 Hrs**
Constraints for STA: Clock Constraints, Other Timing Constraints, 5.2.2 External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate	
Unit –V	**11 Hrs**
Timing Violations and Verification: Slack, Critical Path of Timing Report, Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Recovery and Removal Violation Check, Input/Output Timing Path Checks ,DRC Violation Check, Multi Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Setup Violations, Techniques to Fix Hold Violations, Time borrowing.	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Ability to apply the learnt basic concepts of STA to evaluate the delay of the circuits and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing.
CO2:	Ability to write their own constraint file and create the environment required for the given design and its specification to undergo for analysis using the EDA tool.
CO3:	Ability to set constraints, Validate the results and analyze the reports
CO4:	Ability to understand the journal research papers related to Timing analysis techniques and able to present the knowledge of new techniques for the given design. (Re-do)

Reference Books	
1	"Static Timing Analysis for Nanometer Designs: A Practical Approach", J. Bhasker, R. Chadha, Springer, 2009, ISBN: 978-0-387-93819-6, 978-0-387-93820-2(e-book).
2	"Static Timing Analysis for VLSI circuits", R.Jayagowri, Pushpendra S. Yadav, MEDTECH, A Division of Scientific International , 2018.
3	"Timing Analysis and Optimization of Sequential Circuits," Naresh Maheshwari and Sachin S. Sapatnekar, Springer Science + Business Media, LLC, Library of Congress Cataloging-in-Publication Data, 1999, ISBN:978-1-4613-7579-1, 978-1-4615-5637-4 (eBook).
4	"Constraining Designs for Synthesis and Timing Analysis - A Practical Guide to Synopsys Design Constraints (SDC)," Sridhar Gangadharan and Sanjay Churiwala,Springer Science + Business Media, LLC, Library of Congress Cataloging-in-Publication Data, 2013, ISBN:978-1-4614-3268-5, 978-1-4614-3269-2 (eBook).
5	"Digital Timing Macro modeling for VLSI Verification," Jeong T.K, David O, Springer Science + Business Media, LLC, Library of Congress Cataloging-in-Publication Data, 1995, ISBN: 978-1-4613-5982-1, 978-1-4615-2321-5 (eBook).

Continuous Internal Evaluation (CIE): Total marks: 100

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.

Total CIE is 20+50+30=100 Marks.

Semester End Evaluation (SEE): Total marks: 100

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

INTERNSHIP						
Course Code	**:**	**18MVE33**		**CIE Marks**	**:**	**100**
Credits	**:**	**L:T:P**	**0:0:5**	**SEE Marks**	**:**	**100**
Hours/week	**:**	**10Hrs**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES FOR INTERNSHIP

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the process of applying engineering knowledge to produce product and provide services.

(2) Explain the importance of management and resource utilization

(3) Comprehend the importance of team work, protection of environment and sustainable solutions.

(4) Imbibe values, professional ethics for lifelong learning.

1) The duration of the internship shall be for a period of 8 weeks on full time basis between II semester final exams and beginning of III semester.
2) The student must submit letters from the industry clearly specifying his / her name and the duration of the internship on the company letter head with authorized signature.
3) Internship must be related to the field of specialization or the M.Tech program in which the student has enrolled.
4) Students undergoing internship training are advised to report their progress and submit periodic progress reports to their respective guides.
5) Students have to make a presentation on their internship activities in front of the departmental committee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the internship final report. However interim or periodic reports and reports as required by the industry / organization can be submitted as per the format acceptable to the respective industry /organizations.
6) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
7) The broad format of the internship final report shall be as follows
    - Cover Page
    - Certificate from College
    - Certificate from Industry / Organization
    - Acknowledgement
    - Synopsis
    - Table of Contents
    - Chapter 1 - Profile of the Organization – Organizational structure, Products, Services, Business Partners, Financials, Manpower, Societal Concerns, Professional Practices,
    - Chapter 2 - Activities of the Department -
    - Chapter 3 – Tasks Performed – summaries the tasks performed during 8 week period
    - Chapter 4 – Reflections – Highlight specific technical and soft skills that you acquired during internship
    - References & Annexure

Course Outcomes:

After going through the internship the student will be able to:

CO1: Apply engineering and management principles

CO2: Analyze real-time problems and suggest alternate solutions
CO3: Communicate effectively and work in teams
CO4: Imbibe the practice of professional ethics and need for lifelong learning.

1. Scheme of Continuous Internal Evaluation (CIE):

A committee comprising of the Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation of the application of engineering knowledge in industries 35%
(2) Ability to comprehend the functioning of the organization/ departments 20%
(3) Importance of resource management, environment and sustainability 25%
(4) Presentation Skills and Report 20%

Dissertation Phase 1						
Course Code	**:**	**18MVE34**		**CIE Marks**	**:**	**100**
Credits	**:**	**L:T:P**	**0:0:5**	**SEE Marks**	**:**	**100**
Hours	**:**	**10**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

The students shall be able to

1. Understand the method of applying engineering knowledge to solve specific problems.
2. Apply engineering and management principles while executing the project
3. Demonstrate good verbal presentation and technical report writing skills.
4. Identify and solve complex engineering problems using professionally prescribed standards.

GUIDELINES

1. Major project will have to be carried out by only one student in his/her area of interest.
2. Each student has to select a contemporary topic that will use the technical knowledge of their program of specialization.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The project can be carried out on-campus or in an industry or an organization with prior approval from the Head of the Department.
5. The standard duration of the project is for 16 weeks, however if the guide and the evaluation committee of the department, after the assessment feel that the work is insufficient and it has to be extended, then the student will have to continue as per the directions of the guide and the committee.
6. It is mandatory for the student to present his/her work in one of the international conferences or publish the research finding in a reputed unpaid journal with impact factor.

Course Outcomes:

After going through this course the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate life-long learning

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in THREE Phases. The evaluation committee will comprise of: guide, two senior faculty members, one industry member and Head of the Department.

Phase	Activity	Weightage
4th week	Topic approval along with Synopsis	20%
8th week	Literature survey with Problem Statement	20%
12th week	Motivation and Objectives	20%
15th week	Preliminary report for the approval of selected topic along with methodology.	40%

CIE Evaluation shall be done with marks distribution as follows:

- Selection of the topic 10%
- Literature review and framing of objectives 25%
- Defining the brief methodology along with the algorithm development/experimental setup 25%
- Presentation 20%
- Report writing 20%

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

1. Brief write-up about the project 5%
2. Formulation of Project Objectives & Methodology
   20%
3. Presentation 25%
4. Report
   20%
5. Viva Voce
   30%

Dissertation Phase II						
Course Code	**:**	**18MVE41**		**CIE Marks**	**:**	**100**
Credits	**:**	**L:T:P**	**0:0:20**	**SEE Marks**	**:**	**100**
Hours/Week	**:**	**40**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

The students shall be able to

1. Understand the method of applying engineering knowledge to solve specific problems.
2. Apply engineering and management principles while executing the project
3. Demonstrate good verbal presentation and technical report writing skills.
4. Identify and solve complex engineering problems using professionally prescribed standards.

GUIDELINES

1. Major project will have to be done by only one student in his/her area of interest.
2. Each student has to select a contemporary topic that will use the technical knowledge of their program of specialization.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The project can be carried out on-campus or in an industry or an organization with prior approval from the Head of the Department.
5. The standard duration of the project is for 16 weeks, however if the guide and the evaluation committee of the department, after the assessment feel that the work is insufficient and it has to be extended, then the student will have to continue as per the directions of the guide and the committee.
6. It is mandatory for the student to present his/her work in one of the international conferences or publish the research finding in a reputed unpaid journal with impact factor.

Course Outcomes:

After going through this course the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate life long learning

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in THREE Phases. The evaluation committee will comprise of: guide, two senior faculty members, one industry member and Head of the Department.

Phase II	Activity	Weightage
5th week	Review and refinement of Objectives and methodology.	20%
10th week	Mid-term progress review shall check the compliance with the objectives and methodology presented in Phase I, review the work performed.	40%
15th week	Oral presentation, demonstration and submission of project report. Outcome and publication	40%

CIE Evaluation shall be done with marks distribution as follows:

- Review of formulation of objectives and methodology 10%
- Design and simulation/ algorithm development/experimental setup 25%
- Conducting experiments / implementation / testing / analysis 25%
- Demonstration & Presentation 20%
- Report writing 20%

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

1.	Brief write-up about the project	5%
2.	Formulation of Project Objectives & Methodology	20%
3.	Experiments / Analysis Performed; Results & Discussion	25%
4.	Report	20%
5.	Viva Voce	30%

TECHNICAL SEMINAR						
Course Code	**:**	**18MVE42**		**CIE Marks**	**:**	**50**
Credits	**:**	**L:T:P**	**0:0:2**	**SEE Marks**		**50**
Hours/Week	**:**	**4**		**SEE Duration**		**30 min**

Course Learning Objectives (CLO):
The students shall be able to:

(1) Understand the technological developments in their chosen field of interest
(2) Explain the scope of work and challenges in the domain area
(3) Analyze these engineering developments in the context of sustainability and societal concerns.
(4) Improve his/her presentation skills and technical report writing skills

GUIDELINES

1) The presentation will have to be done by individual students.
2) The topic of the seminar must be in one of the thrust areas with in-depth review and analysis on a current topic that is relevant to industry or on-going research.
3) The topic could be an extension or complementary to the project
4) The student must be able to highlight or relate these technological developments with sustainability and societal relevance.
5) Each student must submit both hard and soft copies of the presentation.

Course Outcomes:
After going through this course the student will be able to:
CO1: Identify topics that are relevant to the present context of the world
CO2: Perform survey and review relevant information to the field of study.
CO3: Enhance presentation skills and report writing skills.
CO4: Develop alternative solutions which are sustainable

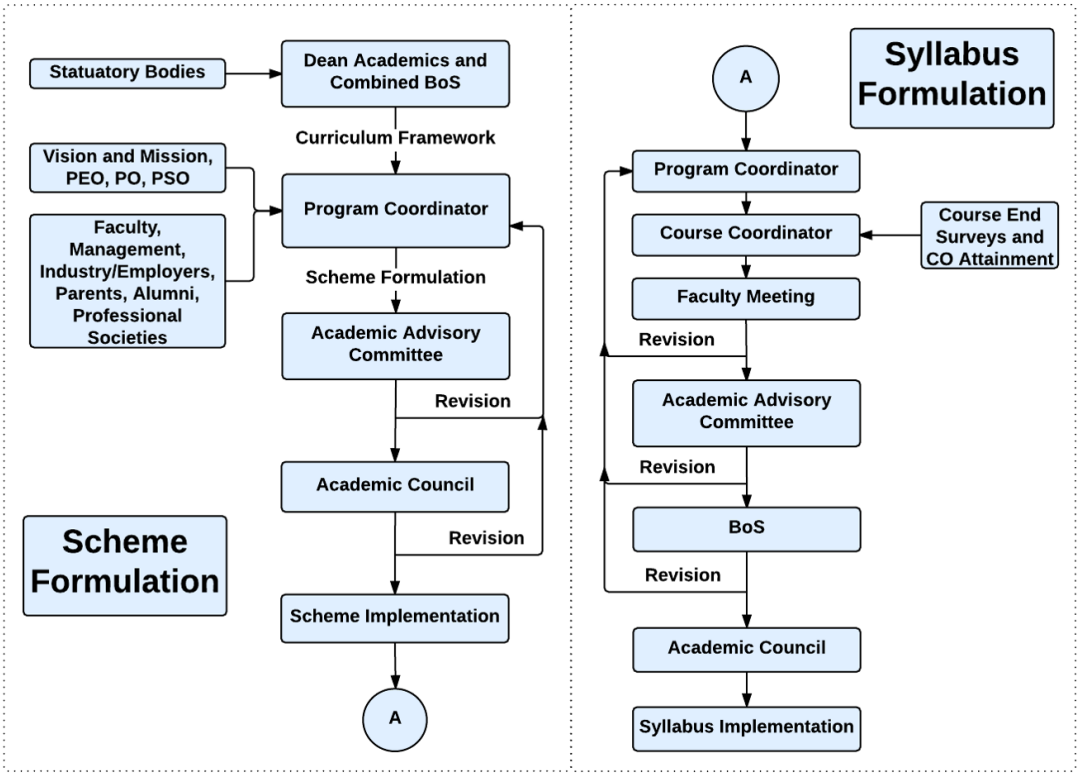
Scheme of Continuous Internal Evaluation (CIE): Evaluation would be carried out in TWO phases. The evaluation committee shall comprise of Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):
The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

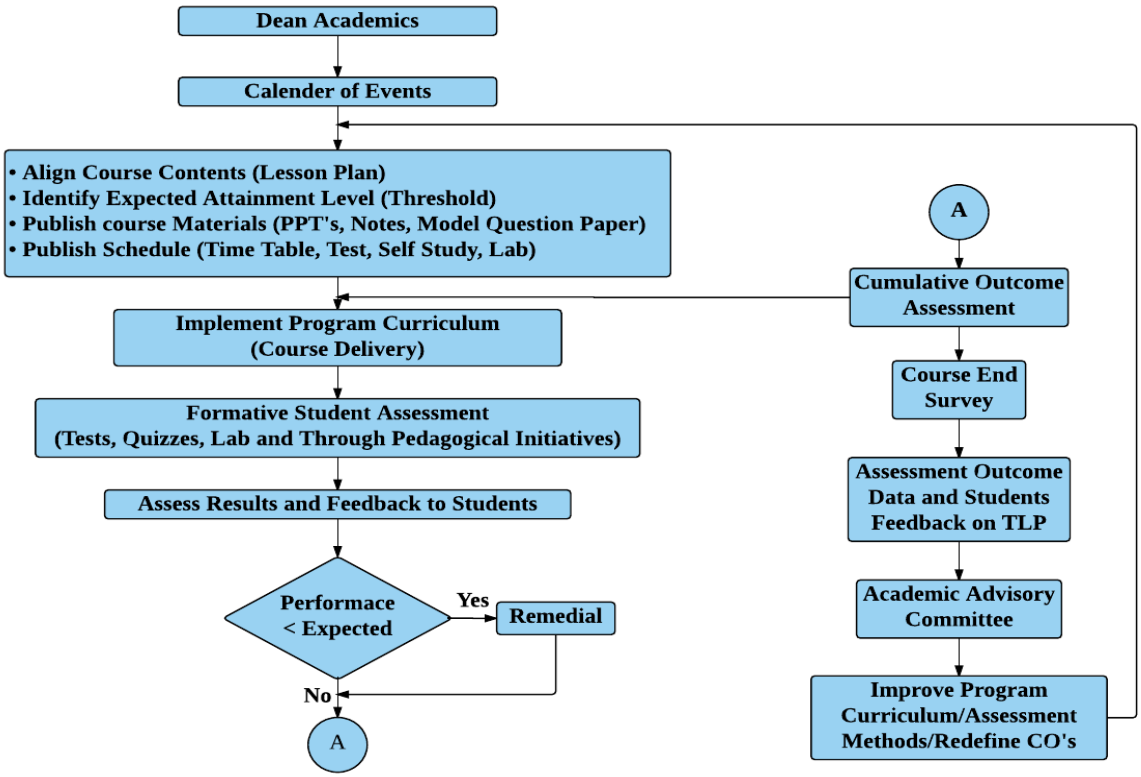
Rubrics for Evaluation:

1) Topic – Technical Relevance, Sustainability and Societal Concerns 15%
2) Review of literature 25%
3) Presentation Skills 35%
4) Report 25%

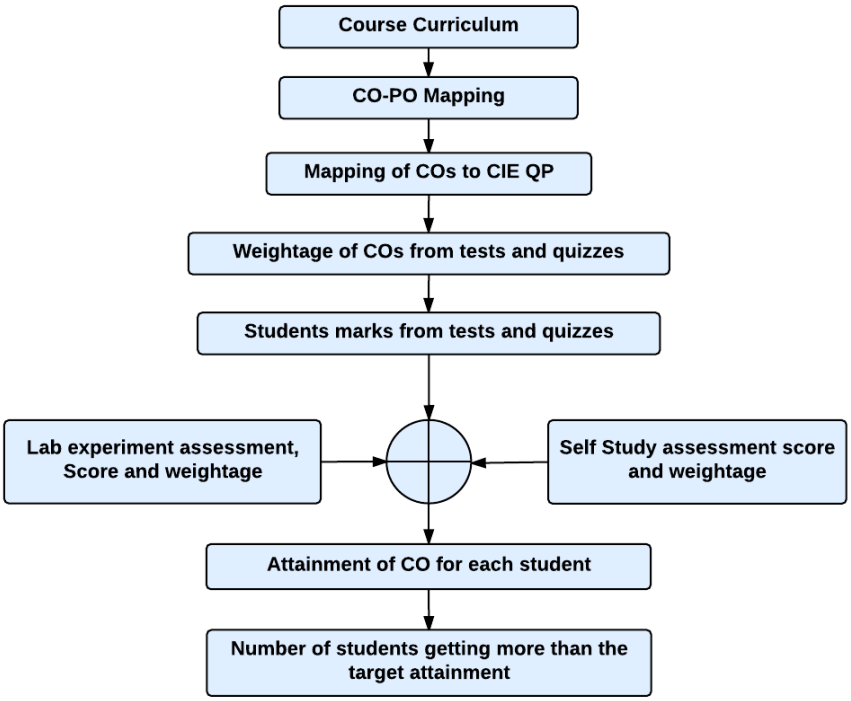
Curriculum Design Process



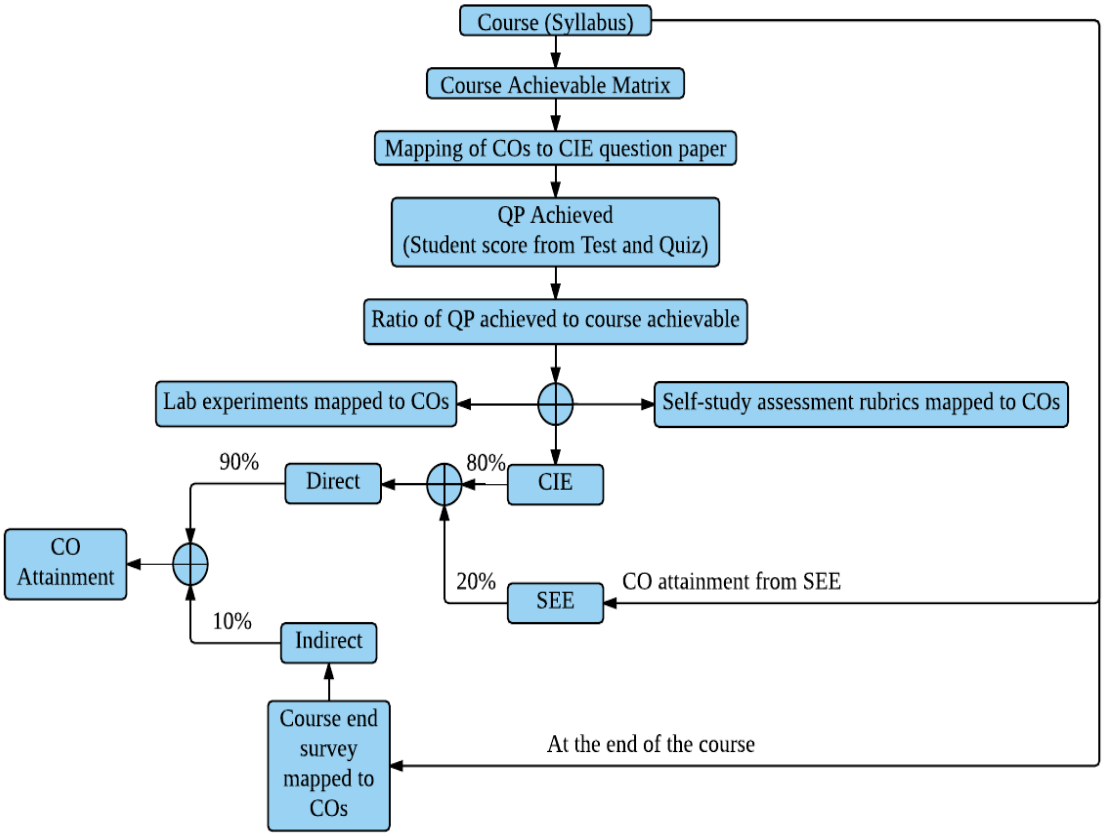
Academic Planning And Implementation



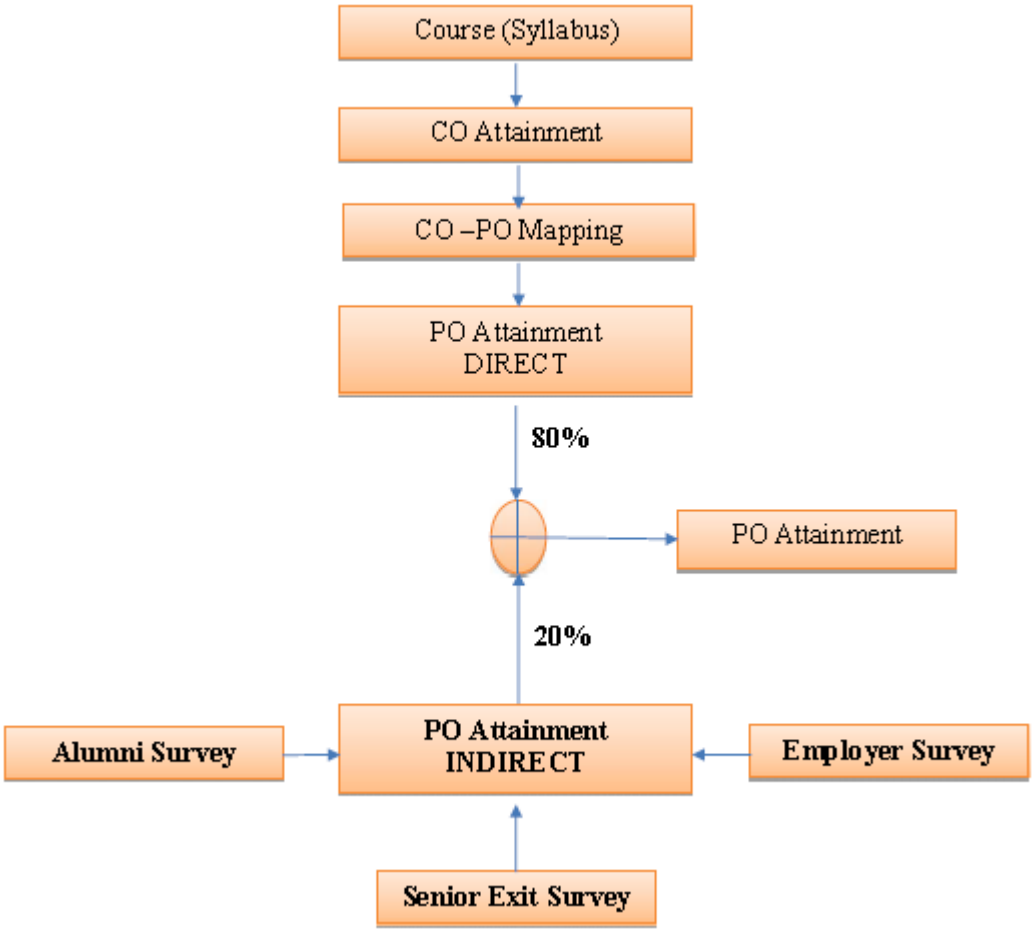
Process For Course Outcome Attainment



Final CO Attainment Process



Program Outcome Attainment Process



PROGRAM OUTCOMES (PO)

M. Tech. Communication Systems graduates will be able to:

PO1: Independently carry out research /investigation and development work to solve practical problems related to Communication Systems.

PO2: Write and present a substantial technical report/document in the field of Communication Systems

PO3: Demonstrate a degree of mastery over the area of Communication Systems. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering program

PO4: Design and develop communication system modules with good economics and business practices in order to meet the global challenges.

PO5: Abstract the requirements of an application to interface with communication modules.

PO6: Acquire professional and intellectual integrity, ethics of research and execute projects efficiently.