RV COLLEGE OF ENGINEERING®

(Autonomous Institution Affiliated to VTU, Belagavi)
RV Vidyaniketan Post, Mysuru Road
Bengaluru – 560 059

Scheme and Syllabus of I to IV Semesters

(Autonomous System of 2018 Scheme)

Master of Technology (M.Tech)
in
VLSI DESIGN AND EMBEDDED SYSTEMS

DEPARTMENT OF

ELECTRONICS & COMMUNICATION ENGINEERING

VISION

Leadership in Quality Technical Education, Interdisciplinary Research & Innovation, with a Focus on Sustainable and Inclusive Technology

MISSION

1. To deliver outcome based Quality education, emphasizing on experiential learning with the state of the art infrastructure.
2. To create a conducive environment for interdisciplinary research and innovation.
3. To develop professionals through holistic education focusing on individual growth, discipline, integrity, ethics and social sensitivity.
4. To nurture industry-institution collaboration leading to competency enhancement and entrepreneurship.
5. To focus on technologies that are sustainable and inclusive, benefiting all sections of the society.

QUALITY POLICY

Achieving Excellence in Technical Education, Research and Consulting through an Outcome Based Curriculum focusing on Continuous Improvement and Innovation by Benchmarking against the global Best Practices.

CORE VALUES

Professionalism, Commitment, Integrity, Team Work and Innovation

RV COLLEGE OF ENGINEERING®

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Scheme and Syllabus of I & II Semesters

(Autonomous System of 2018 Scheme)

Master of Technology (M.Tech)
in
VLSI DESIGN & EMBEDDED SYSTEMS

DEPARTMENT OF

ELECTRONICS & COMMUNICATION ENGINEERING

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

VISION

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering

MISSION

1. To impart quality technical education to produce industry-ready engineers with a research outlook.
2. To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.
3. To create centers of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.
4. To develop entrepreneurial skills among the graduates to create new employment opportunities

PROGRAMME OUTCOMES (PO)

M. Tech. in VLSI Design and Embedded Systems Program graduates will be able to:

PO1: Independently carry out research /investigation and development work to solve practical problems related to VLSI Design & Embedded Systems

PO2: Write and present a substantial technical report/document in the field of VLSI Design & Embedded Systems

PO3: Demonstrate a degree of mastery over the areas of VLSI Design & Embedded Systems. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.

PO4: Conceptualize and solve VLSI design and Embedded system problems and propose optimal solutions.

PO5: Analyze, learn and apply appropriate techniques, resources and modern engineering/IT tools in core and allied areas.

PO6: Acquire professional and intellectual integrity and ethics of research and execute projects efficiently.

ABBREVIATIONS

Sl. No.	Abbreviation	Acronym
1.	VTU	Visvesvaraya Technological University
2.	BS	Basic Sciences
3.	CIE	Continuous Internal Evaluation
4.	SEE	Semester End Examination
5.	CE	Professional Elective
6.	GE	Global Elective
7.	HSS	Humanities and Social Sciences
8.	CV	Civil Engineering
9.	ME	Mechanical Engineering
10.	EE	Electrical & Electronics Engineering
11.	EC	Electronics & Communication Engineering
12.	IM	Industrial Engineering & Management
13.	EI	Electronics & Instrumentation Engineering
14.	CH	Chemical Engineering
15.	CS	Computer Science & Engineering
16.	TE	Telecommunication Engineering
17.	IS	Information Science & Engineering
18.	BT	Biotechnology
19.	AS	Aerospace Engineering
20.	PY	Physics
21.	CY	Chemistry
22.	MA	Mathematics
23.	MCA	Master of Computer Applications
24.	MST	Structural Engineering
25.	MHT	Highway Technology
26.	MPD	Product Design & Manufacturing
27.	MCM	Computer Integrated & Manufacturing
28.	MMD	Machine Design
29.	MPE	Power Electronics
30.	MVE	VLSI Design & Embedded Systems
31.	MCS	Communication Systems
32.	MBS	Bio Medical Signal Processing & Instrumentation
33.	MCH	Chemical Engineering
34.	MCE	Computer Science & Engineering
35.	MCN	Computer Network Engineering
36.	MDC	Digital Communication
37.	MRM	Radio Frequency and Microwave Engineering
38.	MSE	Software Engineering
39.	MIT	Information Technology
40.	MBT	Biotechnology
41.	MBI	Bioinformatics

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M.Tech Program in VLSI DESIGN & EMBEDDED SYSTEMS

FIRST SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Credits**
1	18MVE11	Digital System Design using Verilog	EC	4	0	0	**4**
2	18MVE12	Advanced Embedded System Design	EC	3	1	1	**5**
3	18MVE13	Digital IC Design	EC	3	1	1	**5**
4	18HSS14	Professional Skill Development	HSS	0	0	0	**0**
5	18MVE1AX	Elective – A	EC	4	0	0	**4**
6	18MVE1BX	Elective – B	EC	4	0	0	**4**
Total number of Credits				**18**	**2**	**2**	**22**
Total Number of Hours / Week				**18**	**4**	**4**	**26**

SECOND SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Credits**
1	18MVE21	Analog IC Design	EC	3	1	1	**5**
2	18MVE22	System Verilog for Design & Verification	EC	3	1	0	**4**
3	18IM23	Research Methodology	IM	3	0	0	**3**
4	18MVE24	Minor Project	EC	0	0	2	**2**
5	18MVE2CX	Elective – C	EC	4	0	0	**4**
6	18MVE2DX	Elective – D	EC	4	0	0	**4**
7	18XX2GX	Global Elective-G	Respective boards	3	0	0	**3**
Total number of Credits				**20**	**2**	**3**	**25**
Total Number of Hours / Week				**20**	**4**	**6**	**30**

SEMESTER : I		
GROUP A: PROFESSIONAL ELECTIVES		
Sl. No.	**Course Code**	**Course Title**
1.	18MVE1A1	Advanced Computer Architecture
2.	18MVE1A2	ASIC Design
3.	18MVE1A3	Algorithms for VLSI Design
GROUP B: PROFESSIONAL ELECTIVES		
1.	18MVE1B1	MEMS and Smart Systems
2.	18MVE1B2	System On Chip Design
3.	18MVE1B3	Advanced VLSI Devices
SEMESTER : II		
GROUP C: PROFESSIONAL ELECTIVES		
1.	18MVE2C1	VLSI Testing
2.	18MCS2C2	Machine Learning
3.	18MVE2C3	High speed VLSI Design
GROUP D: PROFESSIONAL ELECTIVES		
1.	18MVE2D1	Low Power VLSI Design
2.	18MVE2D2	Advanced Embedded Processors
3.	18MVE2D3	VLSI Digital Signal Processing Systems

GROUP G: GLOBAL ELECTIVES				
Sl. No.	**Host Dept**	**Course Code**	**Course Title**	**Credits**
1.	CS	18CS2G01	Business Analytics	3
2.	CV	18CV2G02	Industrial & Occupational Health and Safety	3
3.	IM	18IM2G03	Modelling using Linear Programming	3
4.	IM	18IM2G04	Project Management	3
5.	CH	18CH2G05	Energy Management	3
6.	ME	18ME2G06	Industry 4.0	3
7.	ME	18ME2G07	Advanced Materials	3
8.	CY	18CHY2G08	Composite Materials Science and Engineering	3
9.	PY	18PHY2G09	Physics of Materials	3
10.	MA	18MAT2G10	Advanced Statistical Methods	3

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M.Tech Program in VLSI DESIGN & EMBEDDED SYSTEMS

THIRD SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Credits**
1.	18MVE31	Synthesis & Optimization of Digital Circuits	EC	4	1	0	**5**
2.	18MVE32	Internship	EC	0	0	5	**5**
3.	18MVE33	Major Project : Phase I	EC	0	0	5	**5**
4.	18MVE3EX	Professional Elective –E	EC	4	0	0	**4**
Total number of Credits				**8**	**1**	**10**	**19**
Total Number of Hours / Week				**8**	**2**	**20**	**30**

SEMESTER : III		
GROUP E: CORE ELECTIVES		
Sl. No.	**Course Code**	**Course Title**
1.	18MVE3E1	Radio Frequency IC Design
2.	18MVE3E2	ARM Programming and Optimization
3.	18MVE3E3	Static Timing Analysis

FOURTH SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Credits**
1.	18MVE41	Major Project : Phase II	EC	0	0	20	20
2.	18MVE42	Technical Seminar	EC	0	0	2	2
Total number of Credits				**0**	**0**	**22**	**22**
Total Number of Hours / Week				**0**	**0**	**44**	**44**

SEMESTER : I						
DIGITAL SYSTEM DESIGN USING VERILOG						
Course Code	**:**	**18MVE11**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **11 Hrs**

Introduction to Verilog and Design Methodology:

Introduction to Verilog: Verilog IEEE standards, Application Areas and Abstraction levels, Need of verification of HDL design, Simulation and Synthesis, Test-benches,

Verilog Data Types: Net, Register and Constant. Verilog Operators: Logical, Arithmetic, Bitwise, Reduction, Relational, Concatenation and Conditional, Number representation and Verilog ports.

Verilog Primitives. **Logic Simulation, Design Verification, and Test Methodology:** Four-Value Logic and Signal Resolution in Verilog, Test Methodology Signal Generators for Test benches, Event-Driven Simulation, Sized Numbers.Propagation Delay.

Introduction to Design Methodology:

Digital Systems and Embedded Systems, Real-world circuits. Design Methodology: Design Flow-Architecture, Functional design and verification, Synthesis, Physical design. Design Optimization-Area, Timing and Power, System representation.

Unit – II **11 Hrs**

Number Basics and Verilog Modelling Styles:

Number Basics: Unsigned and Signed Integers, Fixed-point and Floating-point Numbers. Boolean Functions and Boolean Algebra, Verilog models for Boolean switching function, Binary Coding.

Behavioural Modelling: Latches and Level-Sensitive Circuits in Verilog, Cyclic Behavioural Models of Flip-Flops and Latches, Cyclic Behaviour and Edge Detection. A Comparison of Styles for Behavioural modelling, Behavioural Models of Multiplexers, Encoders, Decoders and Arithmetic circuits.

Dataflow Modelling: Boolean Equation-Based Models of Combinational Logic, Propagation Delay and Continuous Assignments. Dataflow Models of a Linear-Feedback Shift Register. Modelling Digital Machines with Repetitive Algorithms Machines with Multicycle Operations. Tasks & Functions.

Structural Modelling: Design of Combinational Logic, Verilog Structural Models, Module Ports, Top-Down Design and Nested Modules. Gate level modelling.

Unit – III **10 Hrs**

Synthesis of Digital Sub-systems:

Synthesis of Combinational Sub-systems: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Three-state Devices and Bus Interfaces.

Synthesis of Sequential Sub-systems: Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines, Registered Logic, State Encoding, Synthesis of Implicit State Machines, Registers and Counters.

Unit – IV **10 Hrs**

System Implementation Fabrics and Accelerators: Introduction of Programmable Logic Array (PLA), Programmable Array Logic (PAL), Programmability of PLDs. Complex PLDs (CPLDs), Field-Programmable Gate Arrays (Artix-7 and Virtex-5) The Role of FPGAs in the ASIC Market, FPGA Technologies. Verilog-Based Design Flows for FPGAs and ASICs. Comparison of design implementation using CPLDs, FPGA and ASIC.

System Accelerators: Concepts, Case study: Video Edge detection, Verification of accelerators.

User-Defined Primitives: Combinational Primitives: Basic Features of User-Defined Primitives, Describing Combinational Logic Circuits. Sequential Primitives: Level-Sensitive Primitives, Edge-Sensitive Primitives.

Unit – V **10 Hrs**

Processor Design and System Development:

Design of Processor Architectures: Functional Units for Addition, Subtraction and Multiplication (overview). Design: Hierarchical Decomposition STG-Based Controller Design, Efficient STG-Based Sequential Binary Multiplier.

Interfacing Concepts: Embedded Computer Organization, Instruction and Data, Memory Interfacing. I/O Interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission.

Course Outcomes **After taking up this course, the student will be able to:**	
CO1	Understand the digital system designs skills using VERILOG HDL based on IEEE-1364 standards and managed by Open Verilog International (OVI).
CO2	Demonstrate the skill on cost-effective system designs through proper selection of implementation fabrics for the desired application.
CO3	Analyze complete systems and build small scale applications using Interfacing concepts.
CO4	Design and implement complete digital systems using VERILOG HDL and demonstrate the innovation skills

Reference Books	
1.	Advanced Digital Design With the Verilog HDL, Michael D. Ciletti, 2nd Edition, PHI, ISBN: 978–0–07–338054–4 2015.
2.	Digital Design: An Embedded Systems Approach Using VERILOG, Peter J. Ashenden,Elsevier, ISBN: 978-0-12-369527-7, 2010.
3.	Digital Systems Design Using Verilog, Charles Roth, Lizy K. John, ByeongKil Lee,Cengage Learning, *ISBN*-10: 1285051076, 2015.
4.	Fundamentals ofDigital Logic with Verilog Design, Stephen Brown and ZvonkoVranesic, 6th Edition, McGraw Hill publication, ISBN: 978–0–07–338054–4, 2014.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : I						
ADVANCED EMBEDDED SYSTEM DESIGN (Theory and Practice)						
Course Code	**:**	**18MVE12**		**CIE Marks**	**:**	**100 + 50**
Credits L:T:P	**:**	**3:1:1**		**SEE Marks**	**:**	**100 + 50**
Hours	**:**	**39L+26T+26P**		**SEE Duration**	**:**	**3 +3 Hrs**

Unit – I **9 Hrs**

Introduction to Embedded System Design

Introduction, Characteristics of Embedding Computing Applications, Concept of Real time Systems, Challenges in Embedded System Design, Design Process: Requirements, Specifications, Hardware Software Partitioning, System Integration

Embedded System Architecture

Instruction Set Architectures with examples, Memory system Architecture: Von Neumann, Harvard, caches, Virtual Memory, Memory Management, I/O sub system: Busy wait I/O,DMA, Interrupt Driven I/O, Co-Processor & Hardware Accelerators, Processor performance Enhancement: Pipelining, Superscalar Execution, Multi Core CPUs, Benchmarking Standards: MIPS, MFLOPS, MMACS, Coremark

Unit – II **7 Hrs**

Designing Embedded System Hardware –I

CPU Bus: Bus Protocols, Bus Organisation, Memory Devices and their Characteristics: RAM, EEPROM, Flash Memory, DRAM; I/O Devices: Timers and Counters, Watchdog Timers, Interrupt Controllers, A/D and D/A Converters

Unit – III **8 Hrs**

Designing Embedded System Hardware –II

Component Interfacing: Memory interfacing with case study; I/O Device Interfacing with case Study: Programmed IO, Memory Mapped IO, Interfacing Protocols: SPI, I2C, Reset Circuits, FPGA based Design, Processor Selection Criteria

Unit – IV **7 Hrs**

Designing Embedded System Software –I

Application Software, System Software, Use of High Level Languages: C,C++, Programming & Integrated Development Environment tools: Editor, Compiler, Linker, Automatic Code Generators, Debugger, Board Support Library, Chip Support Library, Analysis and Optimization: Execution Time, Energy & Power, Program Size; Embedded System Coding Standards: MISRA C 2012/CERT

Unit – V **8 Hrs**

Designing Embedded System Software –II

OS based Design, Real Time Kernel, Process& Thread, Inter Process Communications, Synchronization, Case Study: RTX-ARM, Response time Calculation, Interrupt Latency, Time Loading, Memory Loading, Case Study: Embedded Control Applications-Software Coding of a PID Controller

LAB COMPONENT **2 Hrs/Week**

Experiments on bare metal programming

1. Write application program to interface LEDs and push buttons to GPIOs of LPC 1857 cortex M3 evaluation board and demonstrate polling-based IO operation.
2. Write Systick_handler to accurately control the delay between toggling of LEDs to support interrupt driven IO.
3.Write driver for ADC0 in LPC 1857 MCU. Display digital value on GLCD and demonstrate analog sensor interface. Write driver functions for ADC initialization, ADC start of conversion, reading digital value output. Develop main function using APIs of ADC driver to test the functionality.
4. Write I2C driver for LPC1857. Develop following APIs to support I2C.

```
uint32_t  I2C_Init  (void);
uint32_t  I2C_Start  (void);
uint32_t  I2C_Stop  (void);
uint32_t  I2C_Addr  (uint8_t  adr, uint8_t dir);
uint32_t  I2C_Write  (uint8_t  byte);
```

uint32_t I2C_Read (uint32_t ack, uint8_t *byte);

5. Write driver to support LM75a digital temperature sensor through I2C. Make use of APIs developed in experiment 4 to interface LM75a to LPC 1857 MCU. Test the functionality by displaying temperature values on GLCD.

6. Write application program to realize FIR filter on STM32F4 cortex M4 development board. Test the filtering operation on signal generated from function generator and interfaced to STM32F4 development board through WolfsonPI codec.

Experiments using RTOS

1. Create a multitasking application program to demonstrate creation of tasks. Task1 is expected to control the blinking two LEDs and Task2 is to change font and colour of the textual display on GLCD concurrently. Use APIs of RL-RTX/Freertos real time kernel. Configure systick timer to generate tick interval.

2. Create multitasking program to demonstrate task synchronization. Task1 is expected to display LED blinking pattern and Task2 display textual message on GLCD. Synchronize the access of GLD using mutex/semaphore using APIs of RL-RTX/Freertos.

3. Create a multitasking program to demonstrate event flags to synchronize task execution. Create four tasks to simulate the operation of stepper motor driver. Use four LEDs blinking to simulate the activation of the four output driver stages. Create another concurrently executing task to display text on GLCD. The stepper motor driver tasks are expected to run sequentially.

4. Create multitasking program to demonstrate IPC using mailbox. Create a task to read a digital value from ADC and send to another task executing concurrently through mailbox. Synchronize the execution of tasks. Use APIs of RL-ARM/Freertos real time kernel.

5. Create a 'Blinky' project using RL-ARM real time Kernel to simulate the operations of step-motor driver. Use four LEDs blinking to simulate the activation of the four output driver stages. Create other two tasks executing concurrently and competing for GLCD. The first task displays status of LEDs blinking on GLCD and second task displays a string with changing colour of font and background. Use suitable mechanism to protect shared resource.

Course Outcomes

After going through this course the student will be able to:

CO1	Describe hardware & software of embedded systems for real time applications with suitable processor architecture, memory and communication interface.
CO2	Design embedded software & hardware to meet given constraints with the help of modern engineering tools.
CO3	Demonstrate compliance of prescribed safety norms through implementation of the identified engineering problems pertaining to automobiles, aerospace & biomedical applications.
CO4	Engage in self-study to design, implement and demonstrate open ended problem

Reference Books

1.	Embedded Systems – A contemporary Design Tool, James K Peckol, , John Weily, 2008, ISBN: 0-444-51616-6
2.	Introduction to Embedded Systems,Shibu K V, ,Tata McGraw Hill Education Private Limited, 2009, ISBN: 10: 0070678790
3.	Embedded Software Primer, David E.Simon, ,Addison Wesley, ISBN-13: 978-0201615692
4.	The Intel Micro-processors, Architecture, Programming and Interfacing" Barry B.Brey, 6th Edition, Pearson Education.

Scheme of Continuous Internal Evaluation (CIE): Total marks: 100+50=150

Scheme of Continuous Internal Evaluation (CIE): Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Continuous Internal Evaluation (CIE): Practical (50 Marks)
The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Scheme of Semester End Examination (SEE): Practical (50 Marks)
SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

Semester End Evaluation (SEE): Total marks: 100+50=150

Theory (100 Marks) + Practical (50 Marks) =Total Marks (150)

SEMESTER : I						
DIGITAL IC DESIGN (Theory and Practice)						
Course Code	**:**	**18MVE13**		**CIE Marks**	**:**	**100+50**
Credits L:T:P	**:**	**3:1:1**		**SEE Marks**	**:**	**100+50**
Hours	**:**	**39L+26T+26P**		**SEE Duration**	**:**	**3 + 3 Hrs**

Unit – I	**7Hrs**
Introduction: Issues in Digital IC Design, Design abstraction levels in digital circuits, Quality Metrics of a Digital Design **MOS Transistor:** Device structure, MOSFET- static & dynamic behaviour, secondary effects, technology scaling	
Unit – II	**8Hrs**
CMOS inverter: Static CMOS Inverter: static and dynamic Behaviour, Components of Energy and Power **CMOS Combinational Logic Circuit Design:** Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic. Dynamic CMOS Design: Dynamic Logic Design Considerations. Speed and Power Dissipation of Dynamic logic, Signal integrity issues, Cascading Dynamic gates.	
Unit – III	**8Hrs**
CMOS Sequential Logic Circuit Design: Static Latches and Registers. Dynamic Latches and Registers. Pulse Based Registers. Sense Amplifier based registers. Pipelining concepts. **Memory & Array structures design:** Memory core – ROM, SRAM, DRAM, Sense amplifiers, CAM	
Unit – IV	**8Hrs**
Interconnects: Resistive, Capacitive and Inductive Parasitics (basics) **Timing Issues:** Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and Impact on Performance. Clock Distribution techniques, Latch based clocking.	
Unit – V	**8Hrs**
Arithmetic building blocks design: Data paths in digital processor architectures – Adder, binary adder, static adder, mirror adder, TG based adder, carry bypass adder, linear and square root carry select adder, carry lookahead adder, Multiplier- array, carry save multiplier	

Lab Component

1. Introduction to Cadence environment; setup Linux environment; create schematic and symbol, introduction to netlist, technology library.
2. Inverter static characteristics
3. Inverter dynamic characteristics
4. Design and Analysis of NAND, NOR and complex gates
5. Layout, DRC, LVS, RCX and post-layout simulation of CMOS Inverter
6. Layout of CMOS NAND, NOR Inverter static characteristics
7. LEF file generation
8. LIB file generation
9. Synthesis of combinational logics
10. Case study: Synthesis of serial adder and PAR using Encounter tool.

Course Outcomes

After going through this course the student will be able to:

CO1	Investigate device, circuit & system aspects of digital IC design
CO2	Analyze the functionality of digital integrated circuits & systems
CO3	Design and implement digital integrated circuit & systems
CO4	Evaluate the different performance parameters of a digital integrated circuits & systems

Reference Books

1.	Digital Integrated Circuits: A Design Perspective, Jan M.Rabaey, AnanthaChadrakasan, BorivojeNikolic, (2/e), Pearson 2016, ISBN-13: 978-0130909961
2.	Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Erik Brunvand, Pearson 2009, ISBN-13: 9780321547743

3.	Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology, David A Hodges, Horace G Jackson and Resve A Saleh, TMH.2005, ISBN-13: 978-0072283655
4.	CMOS Digital Integrated Circuits; Sung MO Kang, YousufLeblebici, Tata McGrawHill, (3/e), ISBN: 0-7923-7246-8

Scheme of Continuous Internal Evaluation (CIE): Total marks: 100+50=150

Scheme of Continuous Internal Evaluation (CIE): Theory (100 Marks)
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Semester End Evaluation (SEE): Total marks: 100+50=150

Theory (100 Marks) + Practical (50 Marks) =Total Marks (150)

SEMESTER : I						
PROFESSIONAL SKILL DEVELOPMENT (Common to all Programs)						
Course Code	**:**	**18HSS14**		**CIE Marks**	**:**	**50**
Credits L: T: P	**:**	**0:0:0**		**SEE Marks**	**:**	**Audit Course**
Hours	**:**	**24 L**				

Unit – I	**03 Hrs**
Communication Skills: Basics of Communication, Personal Skills & Presentation Skills – Introduction, Application, Simulation, Attitudinal Development, Self Confidence, SWOC analysis. **Resume Writing:** Understanding the basic essentials for a resume, Resume writing tips Guidelines for better presentation of facts. Theory and Applications.	
Unit – II	**08 Hrs**
Quantitative Aptitude and Data Analysis: Number Systems, Math Vocabulary, fraction decimals, digit places etc.Simple equations – Linear equations, Elimination Method, Substitution Method, Inequalities. **Reasoning** – a. **Verbal** - Blood Relation, Sense of Direction, Arithmetic & Alphabet. b. **Non- Verbal reasoning** - Visual Sequence, Visual analogy and classification. **Analytical Reasoning** - Single & Multiple comparisons, Linear Sequencing. **Logical Aptitude** - Syllogism, Venn-diagram method, Three statement syllogism, Deductive and inductive reasoning. Introduction to puzzle and games organizing information, parts of an argument, common flaws, arguments and assumptions. **Verbal Analogies/Aptitude** – introduction to different question types – analogies, Grammar review, sentence completions, sentence corrections, antonyms/synonyms, vocabulary building etc. Reading Comprehension, Problem Solving	
Unit – III	**03 Hrs**
Interview Skills: Questions asked & how to handle them, Body language in interview, and Etiquette – Conversational and Professional, Dress code in interview, Professional attire and Grooming, Behavioral and technical interviews, Mock interviews - Mock interviews with different Panels. Practice on Stress Interviews, Technical Interviews, and General HR interviews	
Unit – IV	**03 Hrs**
Interpersonal and Managerial Skills:Optimal co-existence, cultural sensitivity, gender sensitivity; capability and maturity model, decision making ability and analysis for brain storming; Group discussion(Assertiveness) and presentation skills	
Unit – V	**07 Hrs**
Motivation: Self-motivation, group motivation, Behavioral Management, Inspirational and motivational speech with conclusion. (Examples to be cited). **Leadership Skills:** Ethics and Integrity, Goal Setting, leadership ability.	

Course Outcomes
After going through this course the student will be able to:

CO1	Develop professional skill to suit the industry requirement.
CO2	Analyze problems using quantitative and reasoning skills
CO3	Develop leadership and interpersonal working skills.
CO4	Demonstrate verbal communication skills with appropriate body language.

Reference Books

1.	The 7 Habits of Highly Effective People, Stephen R Covey, 2004 Edition, Free Press, ISBN: 0743272455
2.	How to win friends and influence people, Dale Carnegie, 1st Edition, 2016, General Press, ISBN: 9789380914787
3.	Crucial Conversation: Tools for Talking When Stakes are High, Kerry Patterson, Joseph Grenny, Ron Mcmillan 2012 Edition, McGraw-Hill Publication ISBN: 9780071772204
4.	Ethnus, Aptimithra: Best Aptitude Book, 2014 Edition, Tata McGraw Hill ISBN: 9781259058738

Phase	**Activity**
I	After the completion of Unit 1 and Unit 2, students are required to undergo a test set for a total of 50 marks. The structure of the test will have two parts. Part A will be quiz based, evaluated for 15 marks and Part B will be of descriptive type, set for 50 Marks and reduced to 35 marks. The total marks for

	this phase will be 50 (15 + 35).
II	Students will have to take up second test after the completion Unit 3, Unit 4 and Unit 5.The structure of the test will have two parts. Part A will be quiz based evaluated for 15 marks and Part B will be of descriptive type, set for 50 Marks and reduced to 35 marks. The total marks for this phase will be 50 (15 + 35).
FINAL CIE COMPUTATION	
Continuous Internal Evaluation for this course will be based on the average of the score attained through the two tests. The CIE score in this course, which is a mandatory requirement for the award of degree, must be greater than 50%.The attendance will be same as other courses.	

SEMESTER : I						
ADVANCED COMPUTER ARCHITECTURE (Professional Elective-A1)						
Course Code	**:**	**18MVE1A1**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **11Hrs**

Fundamentals Of Computer Design

Introduction; Classes of computers; Defining computer architecture; Trends in Technology, Power in Integrated Circuits and cost; Dependability; Measuring, reporting and summarizing Performance; Quantitative Principles of computer design. Pipeline and its hazards; Implementation of pipeline; Parallel Computer Models- The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMP Computers, PRAM and VLSI Models**.**

Unit – II **11 Hrs**

Processors and Memory Hierarchy

Advanced Processor Technology - Design Space of Processors, Instruction-Set Architectures CISC Scalar Processors RISC Scalar Processors. Superscalar and Vector Processors Superscalar Processors - The VLIW Architecture , Vector and Symbolic Processors. Memory Hierarchy Technology - Hierarchical Memory Technology, Inclusion, Coherence, and Locality Memory Capacity Planning; Virtual Memory Technology- Virtual Memory Models, TLB, Paging, and Segmentation Memory Replacement Policies Cache Memory Organizations - Cache Addressing Models, Direct Mapping and Associative Cache, Set-Associative and Sector Caches and Cache Performance Issues . Shared-Memory Organizations- Interleaved Memory Organization , Bandwidth and Fault Memory Allocation Schemes

Unit – III **10Hrs**

Multiprocessors and Multicomputer

Multiprocessor System Interconnects - Hierarchical Bus Systems, Crossbar Switch and Multiport Memory, Multistage and Combining Networks. Cache Coherence and Synchronization Mechanisms- The Cache Coherence Problem, Snoopy Bus Protocols, Directory-Based Protocols, Hardware Synchronization Mechanisms. Three Generations of Multicomputer - Design Choices in the Past , Present and Future Development , The Intel Paragon System. Message-Passing Mechanisms- Message-Routing Schemes, Deadlock and Virtual Channels Flow Control Strategies, Multicast Routing Algorithms.

Unit – IV **10Hrs**

Multivector and SIMP Computers

Vector Processing Principles-Vector Instruction Types , Vector-Access Memory Schemes Past and Present Supercomputers,Multivector Multiprocessors , Performance-Directed Design Rules Mainframes and Mini supercomputers,Compound Vector Processing -Compound Vector Operations , Vector Loops and Chaining , Multi pipeline Networking. SIMP Computer Organizations

Unit – V **10Hrs**

Scalable, Multithreaded and Dataflow Architectures

Latency-Hiding Techniques - Shared Virtual Memory , Prefetching Techniques, Distributed Coherent Caches, Scalable Coherence Interface, Relaxed Memory Consistency , Principles of Multithreading, Multithreading Issues and Solutions , Multiple-Context Processor, Multidimensional Architectures,Scalable and Multithreaded Architectures,Dataflow and Hybrid Architectures.

Course Outcomes

After going through this course the student will be able to:

CO1	Understand pipelining concepts, the performance metrics of microprocessors, Multithreading, multivector and dataflow architectures
CO2	Identify the factors affecting performance in superscalar processors and the key components, options and tradeoffs that a designer has to consider when designing such processors
CO3	Evaluate the performance and efficiency in advanced multiple-issue processors
CO4	Design various architectures and techniques for building high performance scalable multithreaded and multiprocessor systems.

Reference Books	
1.	Advanced Computer Architecture: Parallelism, Scalability, Programmabilit", Kai Hwang,, McGraw-Hill, first edition, 1992.
2.	Computer Architecture and parallel processing, Kai_Hwang,_Faye_A._Briggs, McGraw-Hill, first edition, 1984.
3.	Computer Architecture : A Quantitative Approach", Patterson, D.A., and Hennessy, J.L. ,Morgan Kaufmann Publishers, 5th Edition, Inc.2011
4.	Advanced Computer Architectures : A Design Space Approach,DezsoSima, Peter Kacsuk, Terence Fountain, , Pearson Education India, 1997

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : I						
ASIC DESIGN (Professional Elective-A2)						
Course Code	**:**	**18MVE1A2**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **11Hrs**

Introduction to ASICs
Types of ASICs: Full Custom ASIC, Semi-custom based ASICS, Standard Cell based ASIC,Gatearraybased ASIC, Channeledgate array, Channellessgate array, Structuredgate array, Programmablelogicdevices, FPGA.
Design flow.

Unit – II **11Hrs**

CMOS Logic
Combinational logic cells Sequential logic cells: Latch, flipflop, clocked inverter**.**
Data logic cells: Data Path Elements, Adders, Multipliers, Arithmetic operator.(Practical approach).
I/O Cell, Cell Compilers

Unit – III **10Hrs**

ASICLibraryDesign
Logicaleffort:predictingdelay,logicalareaandlogicalefficiency,logicalpaths,multistagecells,optimumdelay, optimum no. ofstages.
Librarycell design.
Programmable ASICS: The Antifuse, Static RAM, EPROM and EEPROM technology.

Unit – IV **10Hrs**

Programmable ASICs logic cells
Actel ACT: ACT1 logic module, Shannon's expansion theorem, Multiplexer logic as function generators, Timing models and critical path, speed gating, worst case timing.
Programmable ASIC Design Software: Design System, logic synthesis**,** Introduction to Synthesis and Simulation. (Practical analysis of the design parameters for speed, area & power optimization).
Low-LevelDesignEntry: SchematicEntry:Hierarchicaldesign.Thecelllibrary,Names,Schematic,Icons&Symbols,Nets ,schematicentry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener,Back annotation.

Unit – V **10Hrs**

ASICConstructionFloorPlanningandPlacement&Routing
PhysicalDesign,CADTools,SystemPartitioning,Estimating ASICsize, partitioningmethods. Floorplanningtools,I/Oandpowerplanning,clockplanning,placementalgorithms,iterativeplacementimprovement, Time drivenplacementmethods. PhysicalDesignflowglobalRouting,LocalRouting,DetailRouting, SpecialRouting, CircuitExtractionand DRC.

Course Outcomes
After going through this course the student will be able to:

CO1	Learn the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test.
CO2	Apply &analyze the design parameters for speed, area & power optimization.
CO3	Develop the algorithms required for the design of ASIC.
CO4	Apply the back-end physical design flow, including floorplanning, placement, andRouting techniques,

Reference Books

1. Application-SpecificIntegratedCircuits, M.J.S.Smith, – Pearson Education, 2003,ISBN:978-817758-408-0
2. Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime, H. Bhatnagar, - 2nd edition, 2001,ISBN:0792385373

3.	A Practical Approach from ASICs-to-SOCs ,FarzadNekoogarFarakNekooga: ISBN: 0-13-033857-5.
4.	Logic Synthesis Using Synopsys, P. Kurup, T. Abbasi, ISBN 0-7923-9582-4

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : I						
ALGORITHMS FOR VLSI DESIGN (Professional Elective-A3)						
Course Code	**:**	**18MVE1A3**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**11Hrs**
High Level Synthesis: Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations. **VLSI Simulation:** Gate-level modelling and simulation - Switch-level modelling and simulation - Combinational Logic Synthesis - Binary Decision Diagram.	
Unit – II	**11Hrs**
Data Structure and Basic Algorithms : Basic Terminology, Graph Search Algorithms Computational Geometry Algorithms. **VLSI partitioning& floor planning:** Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms. Problem formulation, classification, Constraint based, Integer programming based, rectangular dualization, simulated evolution floor planning algorithms.	
Unit – III	**10Hrs**
Placement and Routing : Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms. **Global Routing :**Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path based Algorithms, Steiner tree based Algorithms **Detailed Routing:** Problem formulation, Classification single Layer routing, General river routing, Single row routing.	
Unit – IV	**10Hrs**
Clock and Power Routing : Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms. **Compaction:** Classification of Compaction Algorithms, One-Dimensional Compaction, Two-Dimensional Compaction, Hierarchical Compaction.	
Unit – V	**10Hrs**
Genetic algorithm and its application in VLSI physical design: Terminologies – Simple Genetic algorithms ,steady state algorithm – Genetic operators-types of GA-Genetic algorithms vs Conventional algorithms – GA example – GA for VLSI design. Genetic algorithm in partioning , placement and routing.	

Course Outcomes
After going through this course the student will be able to:

CO1	Understand each stage of VLSI design flow.
CO2	Apply design knowledge to develop algorithms for VLSI design automation.
CO3	Investigate the algorithms for optimizing VLSI design with respect to speed, power and area.
CO4	Create an optimized VLSI cell using various algorithms.

Reference Books

1.	Algorithms for VLSI Design Automation, S.H. Gerez, John Wiley & Sons, 1998, ISBN: 978-0-471-98489-4
2.	Algorithms for VLSI Physical Design Automation, N.A. Sherwani, Kluwar Academic Publishers, 2002, ISBN: 0-7923-8393-1
3.	Genetic algorithms for VLSI design layout and test automation,Pinakimazumder and Elizabeth M Rudnick, Pearson Edition, 2011.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : I						
MEMS AND SMART SYSTEMS (Professional Elective-B1) (Common to VLSI & ES and CS)						
Course Code	**:**	**18MVE1B1**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **11 Hrs**

Introduction to MEMS and principle of operation.

Introduction, History of evolution, Definition of MEMS in a broader sense. Components of a smart system. Commercial products. Microsystems and Miniaturization. Evolution of micro-manufacturing. Design Aspects. Application and future scope of MEMS devices, Market trends.

Definitions and salient features of sensors, actuators and systems. Working principles of Microsystems.Sensors: silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, Actuators: silicon micro-mirror arrays, piezo-electric based inkjet printhead, electrostatic comb-drive and micromotor, magnetic micro relay.

Unit – II **11 Hrs**

Micro and Smart Devices and Systems: Materials and Processing

Materials

Introduction, Substrates and Wafers, Active substrate materials, Si as a substrate material, Si compounds, Si Piezoresistors, Gallium Arsenide, Quartz, Piezoelectric Crystals and Polymers.

Processing

Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization, Silicon micromachining: surface and bulk, bonding based process flows. Thick-film processing: Smart material processing, Emerging trends.

Unit – III **10Hrs**

Mechanical modelling and Scaling laws in Microsystems Modelling

Simplest deformable element: a bar, Transversely deformable element: a beam, Bimorph effect, Mechanical vibration: general formulation, Resonant Vibration, Design theory of accelerometers and damping coefficients. Basics of fluid mechanics in macro and mesoscales, Capillary effect, electro-phoresis and Dielectrophoresis.

Scaling laws in Miniaturization

Importance of scaling in MEMS- Scaling in geometry, Scaling in rigid body dynamics, scaling in electrostatic forces, scaling in electromagnetic forces, scaling in electricity, scaling in fluid dynamics. scaling effects in the optical domain, scaling in biochemical phenomena.

Unit – IV **10Hrs**

RF MEMS

Introduction to RF MEMS, Static Analysis of RF MEMS devices: Spring Constant of Low-k Beams, Spring Constant of Cantilever Beams, Spring Constant of Circular Diaphragms, Beam Curvature due to Stress Gradients. Electrostatic Actuation, Shape of the Deformed Beam Under Electrostatic Actuation, DC Hold-Down Voltage of MEMS Beams and Cantilevers, Forces on MEMS Beams, Self-Actuation of MEMS Capacitive Switches, RF Hold-Down Voltage of MEMS Capacitive Switches.

Unit – V **10Hrs**

Case study of devices: Pressure sensors, accelerometers, micro pump, micro heater. Introduction to CAD tool for simulation of devices.

Packaging : Integration of Microsystems and microelectronics, Packaging Introduction, Micro Systems Packaging, Objectives, Issues in packaging, Special issues in micro system packaging, Types of Microsystem Packages, Packaging Technologies.

Course Outcomes

After going through this course the student will be able to:

CO1	Explain the technology to fabricate advanced micro- and smart systems
CO2	Analyse different methods to fabricate MEMS devices.
CO3	Apply the basics of implementation of MEMS into products.
CO4	Evaluate the principles and processes involved in the implementation of MEMS devices

Reference Books	
1.	Micro and Smart Systems, Dr. A.K.Aatre, Ananth Suresh, K.J.Vinoy, S. Gopalakrishna, K.N.Bhat., John Wiley Publications, 2002, ISBN: 1118213904, 9781118213902
2.	MEMS & Microsystems: Design and Manufacture, Tai-Ran Tsu, Tata Mc-Graw-Hill.2002.8th reprint, ISBN-13:978-0-07-048709-3. ISBN-10:0-07-048709-X
3.	RF MEMS Theory, Design and Technology GABRIEL M. REBEIZ. 2003A JOHN WILEY & SONS PUBLICATION. ISBN: 978-0-471-20169-4
4.	Microsystems Design, S. D. Senturia, Kluwer Academic Publishers, Boston, USA, 2001, ISBN 0-7923-7246-8

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : I						
SYSTEM ON CHIP DESIGN (Professional Elective-B2)						
Course Code	**:**	**18MVE1B2**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**11Hrs**

Motivation for SoC Design: Introduction to SoC, SoB, SiP, Benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap.

System On Chip Design Process: Canonical SoC Design, SoC Design flow - waterfall vs spiral, Top-down vs Bottom up,Specification requirement, Types of Specification, System Design process, System level design issues- Soft IP vs Hard IP, Design for timing closure, Logic design issues- Verification strategy, On-chip buses and interfaces, Low Power, Manufacturing test strategies.

Unit – II	**11Hrs**

Macro Design Process: Overview of IP Design, Key Features, Planning and Specification, Macro design and Verification.

Developing Hard Macros: Overview, Design Issues for Hard Macros, The Hard Macro Design Process, Productization of Hard Macros.

Unit – III	**10Hrs**

SoC Verification:-Verification technology options, Verification methodology, Verification languages,Verification IP Reuse, approaches. Verification and Device Test, Verification Plans.

VLSI Packaging: Introduction, Packaging, Power Distribution, Input/Output, Chip-Package Co-design.

Unit – IV	**10Hrs**

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in anNoC. Packet switching and wormhole routing.

Unit – V	**10Hrs**

MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design: The limitations of traditional ASIC design, General Purpose Processor, The impact of SoC integration.

Course Outcomes

After going through this course the student will be able to:

CO1	Learn about the system on chip design and macro design process.
CO2	Analyze the design flow, IP cores, routing used in system on chip.
CO3	Exposure the concepts of verification methodology and interconnection methods in SoC
CO4	Design & Develop the algorithms required for the design of IP and SoC and Exposure to the concept of MPSoCs.

Reference Books

1	Pierre Bricaud,Reuse Methodology manual for System-On-A-Chip, Michael Keating, Designs,Kluwer Academic Publishers,second edition,2001.
2	SoC Verification-Methodology andTechniques, PrakashRashinkar, Peter Paterson and Leena Singh, Kluwer Academic Publishers,2001.
3	Multiprocessor Systems-on-chips, A.A.Jerraya, W.Wolf, 1st Edition,Morgan Kaufmann, 2004
4	On-Chip Communication Architectures: System on Chip Interconnect, SudeepPasricha and NikilDutt,Morgan Kaufmann Publishers © 2008.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : I						
ADVANCED VLSI DEVICES (Professional Elective-B3)						
Course Code	**:**	**18MVE1B3**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**11Hrs**
MOSFET Device Metrics, Transistors to Circuits, Energy Band View of Transistors, Traditional IV Theory, The "Virtual Source Model". **MOS Electrostatics**: Introduction, Depletion Approximation. Gate Voltage and Surface Potential, Flatband Voltage, Mobile Charge: Bulk MOS, Mobile Charge: ETSOI, 2D Electrostatics, The VS Model Revisited	
Unit – II	**11Hrs**
Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization	
Unit – III	**10 Hrs**
Beyond CMOS: Evolutionary advances beyond CMOS, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing	
Unit – IV	**10Hrs**
Ballistic Nanotransistor: Introduction, Landauer Approach, More on Landauer, The Ballistic MOSFET, The Velocity at the VS Model, Revisiting the VS Model **The Transmission Theory of the MOSFET:** Introduction, Transmission, MFP and Diffusion Coefficient, Transmission Theory of the MOSFET, Connection to the VS Model, Analysis of the Experiments, Limits and Limitations	
Unit – V	**10Hrs**
Advanced CMOS: New Materials and Device Structures (CMOS circuits, SOI MOSFETs, Heterostructure FETs, Nanotube FETs, Nanowire FETs, Novel steep subthreshold slope devices, Alternative devices (Excitons, Spin, Phase Transitions)	

Course Outcomes
After going through this course the student will be able to:

CO1	Describe the physics of semiconductor, basic theory of Metal Semiconductor Contacts and PN junction, MOS & transport mechanism
CO2	Apply the VLSI device paraemetrs and calculate the device performance
CO3	Analyze various modern VLSI devices && compare its performances with MOS devices
CO4	Evaluate or design the transport mechanism and modelling for emerging devices

Reference Books

1.	Advanced Semiconductor Fundamentals, 2nd Edition, R. F. Pierret, Prentice Hall, ISBN No. 0-13-061792-X.
2.	Fundamentals of Modern VLSI Devices, 2nd Edition, Yuan Taur and Tak H. Ning, Cambridge University Press, 2009, ISBN No. 9780521832946.
3.	Introduction to Semiconductor Devices: For Computing and Telecommunications Applications Kevin F Brennan , Cambridge University Press; 1 edition,, ISBN No. 978-0521831505
4.	Operation and Modeling of the MOS Transitor, Y.P. Tsividis, Colin McAndrew, 3rd Edition, Oxford Univ Press,2014, ISBN:978-0195170153

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
ANALOG IC DESIGN (Theory & Practice)						
Course Code	**:**	**18MVE21**		**CIE Marks**	**:**	**100+50**
Credits L:T:P	**:**	**3:1:1**		**SEE Marks**	**:**	**100+50**
Hours	**:**	**39L+26T+26P**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**8 Hrs**

MOS transistors: Components available in a CMOS process, MOS small signal models, concept of $f_{T,}$ noise model.

Single stage Amplifiers: Basic concepts, dc analysis, small signal analysis and noise analysis of common source and common gate stage, power, bandwidth, impedance and frequency scaling of circuits, Frequency response of CS amplifier, Cascode stage- Folded Cascode.

Current Mirror: Basic Current Mirrors, Cascode current Mirrors, amplifiers biased at constant currents.

Unit – II	**8 Hrs**

Differential Amplifiers: Single ended and differential operation, Common mode response, differential pair with active loads, Gilbert cell

Operational Amplifier: One stage op-amp, two stage op-amp, Telescopic Cascodeopamp, Telescopic Cascodeopamp frequency response, Folded Cascodeopamp-dc gain, Telescopic and folded Cascodeopamp-noise, mismatch, slew rate, Two stage opamp-topology, frequency response, gain boosting, common mode feedback.

Unit – III	**8 Hrs**

Noise: Resistors, MOSFET,Input and output referred noise, noise scaling, basic amplifier stages – CS and CG stage

Feedback: Non-idealities- finite dc gain, effect of additional poles & zeros, feedback topologies, sense and return mechanisms, effect of loading, effect of feedback on noise, feedback circuit analysis using return ratio – closed loop gain and impedance using return ratio

Unit – IV	**8 Hrs**

Stability analysis and Frequency compensation: Stability of Feedback: Basic Concepts, Instability and the Nyquist Criterion. Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation

Band gap reference: Band gap reference, Constant current and constant gm bias generators, reducing supply sensitivity

Low dropout regulators: Basic requirements and constraints

Unit – V	**7 Hrs**

Phase Locked Loops : Simple Phase locked loop, Charge pump PLL, Non-ideal effects - Jitter & Phase noise, Applications

Analog Layout techniques: General layout considerations – design rules, antenna effect, layout techniques for multi finger transistors, symmetry, reference distribution, passive devices, interconnects, Electro static discharge (ESD) protection, substrate coupling

Lab Component	**2 Hrs/Week**

1. Study of DC and small signal models of a MOS Transistor
2. Design of MOS current sources and mirrors
3. Design of single stage amplifiers – CS Amplifier with different loads
4. Design of a MOS Differential amplifier with an active load
5. Design of a cascode amplifier , double cascode and triple cascode amplifier
6. Design of Telescopic opamp
7. Design of a 2-stage CMOS Op-Amp
8. Design of Band Gap Reference circuit
9. Post-layout simulation of any two circuits

Course Outcomes **After going through this course the student will be able to:**	
CO1	Define & demonstrate device, circuit & system aspects of analog IC design
CO2	Analyze the functionality of analog circuits & systems
CO3	Design and implement analog integrated circuits & systems
CO4	Evaluate the different performance parameters of analog integrated circuits & systems using CAD tools.

Reference Books	
1.	Design of Analog CMOS Integrated Circuits,BehzadRazavi, McGrawHill Edition, 2002, ISBN: 0-07-238032-2
2.	CMOS Circuit Design, Layout and Simulation, R. Jacob Baker, Harry W. Li and David E. Boyce, IEEE Press, 2002, ISBN: 81-203-1682-7
3.	Analysis and design of Analog Integrated Circuits,Gray, Hurst, Lewis, and Meyer: 4th Edition, John Wiley & Sons, ISBN-10: 0470245999
4.	CMOS Analog Circuit Design, Phillip E. Allen and Douglas R. Holberg, 2nd Edition Oxford University Press, February 2002, *ISBN*: 9780199765072

Scheme of Continuous Internal Evaluation (CIE): Total marks: 100+50=150

Scheme of Continuous Internal Evaluation (CIE): Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks.

Continuous Internal Evaluation (CIE): Practical (50 Marks)
The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Scheme of Semester End Examination (SEE): Practical (50 Marks)
SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

Semester End Evaluation (SEE): Total marks: 100+50=150

Theory (100 Marks) + Practical (50 Marks) =Total Marks (150)

SEMESTER : II						
SYSTEMVERILOG FOR DESIGN AND VERIFICATION						
Course Code	**:**	**18MVE22**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**3:1:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L +26T**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **7Hrs**

Introduction to SystemVerilog:
SystemVerilog standards, Key SystemVerilog enhancements for hardware design.Advantages of System Verilog over Verilog, Data Types: Verilog data types, System Verilog data types, 2 - State Data types, Bit, byte, shortint, int, longint. 4 - State data types. Logic, Enumerated data types, User Defined data types, Struct data types, Strings, Packages, Type Conversion: Dynamic casting, Static Casting, Memories: Arrays, Dynamic Arrays, Multidimensional Arrays, Packed Arrays, Associative Arrays, Queues, Array Methods, Tasks and Functions: Verilog Tasks and Functions.

Unit – II **8Hrs**

Connecting the Testbench and Design:
Verilog interface signals - Limitations of Verilog interface signals, SystemVerilog interfaces, SystemVerilog port connections, Interface instantiation 2.4. Interfaces Arguments, Interface Modports, Interface References, Tasks and functions in interface, Verilog Event Scheduler, SystemVerilog Event Scheduler, Clocking Block, Input and Output Skews, Typical Testbench Environment, Verification plan

Unit – III **8Hrs**

OOPs Basics and Advanced OOPs concepts:
Basic OOP Concepts
Overview of Classes, Properties and Methods in the Classes, Instance/Object Creation, New Constructor, Null Object handles, Accessing Members, this Keyword, Creating an Object, Objects Assignments, Copying an Object: Shallow Copy, Deep Copy
Advanced OOP Concepts
Inheritance: Concept of Inheritance, Super Keyword, Static properties**,** Overriding Methods**,** Polymorphism - $cast**,** Virtual Classes**,** Parameterized Classes

Unit – IV **8Hrs**

Constrained Randomization, Threads and Inter-process Communication:
Constrained Randomization
Random Variables - rand and randc, Randomize( ) Method - Pre/Post Randomize( ) methods, Constraints in the class, Rand_mode and constraint_mode, Constraint and Inheritance, Constraint Overriding, Set Membership, Distribution Constraints, Conditional Constraints - .implication (->),
if/else, Inline Constraints
Threads and Inter-process Communication
Threads, Fork-Join/Join_any/Join_none, Communication – Mailbox, Semaphore, Events, BuildingaTestbenchwithThreadsandIPC

Unit – V **8Hrs**

Functional Coverage andAssertion Based Verification:
Functional Coverage
Coverage Definition, Code Coverage, Functional Coverage: Cover Group, Creating Cover Group Instances, Coverpoints, Bins - . implicit bins, . Explicit bins, Bin creation, Vector and Scalar bins, Cross products, Intersect, Select Expressions, Conditional Expression (iff), Illegal bins, Ignore bins, Coverage Analysis, Covergroup Built-in Methods - . Sample(), . get_coverage(), .get_instance_coverage(), .set_instance_name(string), .start(), . stop()
Assertion Based Verification
Introduction, Types of Assertions - . Immediate, Concurrent, Assertion Properties- . Writing Properties, Sequences. Sequence Composition. and or intersect.

Course Outcomes
After going through this course the student will be able to:

CO1	Demonstrate the use of System Verilog data types for digital system design and functional verification.
CO2	Demonstrate the skill on writing test-benches for design of digital systems and connecting them with

	the design.
CO3	Verify and Analyze the complete systems through robust verification methods such as assertion based verification.
CO4	Design and verify the digital systems such as FIFOs, memories, ATM interfaces, etc. using the learnt methods and demonstrate the skills.

Reference Books

1.	SystemVerilog for Design - A Guide to Using SystemVerilog for Hardware Design and Modeling, Stuart Sutherland, Simon Davidmann and Peter Flake, 2E, Springer Science, ISBN-13: 978-0387-3339-91, 2006.
2.	SystemVerilog for Verification-A Guide to Learning the Testbench Language Features, C Spear, Springer Science, IEEE press, ISBN-13: 978-0387-2703-64,2006.
3.	SystemVerilog golden reference guide-A concise guide to SystemVerilogDoulos,IEEE Standard-1800-2009, Version 5.0,ISBN: 0-9547345-9-9, 2012.
4.	Step-by-Step Functional Verification with SystemVerilog and OVM, SasanIman, Hansen Brown Publishing Company,ISBN-13: 978-0-9816-5621-2, 2008.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
RESEARCH METHODOLOGY (Common to all programs)						
Course Code	**:**	**18IM23**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**08 Hrs**

Overview of Research

Research and its types, identifying and defining research problem and introduction to different research designs. Essential constituents of Literature Review. Basic principles of experimental design, completely randomized, randomized block, Latin Square, Factorial.

Unit – II	**08 Hrs**

Data and data collection

Overview of probability and data types Primary data and Secondary Data, methods of primary data collection, classification of secondary data, designing questionnaires and schedules.

Sampling Methods: Probability sampling and Non-probability sampling

Unit – III	**08 Hrs**

Processing and analysis of Data

Statistical measures of location, spread and shape, Correlation and regression, Hypothesis Testing and ANOVA. Interpretation of output from statistical software tools

Unit – IV	**08 Hrs**

Advanced statistical analyses

Non parametric tests, Introduction to multiple regression, factor analysis, cluster analysis, principal component analysis. Usage and interpretation of output from statistical analysis software tools.

Unit-V	**07 Hrs**

Essentials of Report writing and Ethical issues

Significance of Report Writing , Different Steps in Writing Report, Layout of the Research Report , Ethical issues related to Research, Publishing, Plagiarism

Case studies: Discussion of case studies specific to the domain area of specialization

Course Outcomes

After going through this course the student will be able to:

CO1	Explain the principles and concepts of research types, data types and analysis procedures.
CO2	Apply appropriate method for data collection and analyze the data using statistical principles.
CO3	Present research output in a structured report as per the technical and ethical standards.
CO4	Create research design for a given engineering and management problem situation.

Reference Books

1	Research Methodology Methods and techniques by, Kothari C.R., New Age International Publishers, 4th edition, ISBN: 978-93-86649-22-5
2	Management Research Methodology, Krishnaswami, K.N., Sivakumar, A. I. and Mathirajan, M., Pearson Education: New Delhi, 2006. ISBN: 978-81-77585-63-6
3	The Research Methods Knowledge Base, William M. K. Trochim, James P. Donnelly, 3rd Edition, Atomic Dog Publishing, 2006. ISBN: 978-1592602919
4	Statistics for Management, Levin, R.I. and Rubin, D.S., 7th Edition, Pearson Education: New Delhi.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
MINOR PROJECT						
Course Code	**:**	**18MCN24**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**0:0:2**		**SEE Marks**	**:**	**100**
Hours/Week	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES

1. Each project group will consist of maximum of two students.
2. Each student / group has to select a contemporary topic that will use the technical knowledge of their program of study after intensive literature survey.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The number of projects that a faculty can guide would be limited to four.
5. The minor project would be performed in-house.
6. The implementation of the project must be preferably carried out using the resources available in the department/college.

Course Outcomes

After completing the course, the students will be able to:

CO1	Conceptualize, design and implement solutions for specific problems.
CO2	Communicate the solutions through presentations and technical reports.
CO3	Apply resource managements skills for projects.
CO4	Synthesize self-learning, team work and ethics.

Scheme of Continuous Internal Examination

Evaluation will be carried out in 3 phases. The evaluation committee will comprise of 4 members: Guide, Two Senior Faculty Members and Head of the Department.

Phase	Activity	Weightage
I	Synopsys submission, Preliminary seminar for the approval of selected topic and objectives formulation	20%
II	Mid term seminar to review the progress of the work and documentation	40%
III	Oral presentation, demonstration and submission of project report	40%

** Phase wise rubrics to be prepared by the respective departments

CIE Evaluation shall be done with weightage / distribution as follows:

- Selection of the topic & formulation of objectives 10%
- Design and simulation/ algorithm development/ experimental setup 25%
- Conducting experiments/ implementation / testing 25%
- Demonstration & Presentation 15%
- Report writing 25%

Scheme of Semester End Examination (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

- Brief write up about the project 05%
- Presentation / Demonstration of the Project 20%
- Methodology and Experimental results & Discussion 25%
- Report 20%
- Viva Voce 30%

SEMESTER : II						
VLSI TESTING (Professional Elective-C1)						
Course Code	**:**	**18MVE2C1**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**9 Hrs**
Introduction to Testing: Role of testing VLSI circuits, VLSI trends affecting testing, Physical Faults, Stuck-at Faults, Stuck open Faults, Permanent, Intermittent and Pattern Sensitive Faults, Delay Faults. **Fault Modeling-** Functional Testing, Structural Testing, Types of Fault Models, Stuck-at Faults, Bridging Faults, cross point faults, Fault Equivalence, Fault Dominance	
Unit – II	**9 Hrs**
Testability Measure – Controllability, Observability, SCOAP measures for combinational and sequential circuits. **ATPG for Combinational Circuits:** Path Sensitization Methods, Roth's D- Algorithm, Boolean Difference, PODEM Algorithm. Complexity of Sequential ATPG, Time Frame Expansion.	
Unit – III	**10 Hrs**
Design for Testability- Ad-hoc, Structured DFT- Scan method, Scan Design Rules, Overheads of Scan Design, partial scan methods, multiple chain scan methods. **Fault Simulation-** Fault Simulation algorithm- Serial, Parallel, Deductive and Concurrent Fault Simulation. **Boundary Scan Standard** - TAP Controller, Test Instructions.	
Unit – IV	**10 Hrs**
Self test And Test Algorithms Built-In self-Test, test pattern generation for BIST, response compaction - Parity checking, Ones counting, Transition Count, Signature analyzer.Circular BIST,BIST Architectures. Testable Memory Design Test Algorithms, Reduced Functional Faults-MARCH and MAT+ algorithm. Test generation for Embedded RAMs.	
Unit – V	**10 Hrs**
Fault Diagnosis Logical Level Diagnosis, Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits, Self-checking design, System Level Diagnosis.	

Course Outcomes

After completing the course, the students will be able to

CO1	Acquire knowledge about fault modeling & collapsing.
CO2	Analyse various combinational ATPG techniques
CO3	Evaluate the significance of sequential test pattern generation
CO4	Develop fault simulation techniques & fault diagnosis methods.

Reference Books:

1.	Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuits, Michael L.Bushnell, Vishwani D. Agrawal, Kluwer Academic Publications, 1999.
2.	Digital Systems Testing and Testable Design, MironAbramovici, Melvin A. Breuer, Arthur D. Friedman,, 3rd Edition, Jaico Publishing House, 2004
3.	Logical testing & design for testability, Hideo Fujiwara,, The MIT Press.
4.	Digital Circuit Testing and Testability, Parag.K.Lala, Academic Press.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
MACHINE LEARNING **(Professional Elective-C2)** **Common to VLSI, CS, CNE, DCE, BMI**						
Course Code	**:**	**18MCS2C2**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**10 Hrs**
Introduction: Overview of Probability Theory, Model Selection, Introduction to Machine learning. Linear Regression – Basis Function models, Bias Variance Decomposition, Bayesian linear Regression; Stochastic gradient Descent, Discriminant Functions, Bayesian Logistic regression. Examples on linear regression, logistic regression	
Unit – II	**11 Hrs**
Supervised Learning Kernel Methods: Dual representations, Construction of a kernel, Radial Basis Function Networks, Gaussian Process, Tree Based methods. Sparse Kernel Machines: Maximum margin classifiers (SVM), RVM. Examples on spam, mixer and k nearest neighbour	
Unit – III	**11 Hrs**
Unsupervised Learning **Mixture Models:** K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, The EM Algorithm in General, Principal Component Analysis, Probabilistic PCA. Examples on Market booklet analysis	
Unit – IV	**11 Hrs**
Random Forests Introduction, Definition of Random Forests, Details of Random ,Out of Bag Samples , Variable Importance, Proximity Plots, Random Forests and Over-fitting, Analysis of Random Forests, Variance and the De-Correlation Eff ect, Bias, Adaptive Nearest Neighbors.	
Unit –V	**09 Hrs**
Ensemble Learning Introduction, Boosting and Regularization Paths, Penalized Regression, The "Bet on Sparsity" Principle, Regularization Paths, Over-fitting and Margins, Learning Ensembles, Learning a Good Ensemble, Rule Ensembles	

Course Outcomes

After going through this course the student will be able to:

CO1	Explore the basics of Probability, data distributions and neural networks Algorithms.
CO2	Apply the various dimensionality reduction techniques and learning models for the given Application.
CO3	Analyze the different types of supervised and unsupervised learning models.
CO4	Evaluate the classification and regression algorithms for given data set.

Reference Books

1.	Pattern Recognition and Machine Learning, Christopher M Bishop, 2nd Edition, February 2006, Springer, ISBN-13: 978-0387-31073-2.
2.	The Elements of Statistical Learning, Trevor Hastie, Robert Tibshirani, and Jerome Friedman, 2nd Edition, 2008, Springer, ISBN 978-0-387-84858-7
3.	Data Mining – Concepts and Techniques, Jiawei Han and Micheline Kamber, Morgan Kaufmann, 3rd Edition, 2006,Elsevier, ISBN 1-55860-901-6
4.	Practical data science with R, Zumel, N., & Mount, J, 2014, Manning Publications ISBN 9781617291562

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
HIGH SPEED VLSI DESIGN (Professional Elective-C3)						
Course Code	**:**	**18MVE2C3**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**10 Hrs**
Introduction to high speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines	
Unit – II	**11 Hrs**
Power distribution and Noise: Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference. Power distribution on chips.	
Unit – III	**11 Hrs**
Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.	
Unit – IV	**11 Hrs**
Clocked & non clocked Logics: **Non clocked Logic Styles:**Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families **ClockedLogic Styles**:Single-Rail Domino Logic, Dual-Rail Domino Structures	
Unit –V	**09 Hrs**
Latching Strategies: Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques, DDR memories.	

Course Outcomes

After going through this course the student will be able to:

CO1	Investigate the special requirements that are imposed on high speed digital design.
CO2	Analyze the characteristics of transmission lines and high speed latches and circuits.
CO3	Analyze the Signaling convention in transmission media and high speed digital logics.
CO4	Evaluate the performance of various transmission lines and high speed digital circuits.

Reference Books

1	Digital Systems Engineering, William S. Dally & John W. Poulton, Cambridge University Press, 1998. ISBN 0-521-59292-5
2	High Speed CMOS Design Styles, Kerry Bernstein, Keith M. Carrig, Christopher M. Durham, Patrick R. Hansen, David Hogenmiller, Edward J. Nowak, Norman J. Rohrer.,Kluwer Academic Publishers in 1999, ISBN 978-1-4613-7549-4.
3	High Speed Digital Circuits, Masakazu Shoji, Addison Wesley Publishing Company, 1996. *ISBN* 978-0201634839.
4	High Speed Digital Design, Howard Johnson & Martin Graham, A Handbook of Black Magic, Prentice Hall PTR, 1993.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
LOW POWER VLSI DESIGN (Professional Elective-D1)						
Course Code	**:**	**18MVE2D1**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I — **10 Hrs**

Introduction and Algorithm Level Low power Methods:
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.
Algorithm Level low power Methods: Introduction, design flow, Algorithmic level analysis & optimization.

Unit – II — **10 Hrs**

Device & Technology Impact on Low Power:
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Unit – III — **9 Hrs**

Power estimation methods
Simulation Power analysis:
SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.
Probabilistic power analysis:
Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Unit – IV — **9 Hrs**

Low Power Design at Circuit level and Logic Level:
Low Power Design at Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.
Low Power Design at Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Unit – V — **10 Hrs**

Low power Design at Architecture/System Level and Clock distribution:
Low power Architecture & Systems: Architectural level estimation & synthesis, Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.
Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

Course Outcomes:
After going through this course the student will be able to:

CO1	Acquire the knowledge of the device physics, principles of analysis tools, circuits levels, logic levels and clock distribution techniques for low power designs.
CO2	Identify, formulate, and solve engineering system design problems using low power VLSI design approaches and engineering tools.
CO3	Use the techniques and skills in system designing through modern engineering tools such as logic works SPICE and description languages such as VHDL and Verilog.
CO4	Design digital systems, components or processes to meet the desired low power needs within realistic constraints and create a research oriented platform in thrust areas such as Energy recovery, Quantum computation, Adiabatic computation, etc.

Reference Books

1.	Low Power Design Methodologies, Jan M. Rabaey and MassoudPedram, Kluwer Academic Publishers, 5th reprint, ISBN 978-1-46 13-5975-3, 2002.
2.	Practical Low Power Digital VLSI Design, Gary K. Yeap, Kluwer Academic Publishers, ISBN 978-1-4613-7778-8, 2002.

3.	Low-Power CMOS VLSI Circuit DesignKaushik Roy and Sharat Prasad, John Wiley, 2000. ISBN 13 9788126520237
4.	Low-Power VLSI Circuits and Systems,Ajit Pal, Springer publications, ISBN: ISBN 978-81-322-1936-1, 2015

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
ADVANCED EMBEDDED PROCESSORS (Professional Elective-D2)						
Course Code	**:**	**18MVE2D2**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **10 Hrs**

Introduction
Embedded Processor Selection, PowerPC,ARM Cortex, SoC, Digital Signal Processors
ARM Cortex-M Series Technical Overview
Cortex-M Processor Family, Product Portfolio, Advantages, Applications, Cortex Microcontroller Software Interface Standard (CMSIS), General Information, Features

Unit – II **10 Hrs**

Architecture of ARM Cortex-M Processor
Programmer's Model, Application Program Status Register (APSR), Memory System, Exceptions & Interrupts, System Control Block, Debug, Reset & Reset Sequence
Instruction Set-I
Assembly Language Syntax, Suffixes for Assembly Instructions, Unified Assembly Language, Assembly Instructions

Unit – III **9 Hrs**

Instruction Set-II
Cortex-M4/M7 Specific Instructions, Barrel Shifter
Memory System
Memory Map, Connecting Cortex-M3/M4 with Memory & Peripherals, Endianness, Data Alignment & Unaligned Data Access Support, Bit Band Operations, Memory Access Attributes, Exclusive Access, Memory Barriers, Memory System in a MCU.

Unit – IV **9 Hrs**

Exceptions & Interrupts
Overview of Exceptions and Interrupts, Exception Types, Interrupt Management, Vector Table & Vector Table Relocation, Interrupts Inputs & Pending Behaviours, Exceptions Sequence
Overview, Details pf NVIC Registers for Interrupt Control, SCB Registers for Exceptions & Interrupt Control, Special Registers for Exceptions Masking, Procedures in Setting up Interrupts, Software Interrupts. Exception Handler in C, Stack Frames, Exception Sequences.

Unit – V **10 Hrs**

Low Power and System Control Features
Low Power Designs, Low Power Features, Using WFI & WFE Instructions in for Programming, Developing Low Power Applications, The SysTick Timer, Self-Reset, CPU ID Base Register, Configuration Control Register, Auxiliary Control Registers, Co-Processor Access Control Register.
OS Support Features
Shadowed Stack Pointer, SVC Exception, PendSV Exception, Context Switching in Action, Exclusive Accesses.

Course Outcomes
After going through this course the student will be able to:

CO1	Understand the architecture, instruction set, memory organization and addressing modes of the embedded processors.
CO2	Realize real time signal processing applications & primitive OS operations on different ARM architectures by making use of software libraries.
CO3	Perform market survey of available embedded processors & arrive at the required processor for solving the given problem statement.
CO4	Engage in self-study to formulate, design, implement, analyze and demonstrate

Reference Books	
1.	The Definitive Guide to the ARM Cortex-M3& M4 Processors, Joseph Yiu, , 3rd Edition, Newnes (Elsevier), 2014, ISBN:978-93-5107-175-4
2.	ARM System Developers Guide, Andrew N Sloss, Dominic Symes, Chris Wright, Elsevier, Morgan Kaufman publishers, 2008, ISBN-13:9788181476463
3.	ARM System on Chip Architecture, Steve Furber, Pearson Education Limited, 2nd Edition,2000, ISBN-13:9780201675191
4.	Technical reference manual for ARM processor cores, including Cortex M3, M4, M7 processor families.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
VLSI DIGITAL SIGNAL PROCESSING SYSTEMS (Professional Elective-D3) (Common to VLSI & ES and CS)						
Course Code	**:**	**18MVE2D3**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**10Hrs**
Introduction to digital Signal Processing systems Introduction, Typical DSP algorithms, DSP Application demands and scaled CMOS technologies, Representations of DSP algorithms.	
Unit – II	**10Hrs**
Pipelining and parallel processing Introduction, Pipelining of FIR Digital filters, parallel processing, pipelining and parallel processing for low power.	
Unit – III	**10Hrs**
Algorithmic strength reduction in filters and transforms Introduction, parallel FIR filters, Discrete Cosine transform and inverse DCT, Parallel architectures for Rank-Order Filters.	
Unit – IV	**9 Hrs**
Pipelined and parallel Recursive and Adaptive Filters Introduction, Pipeline interleaving in digital Filters, pipelining in 1st order IIR digital filters, Pipelining in higher order IIR Digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low power IIR digital Filter Design using Pipelining and parallel processing, Pipelined Adaptive Digital Filters.	
Unit – V	**9 Hrs**
Programmable digital Signal Processor Introduction, evolution of programmable Digital Signal processors, Important feature of DSP processors, DSP Processors for Mobile and wirelesses communication, Processor for multimedia signal Processing.	

Course Outcomes
After going through this course the student will be able to:

CO1	Develop a strong grounding in the fundamentals of VLSI digital signal processing ,
CO2	Understand DSP architectures and CMOS technologies to describe, analyze, and solve problems in VLSI digital signal processing.
CO3	Evaluate and test the modern VLSI digital signal processing systems using simulation tool.
CO4	Design suitable algorithm for specific applications & Develop applications using general purpose digital signal processors

Reference Books

1	VLSI Digital Signal processing systems :Design and implementation", Keshab K. Parthi , Wiley 1999,ISBN: 81-265-1098-6.
2	Digital Signal Processing and applications with C6713 and C6416 DSK, Rulph chasseing, Wiley 2005.
3.	Digital Signal Processing System Design: Lab view based hybrid programming, Nasser Kehtarnavaz, Academic press 2008.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
BUSINESS ANALYTICS (Global Elective-G01)						
Course Code	**:**	**18CS2G01**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I — **08 Hrs**

Business analytics

Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics.

Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling.

Unit – II — **08 Hrs**

Trendiness and Regression Analysis

Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

Unit – III — **08 Hrs**

Organization Structures of Business analytics

Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, Predictive Analytics, Predicative Modelling, Predictive analytics analysis.

Unit – IV — **08 Hrs**

Forecasting Techniques

Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Unit –V — **07 Hrs**

Decision Analysis

Formulating Decision Problems, Decision Strategies with and without Outcome, Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

Course Outcomes

After going through this course the student will be able to:

CO1	Explore the concepts, data and models for Business Analytics.
CO2	Analyze various techniques for modelling and prediction.
CO3	Design the clear and actionable insights by translating data.
CO4	Formulate decision problems to solve business applications

Reference Books

1	Business analytics Principles, Concepts, and Applications FT Press Analytics, Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, 1st Edition, 2014, ISBN-13: 978-0133989403, ISBN-10: 0133989402
2	The Value of Business Analytics: Identifying the Path to Profitability, Evan Stubs , John Wiley & Sons, ISBN:9781118983881 |DOI:10.1002/9781118983881,1st Edition 2014
3	Business Analytics, James Evans, Pearsons Education 2nd Edition, ISBN-13: 978-0321997821 ISBN-10: 0321997824
4	Predictive Business Analytics Forward Looking Capabilities to Improve Business, Gary Cokins and Lawrence Maisel, Wiley; 1st Edition, 2013.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
INDUSTRIAL AND OCCUPATIONAL HEALTH AND SAFETY (Global Elective-G02)						
Course Code	**:**	**18CV2G02**		**CIE**	**:**	**100 Marks**
Credits L: T: P	**:**	**3:0:0**		**SEE**	**:**	**100 Marks**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

UNIT – I	**7 Hrs**
Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and fire fighting, equipment and methods.	
UNIT – II	**9 Hrs**
Occupational health and safety: Introduction, Health, Occupational health: definition, Interaction between work and health, Health hazards, workplace, economy and sustainable development, Work as a factor in health promotion. Health protection and promotion Activities in the workplace: National governments, Management, Workers, Workers' representatives and unions, Communities, Occupational health professionals. Potential health hazards: Air contaminants, Chemical hazards, Biological hazards, Physical hazards, Ergonomic hazards, Psychosocial factors, Evaluation of health hazards: Exposure measurement techniques, Interpretation of findings recommended exposure limits. Controlling hazards: Engineering controls, Work practice controls, Administrative controls. Occupational diseases: Definition, Characteristics of occupational diseases, Prevention of occupational diseases.	
UNIT – III	**9 Hrs**
Hazardous Materials characteristics and effects on health: Introduction, Chemical Agents, Organic Liquids, Gases, Metals and Metallic Compounds, Particulates and Fibers, Alkalies and Oxidizers, General Manufacturing Materials, Chemical Substitutes, Allergens, Carcinogens, Mutagens, Reproductive Hazards, Sensitizers and Teratogens, Recommended Chemical Exposure Limits. Physical Agents, Noise and Vibration, Temperature and Pressure, Carcinogenicity, Mutagenicity and Teratogenicity. Ergonomic Stresses: Stress-Related Health Incidents, Eyestrain, Repetitive Motion, Lower Back Pain, Video Display Terminals.	
UNIT – IV	**7 Hrs**
Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.	
UNIT – V	**7 Hrs**
Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, over hauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.	

Course Outcomes
After successful completion of this course the student will be able to:

CO1	Explain the Industrial and Occupational health and safety and its importance.
CO2	Demonstrate the exposure of different materials, occupational environment to which the employee Can expose in the industries.
CO3	Characterize the different type materials, with respect to safety and health hazards of it.

CO4	Analyze the different processes with regards to safety and health and the maintenance required in The industries to avoid accidents.

Reference Books

1.	Maintenance Engineering Handbook, Higgins & Morrow, SBN 10: 0070432015 / ISBN 13: 9780070432017, Published by McGraw-Hill Education. Da Information Services.
2.	H. P. Garg, Maintenance Engineering Principles, Practices & Management, 2009,S. Chand and Company, New Delhi, ISBN:9788121926447
3.	Fundamental Principles of Occupational Health and Safety, Benjamin O. ALLI, Second edition,2008 International Labour Office – Geneva: ILO, ISBN 978-92-2-120454-1
4.	Foundation Engineering Handbook, 2008, Winterkorn, Hans, Chapman & Hall London. ISBN:8788111925428.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
MODELING USING LINEAR PROGRAMMING (Global Elective-G03)						
Course Code	**:**	**18IM2G03**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**08 Hrs**
Linear Programming: Introduction to Linear Programming problem **Simplex methods:** Variants of Simplex Algorithm – Use of Artificial Variables	
Unit – II	**08 Hrs**
Advanced Linear Programming : Two Phase simplex techniques, Revised simplex method **Duality:** Primal-Dual relationships, Economic interpretation of duality	
Unit – III	**08 Hrs**
Sensitivity Analysis: Graphical sensitivity analysis, Algebraic sensitivity analysis - changes in RHS, Changes in objectives, Post optimal analysis - changes affecting feasibility and optimality	
Unit – IV	**08 Hrs**
Transportation Problem: Formulation of Transportation Model, Basic Feasible Solution using North-West corner, Least Cost, Vogel's Approximation Method, Optimality Methods, Unbalanced Transportation Problem, Degeneracy in Transportation Problems, Variants in Transportation Problems.	
Unit –V	**07 Hrs**
Assignment Problem: Formulation of the Assignment problem, solution method of assignment problem-Hungarian Method, Variants in assignment problem, Travelling Salesman Problem (TSP).	

Course Outcomes
After going through this course the student will be able to:

CO1	Explain the various Linear Programming models and their areas of application.
CO2	Formulate and solve problems using Linear Programming methods.
CO3	Develop models for real life problems using Linear Programming techniques.
CO4	Analyze solutions obtained through Linear Programming techniques.

Reference Books

1	Operation Research An Introduction, Taha H A, 8th Edition, 2009, PHI, ISBN: 0130488089.
2	Principles of Operations Research – Theory and Practice, Philips, Ravindran and Solberg – John 2nd Edition, 2000, Wiley & Sons (Asia) Pvt Ltd, ISBN 13: 978-81-265-1256-0
3	Introduction to Operation Research, Hiller, Liberman, Nag, Basu, 9th Edition, 2012, Tata McGraw Hill ISBN 13: 978-0-07-133346-7
4	Operations Research Theory and Application, J K Sharma, 4th Edition, 2009, Pearson Education Pvt Ltd, ISBN 13: 978-0-23-063885-3.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.
Total CIE (Q+T+A) is 20+50+30=100 Marks.

Scheme of Semester End Examination (SEE) for 100 marks:
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
PROJECT MANAGEMENT (Global Elective-G04)						
Course Code	**:**	**18IM2G04**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **08 Hrs**

Introduction: Project Planning, Need of Project Planning, Project Life Cycle, Roles, Responsibility and Team Work, Project Planning Process, Work Breakdown Structure (WBS), Introduction to Agile Methodology.

Unit – II **08 Hrs**

Capital Budgeting: Capital Investments: Importance and Difficulties, phases of capital budgeting, levels of decision making, facets of project analysis, feasibility study – a schematic diagram, objectives of capital budgeting

Unit – III **08 Hrs**

Project Costing: Cost of Project, Means of Finance, Cost of Production, Working Capital Requirement and its Financing, Profitability Projections, Projected Cash Flow Statement, Projected Balance Sheet, Multi-year Projections, Financial Modeling, Social Cost Benefit Analysis

Unit – IV **08 Hrs**

Tools & Techniques of Project Management: Bar (GANTT) chart, bar chart for combined activities, logic diagrams and networks, Project evaluation and review Techniques (PERT) Critical Path Method (CPM), Computerized project management

Unit-V **07 Hrs**

Project Management and Certification: An introduction to SEI, CMMI and project management institute USA – importance of the same for the industry and practitioners. PMBOK 6 - Introduction to Agile Methodology, Themes / Epics / Stories, Implementing Agile.

Domain Specific Case Studies on Project Management: Case studies covering project planning, scheduling, use of tools & techniques, performance measurement.

Course Outcomes

After going through this course the student will be able to:

CO1	Explain project planning activities that accurately forecast project costs, timelines, and quality.
CO2	Evaluate the budget and cost analysis of project feasibility.
CO3	Analyze the concepts, tools and techniques for managing projects.
CO4	Illustrate project management practices to meet the needs of Domain specific stakeholders from multiple sectors of the economy (i.e. consulting, government, arts, media, and charity organizations).

Reference Books

1	Project Planning Analysis Selection Financing Implementation & Review, Prasanna Chandra, 8th Edition, 2010, Tata McGraw Hill Publication, ISBN 0-07-007793-2.
2	A Guide to the Project Management Body of Knowledge (PMBOK Guide), Project Management Institute, 5th Edition, 2013, ISBN: 978-1-935589-67-9
3	Project Management A System approach to Planning Scheduling & Controlling, Harold Kerzner, 11th Edition, 2013, John Wiley & Sons Inc., ISBN 978-1-118-02227-6.
4	Project Management – Planning and Controlling Techniques, Rory Burke, 4th Edition, 2004, John Wiley & Sons, ISBN: 9812-53-121-1

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks:
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
ENERGY MANAGEMENT (Global Elective-G05)						
Course Code	**:**	**18CH2G05**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit-I	**08 Hrs**
Energy conservation: Principles of energy conservation, Energy audit and types of energy audit, Energy conservation approaches, Cogeneration and types of cogeneration, Heat Exchangers and classification.	
Unit-II	**08 Hrs**
Wet Biomass Gasifiers: Introduction, Classification of feedstock for biogas generation, Biomass conversion technologies: Wet and dry processes, Photosynthesis, Biogas generation, Factors affecting bio-digestion, Classification of biogas plants, Floating drum plant and fixed dome plant their advantages and disadvantages	
Unit –III	**08 Hrs**
Dry Biomass Gasifiers : Biomass energy conversion routes, Thermal gasification of biomass, Classification of gasifiers, Fixed bed systems: Construction and operation of up draught and down draught gasifiers.	
Unit –IV	**08Hrs**
Solar Photovoltaic: Principle of photovoltaic conversion of solar energy, Types of solar cells and fabrication. **Wind Energy:** Classification, Factors influencing wind, WECS & classification.	
Unit –V	**07 Hrs**
Alternative liquid fuels: Introduction, Ethanol production: Raw materials, Pre-treatment, Conversion processes with detailed flow sheet. Gasification of wood: Detailed process, Gas purification and shift conversion, Biofuel from water hyacinth.	

Course Outcomes
After successful completion of this course the student will be able to:

CO1	Understand the use alternate fuels for energy conversion
CO2	Develop a scheme for energy audit
CO3	Evaluate the factors affecting biomass energy conversion
CO4	Design a biogas plant for wet and dry feed

Reference Books

1	Nonconventional energy, Ashok V Desai, 5th Edition, 2011, New Age International (P) Limited, ISBN 13: 9788122402070.
2	Biogas Technology - A Practical Hand Book, Khandelwal K C and Mahdi S S, Vol. I & II, 1986, McGraw-Hill Education, ISBN-13: 978-0074517239.
3	Biomass Conversion and Technology, Charles Y Wereko-Brobby and Essel B Hagan, 1st Edition, 1996, John Wiley & Sons, ISBN-13: 978-0471962465.
4	Solar Photovoltaics: Fundamental Applications and Technologies, C. S. Solanki, 2nd Edition, 2009, Prentice Hall of India, ISBN: 9788120343863.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks.

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
INDUSTRY 4.0 (Global Elective-G06)						
Course Code	**:**	**18ME2G06**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **07Hrs**

Introduction: Industrial, Internet, Case studies, Cloud and Fog, M2M Learning and Artificial Intelligence, AR, Industrial Internet Architecture Framework (IIAF), Data Management.

Unit – II **08Hrs**

The Concept of the IIoT: Modern Communication Protocols, Wireless Communication Technologies, Proximity Network Communication Protocols, TCP/IP, API: A Technical Perspective, Middleware Architecture.

Unit – III **08Hrs**

Data Analytics in Manufacturing: Introduction, Power Consumption in manufacturing, Anomaly Detection in Air Conditioning, Smart Remote Machinery Maintenance Systems with Komatsu, Quality Prediction in Steel Manufacturing.

Internet of Things and New Value Proposition, Introduction, Internet of Things Examples, IoTs Value Creation Barriers: Standards, Security and Privacy Concerns.

Advances in Robotics in the Era of Industry 4.0, Introduction, Recent Technological Components of Robots, Advanced Sensor Technologies, Artificial Intelligence, Internet of Robotic Things, Cloud Robotics.

Unit – IV **08 Hrs**

Additive Manufacturing Technologies and Applications: Introduction, Additive Manufacturing (AM) Technologies, Stereo lithography, 3DP, Fused Deposition Modeling, Selective Laser Sintering, Laminated Object Manufacturing, Laser Engineered Net Shaping, Advantages of Additive Manufacturing, Disadvantages of Additive Manufacturing.

Advances in Virtual Factory Research and Applications, The State of Art, The Virtual Factory Software , Limitations of the Commercial Software

Unit –V **08 Hrs**

Augmented Reality: The Role of Augmented Reality in the Age of Industry 4.0, Introduction, AR Hardware and Software Technology, Industrial Applications of AR, Maintenance , Assembly, Collaborative Operations , Training.

Smart Factories: Introduction, Smart factories in action, Importance, Real world smart factories, The way forward.

A Roadmap: Digital Transformation, Transforming Operational Processes, Business Models, Increase Operational Efficiency, Develop New Business Models.

Course Outcomes
After going through this course the student will be able to:

CO1	Understand the opportunities, challenges brought about by Industry 4.0 for benefits of organizations and individuals
CO2	Analyze the effectiveness of Smart Factories, Smart cities, Smart products and Smart services
CO3	Apply the Industrial 4.0 concepts in a manufacturing plant to improve productivity and profits
CO4	Evaluate the effectiveness of Cloud Computing in a networked economy

Reference Books

1	Industry 4.0 the Industrial Internet of Things, Alasdair Gilchrist, Apress Publisher, ISBN-13 (pbk): 978-1-4842-2046-7
2	Industry 4.0: Managing The Digital Transformation, Alp Ustundag, Emre Cevikcan, Springer, 2018 ISBN 978-3-319-57869-9.
3	Designing the industry - Internet of things connecting the physical, digital and virtual worlds, Ovidiu Vermesan and Peer Friess, Rivers Publishers, 2016 ISBN 978-87-93379-81-7
4	The concept Industry 4.0- An Empirical Analysis of Technologies and Applications in Production Logistics, Christoph Jan Bartodziej, Springer Gabler, 2017 ISBN 978-3-6581-6502-4.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
ADVANCED MATERIALS (Global Elective-G07)						
Course Code	**:**	**18ME2G07**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**07 Hrs**
Classification and Selection of Materials: Classification of materials. Properties required in Engineering materials, Criteria of selection of materials. Requirements / needs of advance materials.	
Unit – II	**08 Hrs**
Non Metallic Materials: Classification of n on metallic materials, Rubber: Properties, processing and applications. Plastics: Thermosetting and Thermoplastics, Applications and properties. Ceramics: Properties and applications. Adhesives: Properties and applications. Optical fibers: Properties and applications. Composites : Properties and applications.	
Unit – III	**08 Hrs**
High Strength Materials: Methods of strengthening of alloys, Materials available for high strength applications, Properties required for high strength materials, Applications of high strength materials	
Unit – IV	**08 Hrs**
Low & High Temperature Materials Properties required for low temperature applications, Materials available for low temperature applications, Requirements of materials for high temperature applications, Materials available for high temperature applications, Applications of low and high temperature materials.	
Unit –V	**08 Hrs**
Nanomaterials: Definition, Types of nanomaterials including carbon nanotubes and nanocomposites, Physical and mechanical properties, Applications of nanomaterials	

Course Outcomes
After going through this course the student will be able to:

CO1	Describe metallic and non metallic materials
CO2	Explain preparation of high strength Materials
CO3	Integrate knowledge of different types of advanced engineering Materials
CO4	Analyse problem and find appropriate solution for use of materials.

Reference Books

1	The Science & Engineering of Materials, Donald R. Askeland, and Pradeep P. Fulay, 5th Edition, Thomson, 2006, ISBN-13-978-0534553968
2	Nanotechnology, Gregory L. Timp, 1999th Editionmm Springer, 1999 ISBN-13: 978-0387983349
3	Material Science and Metallurgy, Dr. VD Kodgire and Dr. S V Kodgire, 42nd Edition 2018, Everest Publishing House ISBN NO: 81 86314 00 8
4	Processing and Fabrication of Advanced Materials, N Bhatnagar, T S Srivatsan, 2008, IK International, ISBN: 978819077702

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
COMPOSITE MATERIALS SCIENCE AND ENGINEERING (Global Elective-08)						
Course Code	**:**	**18CHY2G08**		**CIE Marks**	**:**	**100**
Credits L:T:P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit-I	**08 Hrs**

Introduction to composite materials

Fundamentals of composites – need for composites – Enhancement of properties – Classification based on matrix- Polymer matrix composites (PMC), Metal matrix composites (MMC), Ceramic matrix composites (CMC) – Constituents of composites, Interfaces and Interphases, Distribution of constituents, Types of Reinforcements, Particle reinforced

composites, Fibre reinforced composites. Fiber production techniques for glass, carbon and ceramic fibers Applications of various types of composites.

Unit – II	**08 Hrs**

Polymer matrix composites (PMC)

Polymer resins – Thermosetting resins, Thermoplastic resins & Elastomers,

Reinforcement fibres-Types, Rovings, Woven fabrics. PMC processes – Hand Layup Processes, Spray up processes – Compression Moulding – Injection Moulding – Resin Transfer Moulding – Pultrusion – Filament winding – Injection moulding. Glass fibre and carbon fibre reinforced composites (GFRP & CFRP). Laminates- Balanced Laminates, Symmetric Laminates, Angle Ply Laminates, Cross Ply Laminates. Mechanical Testing of PMC- Tensile Strength, Flexural Strength, ILSS, Impact Strength- As per ASTM Standard. Applications of PMC in aerospace, automotive industries**.**

Unit -III	**08 Hrs**

Ceramic matrix composites and special composites

Engineering ceramic materials – properties – advantages – limitations – monolithic ceramics

– need for CMC – ceramic matrix – various types of ceramic matrix composites- oxide ceramics – non oxide ceramics – Aluminium oxide – silicon nitride – reinforcements – particles- fibres- whiskers. Sintering – Hot pressing – Cold Isostatic Pressing (CIPing) – Hot isostatic pressing (HIPing). Applications of CMC in aerospace, automotive industries- Carbon /carbon composites – advantages of carbon matrix – limitations of carbon matrix carbon fibre – chemical vapour deposition of carbon on carbon fibre perform. Sol-gel technique- Processing of Ceramic Matrix composites.

Unit –IV	**07 Hrs**

Metal matrix composites

Characteristics of MMC, various types of metal matrix composites alloy vs. MMC, advantages of MMC, limitations of MMC, Reinforcements – particles – fibres. Effect of reinforcement – volume fraction – rule of mixtures. Processing of MMC – powder metallurgy process – diffusion bonding – stir casting – squeeze casting, a spray process,

Liquid infiltration In-situ reactions-Interface-measurement of interface properties- applications of MMC in aerospace, automotive industries.

Unit –V	**08 Hrs**

Polymer nano composites

Introduction and Significance of polymer Nano composites. Intercalated And Exfoliated Nanocomposites. Classification of Nano fillers- nanolayers, nanotubes, nanoparticles. Preparation of Polymer Nano composites by Solution, In-situ Polymerization and melt mixing techniques. Characterization Of polymer nanocomposites- XRD, TEM, SEM and AFM. Mechanical and Rheological properties of Polymer Nano composites. Gas barrier,

Chemical-Resistance, Thermal and Flame retardant properties of polymer nanocomposites. Optical properties and Biodegradability studies of Polymer nanocomposites, Applications of polymer nano-composites.	
Course Outcomes **After completing the course, the students will be able to:**	
CO1	Understand the purpose and the ways to develop new materials upon proper combination of known materials.
CO2	Identify the basic constituents of a composite materials and list the choice of materials available
CO3	Will be capable of comparing/evaluating the relative merits of using alternatives for important engineering and other applications.
CO4	Get insight to the possibility of replacing the existing macro materials with nano-materials
Reference Books	
1	Composite Materials Science and Engineering, Krishan K Chawla, 3rd Edition Springer-verlag Gmbh,2012 , ISBN: 978-0387743646
2	The Science and Engineering of Materials, K Balani, Donald R Askeland, 6th Edition- Cengage, Publishers,2013, ISBN: 13: 978-8131516416
3	Polymer Science and Technology, Joel R Fried , 2nd Edition, Prentice Hall, 2014, ISBN: 13: 978-0137039555
4	Nanomaterials and nanocomposites, Rajendra Kumar Goyal , 2nd Edition, CRC Press-Taylor & Francis, 2010, ISBN: 10-9781498761666, 1498761666

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
PHYSICS OF MATERIALS (Global Elective-09)						
Course Code	**:**	**18PHY2G09**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I **08 Hrs**

Crystal Structure

Discussion of lattice and lattice parameters, seven crystals systems, crystal planes, Miller indices, Interplanar distance, Packing fraction, Structure of different crystals-NaCl and Diamond, Bragg's law, Powder method, Bragg's spectrometer, Qualitative Analysis of Crystal structure using XRD,
Reciprocal lattice, Crystal defects-Point, Line, Planar and Volume defects.

Unit – II **08 Hrs**

Dielectric Materials

Basic concepts, Langevin's Theory of Polarisation, Types of Polarisation, Dipolar relaxation, Frequency Dependence of total polarization (polarizability as a function of frequency), Qualitative discussion of Internal Field and Claussius Mossotti, Dielectric loss spectrum, Dielectric strength, Dielectric Breakdown, Breakdown mechanisms in solid dielectrics, Applications of Solid Insulating materials in capacitors and Liquid insulating materials in Transformers, Dielectric Heating, Piezoelectricity, Direct and Inverse Piezoelectric effect,

Coupling factor, spontaneous polarization, Piezolelectricty in Quartz, Various piezoelectric materials- PZT, PVDF, Ferroelectricity, Barium titanate, Poling in Ceramics.

Unit – III **08 Hrs**

Magnetic Materials

Review of Dia, Para and Ferromagnetic materials, Weiss theory of Ferromagnetism, Hysteresis effect, Magnetostriction, Anti-ferromagnetism, Ferrimagnetsim, Soft and Hard magnetic materials, examples and applications in Transformer cores and Magnetic storage devices, Superconductors, properties, Types of Superconductors, BCS theory, High Temperature Superconductors, Applications in Cryotron and SQUID.

Unit – IV **07 Hrs**

Semiconducting Materials

Semiconductors-Direct and Indirect band gap semiconductors, Importance of Quantum confinement-quantum wires and dots, size dependent properties, Top down approach, Fabrication process by Milling and Lithography, Bottom up approach, fabrication process by vapour phase expansion and vapor phase condensation, Polymer semi-conductors-Photo conductive polymers, Applications.

Unit –V **08 Hrs**

Novel Materials

Smart materials-shape memory alloys, Austenite and Martensite phase, Effect of temperature and mechanical load on phase transformation, Pseudoeleasticity, Transformation hysteresis, Superelasticity, Characterization technique-Differntial Scanning calorimetry, Preparation technique- spin coating, Nitinol, CuAlNi alloy and applications.

Biomaterials-Metallic, ceramic and polymer biomaterials, Titanium and Titanium alloys, Carbon nanotubes, Graphene- Properties and Applications.

Course Outcomes

After going through this course the student will be able to:

CO1	Apply the principles of Physics in Engineering.
CO2	Apply the knowledge of Physics for material analysis.
CO3	Identify and Analyze Engineering Problems to achieve practical solutions.
CO4	Develop solutions for Problems associated with Technologies.

Reference Books

1.	Solid State Physics, S O Pillai, 6th Edition, New Age International Publishers, ISBN 10-8122436978.

2.	Introduction to Solid State Physics, C.Kittel, 7th Edition, 2003, John Wiley & Sons, ISBN 9971-51-780
3.	Engineering Physics, Dr.M N Avadhanulu, Dr. P G Kshirsagar, S Chand Publishing, Reprint 2015.
4.	The Science and Engineering of Materials, Askeland, Fulay, Wright, Balanai, 6th Edition, Cengage Learning, ISBN-13:978-0-495-66802-2.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : II						
ADVANCED STATISTICAL METHODS (Global Elective-G10)						
Course Code	**:**	**18MAT2G10**		**CIE Marks**	**:**	**100**
Credits L: T: P	**:**	**3:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**39L**		**SEE Duration**	**:**	**3 Hrs**

Unit – I	**07 Hrs**
Sampling Techniques: Concepts of random sampling from finite and infinite populations, Simple random sampling (with replacement and without replacement), Sampling distribution of proportions, Expectation and standard error of sample mean and proportion, Sampling distributions of differences and sums.	
Unit – II	**08 Hrs**
Estimation: Point estimation, Estimator and estimate, Criteria for good estimates - unbiasedness, consistency, efficiency and sufficiency, Method of moment's estimation and maximum likelihood estimation, Confidence intervals-population mean (large sample).	
Unit – III	**08 Hrs**
Tests of Hypothesis: Principles of Statistical Inference, Formulation of the problems with examples. Simple and composite hypotheses. Null and alternative hypotheses. Tests - type I and type II error, Testing of mean and variance of normal population (one sample and two samples), Exact and asymptotic tests of proportions. Chi squared test for goodness of fit (Relevant case studies).	
Unit – IV	**07 Hrs**
Linear Statistical Models: Definition of linear model and types, One way ANOVA and two way ANOVA models-one observation per cell, multiple but equal number of observation per cell (Relevant case studies).	
Unit –V	**09 Hrs**
Linear Regression: Simple linear regression, Estimation of parameters, Properties of least square estimators, Estimation of error variance, Multivariate data, Multiple linear regressions, Multiple and partial correlation, Autocorrelation-introduction and plausibility of serial dependence, sources of autocorrelation, Durbin-Watson test for auto correlated variables.	

Course Outcomes
After going through this course the student will be able to:

CO1	Identify and interpret the fundamental concepts of sampling techniques, estimates and types, hypothesis, linear statistical models and linear regression arising in various fields engineering.
CO2	Apply the knowledge and skills of simple random sampling, estimation, null and alternative hypotheses, errors, one way ANOVA, linear and multiple linear regressions.
CO3	Analyse the physical problem to establish statistical/mathematical model and use appropriate statistical methods to solve and optimize the solution.
CO4	Distinguish the overall mathematical knowledge gained to demonstrate the problems of sampling techniques, estimation, tests of hypothesis, regression and statistical model arising in many practical situations.

Reference Books

1.	Fundamentals of Statistics (Vol. I and Vol. II), A. M. Goon, M. K. Gupta and B. Dasgupta, 3rd Edition, 1968, World Press Private Limited, ISBN-13: 978-8187567806.
2.	Applied Statistics and Probability for Engineers, Douglas C. Montgomery and George C. Runger, 6th Edition, John Wiley & Sons, 2014, ISBN:13 9781118539712, ISBN (BRV):9781118645062.
3.	Fundamentals of Mathematical Statistic-A Modern Approach, S.C. Gupta and V.K. Kapoor, 10th Edition, 2000, S Chand Publications, ISBN: 81-7014-791-3.
4.	Regression Analysis: Concepts and Applications, F. A. Graybill and H. K. Iyer, Belmont, Calif, 1994, Duxbury Press, ISBN-13: 978-0534198695.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks

Scheme of Semester End Examination (SEE) for 100 marks
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SYLLABUS

FOR

SEMESTER III & IV

SEMESTER : III						
SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS (Theory)						
Course Code	**:**	**18MVE31**		**CIE Marks**	**:**	**100**
Credit L:T:P	**:**	**4:1:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L+26T**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**11 Hrs**
Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization. **Graphs**: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.	
Unit – II	**11 Hrs**
Schedule Algorithms: A model for scheduling problems, Scheduling wither source and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. **Hardware Modelling**: Hardware Modelling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, dataflow and sequencing graphs, compilation and optimization techniques.	
Unit –III	**10 Hrs**
Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.	
Unit –IV	**10 Hrs**
Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.	
Unit –V	**10 Hrs**
Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models. **Cell Library Binding**: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table FPGAs and Anti fuse based FPGAs), rule based library binding.	

Course Outcomes **After completing the course, the students will be able to:**	
CO1:	Understand and apply the various algorithms and graphs to synthesis and optimization of different digital circuit.
CO2:	Analyze the performance of standard algorithm used for synthesis and optimization of two level, multiple level and sequential logic circuits
CO3:	Demonstrate the improvement of optimization techniques used for digital circuits
CO4:	Develop an algorithm for synthesis and optimization

Reference Books	
1	Synthesis and Optimization of Digital Circuits, Giovanni De Micheli, 2003, Tata McGraw-Hill, ISBN: 978-0-07-058278-1
2	Logic Synthesis, Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, 1994, McGraw-Hill, USA, ISBN: 978-0-07-016500-7
3	Finite State Machine Datapath Design, Optimization, and Implementation, Justin Davis, Robert Reese,1st edition, 2007, Morgan & Claypool Publishers, ISBN-13: 978-1598295290
4	Principles of CMOS VLSI Design: A System Perspective, Neil Weste and K. Eshragian, 2nd Edition, 2000, Pearson Education (Asia) Pvt Ltd., ISBN: 978-0-20-153376-7

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks.

Scheme of Semester End Examination (SEE) for 100 marks:
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER: III						
INTERNSHIP						
Course Code	**:**	**18MVE32**		**CIE Marks**	**:**	**100**
Credit L:T:P	**:**	**0:0:5**		**SEE Marks**	**:**	**100**
Hours/week	**:**	**10**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES

1) The duration of the internship shall be for a period of 8 weeks on full time basis after II semester final exams and before the commencement of III semester.
2) The student must submit letters from the industry clearly specifying his / her name and the duration of the internship on the company letter head with authorized signature.
3) Internship must be related to the field of specialization of the respective PG programme in which the student has enrolled.
4) Students undergoing internship training are advised to report their progress and submit periodic progress reports to their respective guides.
5) Students have to present the internship activities carried out to the departmental committee and only upon approval by the committee, the student can proceed to prepare and submit the hard copy of the final internship report. However, interim or periodic reports as required by the industry / organization can be submitted as per the format acceptable to the respective industry /organizations.
6) The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be Ivory color for PG circuit Programs and Light Blue for Non-Circuit Programs.
7) The broad format of the internship final report shall be as follows
    - Cover Page
    - Certificate from College
    - Certificate from Industry / Organization
    - Acknowledgement
    - Synopsis
    - Table of Contents
    - Chapter 1 - Profile of the Organization: Organizational structure, Products, Services, Business Partners, Financials, Manpower, Societal Concerns, Professional Practices,
    - Chapter 2 - Activities of the Department
    - Chapter 3 - Tasks Performed: summaries the tasks performed during 8-week period
    - Chapter 4 – Reflections: Highlight specific technical and soft skills that you acquired during internship
    - References & Annexure

Course Outcomes:

After going through the internship the student will be able to:

CO1: Apply engineering and management principles
CO2: Analyze real-time problems and suggest alternate solutions
CO3: Communicate effectively and work in teams
CO4: Imbibe the practice of professional ethics and need for lifelong learning.

Scheme of Continuous Internal Evaluation (CIE):

The evaluation committee shall consist of Guide, Professor/Associate Professor and Assistant Professor. The committee shall assess the presentation and the progress reports in two reviews.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
Review-I	Explanation of the application of engineering knowledge in industries, ability to comprehend the functioning of the organization/ departments,	45%
Review-II	Importance of resource management, environment and sustainability presentation skills and report writing	55%

Scheme for Semester End Evaluation (SEE):
The SEE examination shall be conducted by an external examiner (domain expert) and an internal examiner. Evaluation shall be done in batches, not exceeding 6 students per batch.

SEMESTER: III						
MAJOR PROJECT: PHASE-I						
Course Code	**:**	**18MVE33**		**CIE Marks**	**:**	**100**
Credit L:T:P	**:**	**0:0:5**		**SEE Marks**	**:**	**100**
Hours/week	**:**	**10**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES

1. The Major Project work comprises of Phase-I and Phase-II. Phase-I is to be carried out in third semester and Phase-II in fourth semester.
2. The total duration of the Major project Phase-I shall be for 16 weeks.
3. Major project shall be carried out on individual student basis in his/her respective PG programme specialization. Interdisciplinary projects are also considered.
4. The allocation of the guides shall be preferably in accordance with the expertise of the faculty.
5. The project may be carried out on-campus/industry/organization with prior approval from Internal Guide, Associate Dean and Head of the Department.
6. Students have to complete Major Project Phase-I before starting Major Project Phase-II.
7. The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be Ivory color for PG circuit Programs and Light Blue for Non-Circuit Programs.

Course Outcomes :

After going through this course the students will be able to:

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate life-long learning

Scheme of Continuous Internal Examination (CIE)

Evaluation shall be carried out in two reviews. The evaluation committee shall consist of Guide, Professor/Associate Professor and Assistant Professor.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
Review-I	Selection of the topic, Literature Survey, Problem Formulation and Objectives	45%
Review-II	Methodology and Report writing	55%

Scheme for Semester End Evaluation (SEE):

Major Phase-I evaluation shall be done by an external examiner (domain expert) and respective guide as per the schedule. Maximum of four candidates per batch shall be allowed to take examination. The batches are to be formed based on specific domain of work.

SEMESTER: III						
RADIO FREQUENCY IC DESIGN (Professional Elective- E1)						
Course Code	**:**	**18MVE3E1**		**CIE Marks**	**:**	**100**
Credit L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**10 Hrs**
Basic concepts in RF design - Nonlinearity and Time Variance, Effects of nonlinearity – harmonic distortion, gain compression, desensitization, cross modulation, intermodulation, cascaded nonlinear stages – level diagram. Noise in RF circuits – Noise figure, Noise figure of cascaded and lossy circuits, Sensitivity and dynamic range.	
Unit – II	**10 Hrs**
RF Systems Design - Receiver architectures - Heterodyne - dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, Image Reject – Hartley architecture, Transmitter architectures - Direct conversion and two-step transmitters.	
Unit –III	**11 Hrs**
RF Circuits Design (MOSFET circuits only) **Low noise Amplifier -** Performance parameters, Problem of Input matching, LNA topologies – Variants of common source only, design examples. **Mixer -** Mixer fundamentals, Performance parameters, Nonlinear systems as linear mixers, two port example –square law mixers, multiplier based mixers – Single balanced and double balanced (active and passive) - working and implementation, (MOSFET circuits only).	
Unit –IV	**11 Hrs**
Oscillator - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, VCO characteristics, Phase noise – basic concepts and effects of phase noise (no analysis). **Phase Locked Loop Design -** Type-II PLL: design equations, phase margin, and closed-loop PLL response, Design methodology for a Type-II 3rd –order PLL, charge pump design issues, Charge Pump design techniques: charge-injection, clock feed-through.	
Unit –V	**10 Hrs**
Frequency Synthesizers: General considerations, Basic Integer N synthesizer, settling behaviour, spur reduction techniques, PLL based modulation, Divider design – Pulse swallow divider, dual modulus divider, divider logic styles – current steering, CML latch, true single phase clocking. Fractional N synthesizers- basic concepts only.	

Course Outcomes

After completing the course, the students will be able to:

CO1: Apply the knowledge of RF circuits & systems in IC design
CO2: Analyze CMOS circuits and its impact on Radio frequency IC design.
CO3: Design and implement RF transceiver chain with specification.
CO4: Evaluate the different performance parameters used in RF design using CAD tools.

Reference Books

1	RF Microelectronics, Behzad Razavi, 2nd Edition, 2012, Pearson Education, ISBN: 978-9-33-251863-6
2	Radio Frequency Integrated Circuits Design, John Rogers ,Calvin Plett, 2003, Artech House, ISBN: 978-1-58-053502-1
3	The Design of CMOS Radio Frequency Integrated Circuits, Thomas H Lee , 2nd Edition, 2004, Cambridge University Press, ISBN: 978-0-52-183539-8
4	VLSI for Wireless Communications, Bosco Leung, 2004, Pearson Education, ISBN: 978-1-48-997377-1

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks.

Scheme of Semester End Examination (SEE) for 100 marks:
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER: III						
ARM PROGRAMMING AND OPTIMIZATION (Professional Elective- E2)						
Course Code	**:**	**18MVE3E2**		**CIE Marks**	**:**	**100**
Credit L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**11 Hrs**
Introduction, Data Path Architecture, Registers, Modes, Exceptions **Programming in C for ARM** Overview of C Compilers and optimization, basic C data types, C looping structures, register allocation, function calls, pointer aliasing, structure arrangement, bit fields, unaligned Data and Endianess, division, floating point, inline functions and inline assembly, portability issues.	
Unit – II	**11 Hrs**
Writing and Optimizing ARM Assembly Code Writing assembly code, profiling and cycle counting, instruction scheduling, register allocation, conditional execution, looping constructs, Bit manipulation, efficient switches. Handling unaligned data.	
Unit –III	**10 Hrs**
Digital Signal Processing on ARM Representing a digital signal, Introduction to DSP on the ARM, FIR filters: Realization of filters on ARM7 and Cortex M3, IIR Filters: Realization of filters on ARM7 and Cortex M3, CMSIS DSP Library.	
Unit –IV	**10 Hrs**
Firmware: Firmware and Boot loader **Embedded Operating Systems:** Fundamental Components, Simple Operating System.	
Unit –V	**10 Hrs**
Memory Protection Unit Over view of the MPU's, MPU registers, setting up the MPU, Memory barrier and memory configuration, Using sub-region disable, Consideration when using MPU, Other usages of MPU.	

Course Outcomes

After completing the course, the students will be able to:

CO1: Describe the programmer's model of ARM processor and analyse the instruction set architecture to realize complex operations.

CO2: Apply the optimization methods available for ARM architectures to design embedded software to meet given constraints with the help of modern engineering tools.

CO3: Realize real time signal processing applications & primitive OS operations on different ARM architectures by making use of software libraries.

CO4: Engage in self-study to formulate, design, implement, analyze and demonstrate an application realized on ARM development boards through assignments.

Reference Books

1	ARM System Developers Guide, Andrew N Sloss, Dominic Symes, Chris Wright, 2008, Elsevier, Morgan Kaufman publishers, ISBN-13:9788181476463
2	The definitive Guide to the ARM Cortex- M3 & M4 Processors, Joseph Yiu, 3rd Edition, 2014, Newnes (Elsevier), ISBN: 978-93-5107-175-4
3	ARM System on Chip Architecture, Steve Furber, 2nd Edition, 2001, Pearson Education Limited, ISBN-13:9780201675191
4	Technical reference manual for ARM processor cores, including Cortex M series, ARM 11, ARM 9 & ARM 7 processor families.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.
Total CIE (Q+T+A) is 20+50+30=100 Marks.

Scheme of Semester End Examination (SEE) for 100 marks:
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : III						
STATIC TIMING ANALYSIS (Professional Elective-E3)						
Course Code	**:**	**18MVE3E3**		**CIE Marks**	**:**	**100**
Credit L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Hours	**:**	**52L**		**SEE Duration**	**:**	**03 Hrs**

Unit-I	**11 Hrs**

Introduction: Basics of timing concepts- Propagation delay, slew, timing arcs, min and max timing paths, clock domains.

Delay Concepts for Digital Designing: Types of Delays in Digital Circuits, Different Cause for Delay

Timing parameters of digital circuits: Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design,Clock Concepts

The STA Environment- timing path groups, modeling of external attributes, virtual clocks, refining the timing analysis, point-to-point specification

Unit – II	**10 Hrs**

Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitics, Interconnects, Parasitic Extraction Formats, linear v/s. non-linear delay model. **Clock Network Optimization**: Metrics, clock skew-scheduling, handling variability.

Parallel Timing Optimization: Circuit partitioning for independent timing regions.

Post-Silicon Timing Validation: Introduction, sources of post-silicon timing failure, post-silicon tuning

Unit –III	**10 Hrs**

Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design: Cause for Crosstalk on Integrated Circuits, Crosstalk Prevention Methods

Unit –IV	**10 Hrs**

Constraints for STA: Clock Constraints, Other Timing Constraints, 5.2.2 External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate

Unit –V	**11 Hrs**

Timing Violations and Verification: Slack, Critical Path of Timing Report, Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Recovery and Removal Violation Check, Input/Output Timing Path Checks ,DRC Violation Check, Multi Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Setup Violations, Techniques to Fix Hold Violations, Time borrowing.

Course Outcomes

After completing the course, the students will be able to:

CO1: Ability to apply the learnt basic concepts of STA to evaluate the delay of the circuits and analyze the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing.

CO2: Ability to write their own constraint file and create the environment required for the given design and its specification to undergo for analysis using the EDA tool.

CO3: Ability to set constraints, Validate the results and analyze the reports

CO4: Ability to understand the journal research papers related to Timing analysis techniques and able to present the knowledge of new techniques for the given design.

Reference Books

1	Static Timing Analysis for Nanometer Designs: A Practical Approach, J. Bhasker, R. Chadha, 2009, Springer, ISBN: 978-0-387-93819-6, 978-0-387-93820-2(e-book).
2	Static Timing Analysis for VLSI circuits, R. Jayagowri, Pushpendra S. Yadav, 2018,

	MEDTECH, A Division of Scientific International , ISBN: 978-9-38-721006-6.
3	Timing Analysis and Optimization of Sequential Circuits, Naresh Maheshwari and Sachin S. Sapatnekar, 1999, Springer Science + Business Media, LLC, Library of Congress Cataloging-in-Publication Data, ISBN:978-1-4613-7579-1, 978-1-4615-5637-4 (eBook).
4	Constraining Designs for Synthesis and Timing Analysis - A Practical Guide to Synopsys Design Constraints (SDC), Sridhar Gangadharan and Sanjay Churiwala, Springer Science + Business Media, LLC, Library of Congress Cataloging-in-Publication Data, 2013, ISBN:978-1-4614-3268-5, 978-1-4614-3269-2 (eBook).

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of Quizzes (Q), Tests (T) and Assignments (A). A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. Three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) Solving innovative problems 2) Seminar/new developments in the related course 3) Laboratory/field work 4) Minor project.

Total CIE (Q+T+A) is 20+50+30=100 Marks.

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER : IV						
MAJOR PROJECT : PHASE-I						
Course Code	**:**	**18MVE41**		**CIE Marks**	**:**	**100**
Credit L:T:P	**:**	**0:0:20**		**SEE Marks**	**:**	**100**
Hours/Week	**:**	**40**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES

1. Major Project Phase-II is continuation of Phase-I.
2. The duration of the Phase-II shall be of 16 weeks.
3. The student needs to complete the project work in terms of methodology, algorithm development, experimentation, testing and analysis of results.
4. It is mandatory for the student to present/publish the work in National/International conferences or Journals
5. The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be Ivory color for PG circuit Programs and Light Blue for Non-Circuit Programs.

Course Outcomes

After going through this course the students will be able to:

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate life-long learning

Scheme of Continuous Internal Examination (CIE)

Evaluation shall be carried out in three reviews. The evaluation committee shall consist of Guide, Professor/Associate Professor and Assistant Professor.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
Review-I	Review and refinement of Objectives, Methodology and Implementation	20%
Review-II	Design, Implementation and Testing	40%
Review-III	Experimental Result & Analysis, Conclusions and Future Scope of Work, Report Writing and Paper Publication	40%

Scheme for Semester End Evaluation (SEE):

Major Project Phase-II SEE shall be conducted in two stages. This is initiated after fulfilment of submission of project report and CIE marks.

Stage-1 Report Evaluation

Evaluation of Project Report shall be done by guide and an external examiner.

Stage-2 Project Viva-voce

Major Project Viva-voce examination is conducted after receipt of evaluation reports from guide and external examiner.

Both Stage-1 and Stage-2 evaluations shall be completed as per the evaluation formats.

SEE procedure is as follows:

	Internal Guide	External Examiner	TOTAL	
SEE Report Evaluation	100 marks	100 marks		200 marks
			(A)	(200/2) = 100 marks

Viva-Voce	Jointly evaluated by Internal Guide & External Evaluator	(B)	100 marks
		Total Marks	**[(A)+(B)]/2 = 100**

SEMESTER : IV						
TECHNICAL SEMINAR						
Course Code	**:**	**18MVE42**		**CIE Marks**	**:**	**50**
Credit L:T:P	**:**	**0:0:2**		**SEE Marks**	**:**	**50**
Hours/Week	**:**	**4**		**SEE Duration**	**:**	**30 Mins**

GUIDELINES

1. The presentation shall be done by individual students.
2. The seminar topic shall be in the thrust areas of respective PG programme.
3. The seminar topic could be complementary to the major project work
4. The student shall bring out the technological developments with sustainability and societal relevance.
5. Each student must submit both hard and soft copies of the presentation along with the report.
6. The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be Ivory color for PG circuit Programs and Light Blue for Non-Circuit Programs.

Course Outcomes

After going through this course the student will be able to:

CO1: Identify topics that are relevant to the present context of the world
CO2: Perform survey and review relevant information to the field of study.
CO3: Enhance presentation skills and report writing skills.
CO4: Develop alternative solutions which are sustainable

Scheme of Continuous Internal Evaluation (CIE): Evaluation shall be carried out in two reviews. The evaluation committee shall consist of Guide, Professor/Associate Professor and Assistant Professor.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
Review-I	Selection of Topic, Review of literature, Technical Relevance, Sustainability and Societal Concerns, Presentation Skills	45%
Review-II	Technological Developments, Key Competitors, Report writing	55%

Scheme for Semester End Evaluation (SEE):

The SEE examination shall be conducted by an external examiner and an internal examiner. Evaluation shall be done in batches, not exceeding 6 students per batch.