RV COLLEGE OF ENGINEERING®

(Autonomous Institution Affiliated to VTU, Belagavi)

R.V. Vidyaniketan Post, Mysore Road

Bengaluru – 560 059

Scheme and Syllabus of III & IV Semesters

(Autonomous System of 2018 Scheme)

Master of Technology (M.Tech)

in

POWER ELECTRONICS

DEPARTMENT OF

ELECTRICAL AND ELECTRONICS ENGINEERING

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Department Vision

Attain technical excellence in Electrical and Electronics Engineering through graduate programs and interdisciplinary research related to sustainability in power, energy and allied fields.

Department Mission

- To provide technical education that combines rigorous academic study and the excitement of innovation enabling the students to engage in lifelong learning
- To establish Centre of Excellence in sustainable electrical energy, smart grids and systems
- To establish tie-ups with industries and institutions of repute and to foster building up of a wide knowledge base to keep in tune with upcoming technologies.
- To motivate commitment of faculty and students to collate, generate, disseminate, persevere, knowledge and to work for the benefit of society.
- To develop simple, appropriate and cost effective inclusive technologies which are instrumental in the up-liftment of the rural society.

ABBREVIATIONS

Sl. No.	Abbreviation	Meaning
1.	VTU	Visvesvaraya Technological University
2.	BS	Basic Sciences
3.	CIE	Continuous Internal Evaluation
4.	SEE	Semester End Examination
5.	CE	Professional Core Elective
6.	GE	Global Elective
7.	HSS	Humanities and Social Sciences
8.	CV	Civil Engineering
9.	ME	Mechanical Engineering
10.	EE	Electrical and Electronics Engineering
11.	EC	Electronics & Communication Engineering
12.	IM	Industrial Engineering & Management
13.	EI	Electronics & Instrumentation Engineering
14.	CH	Chemical Engineering
15.	CS	Computer Science & Engineering
16.	TE	Telecommunication Engineering
17.	IS	Information Science & Engineering
18.	BT	Biotechnology
19.	AS	Aerospace Engineering
20.	PHY	Physics
21.	CHY	Chemistry
22.	MAT	Mathematics

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R V COLLEGE OF ENGINEERNG, BENGALURU-560 059
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DEPARTMENT OF ELECTRICAL ENGINEERING
M.Tech in POWER ELECTRONICS

THIRD SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Total Credits**
1	18 MPE31	PLC and SCADA	EE	4	0	1	**5**
2	18 MPE3EX	Elective 5	EE	4	0	0	**4**
3	18 MPE33	Internship	EE	0	0	5	**5**
4	18 MPE34	Dissertation Phase I	EE	0	0	5	**5**
5	18 MPE31	PLC and SCADA	EE	4	0	1	**5**
6	18 MPE3EX	Elective 5	EE	4	0	0	**4**
Total number of Credits				8	0	11	**19**
Total Number of Hours / Week				8	0	11	**19**

III Semester		
GROUP E: CORE ELECTIVES		
Sl. No.	**Course Code**	**Course Title**
1.	18 MPE 3E1	Digital System Design
2.	18 MPE 3E2	High Voltage DC Transmission
3.	18 MPE 3E3	Nano materials and Devices

FOURTH SEMESTER CREDIT SCHEME							
Sl. No.	**Course Code**	**Course Title**	**BoS**	**Credit Allocation**			
				L	**T**	**P**	**Total Credits**
1	18MPE41	Dissertation Phase II	EE	0	0	20	20
2	18MPE42	Technical Seminar	EE	0	0	2	2
Total number of Credits				**0**	**0**	**22**	**22**
Total Number of Hours / Week				**0**	**0**	**22**	**22**

Semester: III						
Program Logic Controller and Supervisory Control & Data Acquisition (PLC and SCADA) (Theory and Practical)						
Course Code	**:**	**18MPE31**		**CIE Marks**	**:**	**100+50**
Credits: L:T:P	**:**	**4:0:1**		**SEE Marks**	**:**	**100+50**
Total Hours	**:**	**50L+16P**		**SEE Duration**	**:**	**3+3Hrs**

Course Learning Objectives (CLO):	
1	Recognize industrial control problems and access suitability of using PLC for control.
2	Understand PLC architecture including timers, counters, sequencers and Programme PLC's using ladder logic.
3	Compare different communication protocol in SCADA systems and integrate with PLC.
4	Select the essential elements and practices needed to develop and implement the Engineering Automation using PLC approach.

Unit-I	**10 Hrs**
Programmable Logic Controllers An Overview: Programmable Logic Controllers , Parts of a PLC ,Principles of Operation, Modifying the Operation , PLCs versus Computers, PLC Size and Application. **PLC Hardware Components:** The I/O Section, Discrete, Analog and Special I/O Modules, Typical Discrete and Analog I/O Module Specifications, The Central Processing Unit(CPU), Memory Design, Memory Types, Programming Terminal Devices, Recording and Retrieving Data, Human Machine Interfaces (HMIs)	
Unit – II	**10 Hrs**
Fundamentals of Logic: The Binary Concept , AND, OR, NOT and XOR Function, Boolean Algebra , Developing Logic Gate circuits, from Boolean Expressions, Producing the Boolean Equation for a Given Logic Gate Circuit, Hardwired Logic versus Programmed Logic, Programming Word Level Logic Instructions, **Basics of PLC Programming:** Processor Memory Organization, Program Files, Data Files, Program Scan, PLC Programming Languages, Relay-Type Instructions, Instruction Addressing, Branch Instructions, Internal Relay Instructions, Programming Examine If Closed and Examine If Open Instructions, Entering the Ladder Diagram, Modes of Operation.	
Unit -III	**10 Hrs**
Developing Fundamental PLC Wiring Diagrams and Ladder Logic Programs : Electromagnetic Control Relays, Contactors, Motor Starters, Manually Operated Switches, Mechanically Operated Switches, Output Control Devices, Seal-In Circuits, Latching Relays, Converting Relay Schematics into PLC, Ladder Programs, Writing a Ladder Logic Program, Directly from a Narrative Description **Programming Timers:** Mechanical Timing Relays**,** Timer Instructions, On-Delay Timer Instruction, Off-Delay Timer Instruction, Retentive Timer, Cascading Timers. **Interfacing with different sensors:** Proximity sensors Inductive, capacitive sensors, Photoelectric Sensors and Switches, Encoders, Temperature sensors, position and displacement sensors, pressure sensors.	
Unit –IV	**09 Hrs**
Programming Counters: Counter Instructions, Up-Counter, One-Shot Instruction, Down-Counter, Cascading Counters, Incremental Encoder-Counter, Applications, Combining Counter and Timer Functions **Program Control Instructions:** Master Control Reset Instruction, Jump Instruction, Subroutine Functions, Immediate Input and	

Immediate Output Instructions, Forcing External I/O Addresses, Safety Circuitry, Selectable Timed Interrupt , Fault Routine, Temporary End Instruction, Suspend instruction.

Data Manipulation Instructions:

Data Manipulation, Data Transfer Operations, Data Compare Instructions, Data Manipulation Programs Closed-Loop Control, Math Instructions, Addition Instruction, Subtraction Instruction, Multiplication Instruction Division Instruction.

Unit –V	**09 Hrs**

SCADA System:

History of Critical Infrastructure Directives, SCADA System Evolution, Definitions and Basic Architecture, SCADA Evolution, SCADA Definition, SCADA System Architecture, SCADA Applications, Redundancy as a Component of SCADA Security, SCADA System Desirable Properties.

SCADA Systems and its application:

Employment of SCADA Systems for various applications. (The Basic Refining Process, Nuclear Power Generation, The Boiling Water Reactor, The Pressurized Water Reactor, Conventional Electric Power Generation, Water Purification System , Crane Control)

SCADA Protocols:

Evolution of SCADA Protocols, Overview of the OSI Model, TCP/IP Model. MODBUS Model, DNP3 Protocol, UCA 2.0 and IEC61850 Standards, Controller Area Network, Device Net, Control Net , Ethernet/IP, Profibus.

UNIT VI Lab Component

PLC & AUTOMATION LAB

Unit-VI Lab Component

1. Simulation and verification of operation of relays, switches and pushbuttons using PLC(Usage of Digital I/o Modules)
2. PLC Program on concept of latching and interlocking
3. Interfacing of different Proximity sensors like Capacitive, inductive and infrared sensors to PLC.
4. Speed control of dc motor using PLC(Usage of Analog I/O Modules)
5. Programs on Timers and Counters.
6. Simulation and verification of Starting of Three Phase induction Motors Via Star-Delta Starter.
7. Verification of pneumatic applications using PLC.
8. Speed control of ac servo motor using programmable logic controller.
9. PLC program on Tank filling device simulator(Using Universal Simulator)
10. PLC program on Selective band switch (Using Universal Simulator)
11. Experiments on HMI or SCADA
12. Open Ended Experiment (to be Designed Executed by Students)

Course Outcomes: After completing the course, the students will be able to	
CO1:	Understand the basic concepts of PLC and SCADA systems.
CO2:	Assess the control needs of a process industry and evaluate various options of using PLC or SCADA
CO3:	Design and program the PLC to meet a specified control objective
CO4:	Build a complete control system through integration of sensor with PLC.

Reference Books	
1	Programmable Logic Controllers, Frank D. Petruzella, 4th Edition, 2010 McGraw-Hill Publisher, ISBN 13: 9780073510880
2	Securing SCADA System, Ronald L. Krutz, 1st Edition, 2015, Wiley Publications, ISBN-10: 9788126557349.
3	Programmable Logic Controllers, W.Bolton, 4th Edition, 2006, Elsevier ISBN-13: 978-0-7506-8112-4
4	Programmable Logic Controllers: Programming Methods and Applications, John R. Hackworth and Frederick D. Hackworth, Jr., 1st Eidtion, 2004, Pearson/Prentice Hall, ISBN-9780130607188.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)
CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

Scheme of Continuous Internal Evaluation (CIE) for Practicals: (50 Marks)
The Laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are rewarded for 10 marks. Total marks for the laboratory is 50.

Semester End Evaluation (SEE): Total marks: 100+50=150
Theory (100 Marks) + Practical (50 Marks) = Total Marks (150)

Scheme of Semester End Examination (SEE) for 100 marks:
The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit.

Scheme of Semester End Examination (SEE); Practical (50 Marks)
SEE for the practical courses will be based on experiment conduction with proper results, is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

Semester: III						
DIGITAL SYSTEM DESIGN (Elective Group E: Core Elective)						
Course Code	**:**	**18MPE3E1**		**CIE Marks**	**:**	**100**
Credits: L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Total Hours:	**:**	**50L**		**SEE Duration**	**:**	**3Hrs**

Course Learning Objectives (CLO):	
1	Compare methodologies and solve problems in sequential and combinational circuits
2	Analyse digital circuits and systems using ASM charts and Design digital circuits using programmable logic devices and FPGAs
3	Acquiring-depth knowledge of input/output modules, their timing parameters and the interfacing
4	Read data sheets of PLDs , analyse them and select appropriate device for a given Application

Unit-I	**10 Hrs**
Review of Digital Logic Design Fundamentals: Development and evolution digital devices, design and verification tools. Abstraction levels of digital system design. Designing of combinational circuits. Design of sequential circuits- Finite State machine; mealy and moore machines. Sequential packages;	
Unit – II	**10 Hrs**
Design Development flow : Overview of PLDs and EDA Software: Introduction of PLDs, general FPGAs devices, Overview of the hardware platform, EDA Tools: Integrated software Environment, creation of design project and HDL codes, test-bench and perform the RTL simulation, RTL Design with HDLs: Combinational circuits design and verification, regular sequential circuits and components, Finite state machine(FSM), Finite State Machine with Datapath (FSMD) code development of FSMD- design examples, CPU design, Algorithmic state machine charts (ASM), code conversion of ASM	
Unit –III	**10 Hrs**
Input / Output Modules: UART: Introduction, UART receiving subsystem, Oversampling procedure, Baud rate generator, UART receiver, Interface circuit, UART transmitting subsystem, Overall UART system, Complete UART core, example circuits. PS2: Introduction, PS2 receiving subsystem, Device-to-host communication protocol, Design and code, PS2 keyboard scan code, example circuits. External SRAM: Introduction, Specification of SRAM, Architectural Block diagram, Timing parameters, Timing requirement, Design ASMD chart, Timing analysis	
Unit –IV	**10 Hrs**
Customized Hardware and Software: Special-purpose FSMD, general-purpose microcontroller, embedded microcontrollers. Xilinx'sPico Blaze Overview: Overview of Pico Blaze, Internal Architecture, Development flow, Instruction set, Programming model, Instruction format, Interfacing, Interrupt handling, KCPSM3 directives Pico Blaze Assembly Code Development: Development tools- Xilinx's KCPSM3 and PBlazeIDE - Assembler directives, useful code constructs, control structure, subroutine development, example programme and their verification through PBlaze IDE	
Unit –V	**10 Hrs**
FPGA Implementation of Digital Circuits: Constraint files development, synthesis and implementation of HDL codes. Generation and downloading of the configuration file to a PLD device; Soft core microcontroller implementation: Picoblaze use in HDL design flow, implementation of programmed processor, development of SOPC.	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Formulate and solve problems in Sequential and combinational circuits
CO2:	Design digital circuits using HDL
CO3:	Implement digital systems using FPGA
CO4:	Develop design flow for SOPC

Reference Books	
1	Digital Design, Mano M. M. and Ciletti M. D., 4thEdition, 2008. Pearson Education, **ISBN:**9788131714508
2	Digital Systems Design Using VHDL, Charles H Roth Jr., 2nd Edition 1998, PWS Publishing Company, ***ISBN***-13: 978-0-495-66776-6, ***ISBN:*** 0-495-66776-5
3	The Design Warrior's Guide to FPGAs – Devices, Tools and Flows, Maxfield C. M., 1st Edition, 2004, Newnes. ISBN-13: 978-0750676045, ISBN-10: 0750676043
4	Fundamentals of Digital Logic with VHDL Design, Brown S. and Vranesic Z., 3rdEdition., 2008, Tata McGraw-Hill Publishing Company Limited., ISBN:9781259025976

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit.

HIGH VOLTAGE DC TRANSMISSION (Elective Group E: Core Elective)						
Course Code	**:**	**18MPE3E2**		**CIE Marks**	**:**	**100**
Credits: L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Total Hours:	**:**	**50L**		**SEE Duration**	**:**	**3Hrs**

Course Learning Objectives (CLO):	
1	Understand the modern trends in long distance DC transmission and related issues
2	Analyze the control strategies and the importance of reactors in DC transmission system
3	Analyze the reactive power control requirement for stable operation of the system
4	Design the DC reactor and converter control circuits for HVDC system

Unit-I	**10 Hrs**
HVDC Power Transmission Technology: Historical sketch, existing HVDC projects, Classification of HVDC links, Components of HVDC transmission system, Comparison of AC and DC Transmission, Application of DC Transmission, Modern trends in DC Transmission, Ground Return- advantages and disadvantages. Choice of converter configuration.	
Unit – II	**10 Hrs**
HVDC CONVERTER: Introduction to line commutated converter, analysis of six and twelve pulse converter without overlap. Effect of smooting reactor,. Two and three level voltage source converter, pulse width modulation. Analysis of converter two and three , three and four valve conduction. Conduction modes. 12 pulse detailed analysis	
Unit –III	**10 Hrs**
CONTROL OF CONVERTERS AND HVDC LINK: Converter control characteristics, firing angle control,CEA control, Starting and stopping of DC link, Power control , frequency control. Reactive power control, tap changer control. Control of voltage source converter. **CONVERTER FAULTS AND PROTECTION:** Converter faults, protection against over voltages, over currents in converter station. Surge arrester. Protection agains faults in voltage source converter.	
Unit –IV	**10 Hrs**
SMOOTHING REACTOR AND DC LINE: Smooting reactors, effects of corona loss, DC line insulators, Transient over voltages in DC line, protection in DC line. Detection and protection of faults, DC breakers. **REACTIVE POWER CONTROL:** Reactive power control in steady state and transient state. Sources of Reactive power, SVC and STATCOM.	
Unit –V	**10 Hrs**
POWER FLOW ANALYSIS IN AC/DC SYSTEM: Introduction to DC system model, procedure, inclusion of constraints, Power flow analysis under dynamic conditions, power flow with VSC based HVDC system. Introduction to stability concepts, analysis of voltage stability in asynchronous AC/DC system. **MULTI TERMINAL DC SYSTEM**: Introduction, types , control and protection.	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Understand the importance of modern long distance transmission technology, and related issues.
CO2:	Analyze the control of converter and faults in the system
CO3:	Evaluate the power control in AC/DC systems and its modeling.
CO4:	Design DC reactor, filters and transmission line as per the specifications.

Reference Books	
1	Direct current Transmission, Kimbark E.W. Vol 1, Wiley Interscience,1971. ISBN 0471475807, 9780471475804
2	High Voltage Direct Current Power Transmission system- Technology and Systems Interactions, Padiyar K R , 1992, Wiley Eastern Ltd, ISBN-13: 978-1906574772
3	High voltage direct current transmission, Arrillage , 1st Edition, 1983, Peter pregrinus Ltd., London, ISBN 0906048974, 9780906048979
4	High voltage direct current power transmission, Adamson C Hingorani N G, Grraway ltd, London, 1960.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit.

NANO MATERIALS AND DEVICES (Elective Group E: Core Elective)						
Course Code	**:**	**18MPE3E3**		**CIE Marks**	**:**	**100**
Credits: L:T:P	**:**	**4:0:0**		**SEE Marks**	**:**	**100**
Total Hours:	**:**	**50L**		**SEE Duration**	**:**	**3Hrs**

Course Learning Objectives (CLO):	
1	Understand the basic concepts of Nanotechnology
2	Familiarize with the properties of nanomaterials and their applications
3	Expose to nanoelectronic devices and their applications
4	Synthesize and characterize nano materials

Unit-I	**10 Hrs**
Introduction: Nanotechnology : Background and definition of nanotechnology –Types of nano materials-Microstructure – Properties – Application in different fields – Reliability issues of MEMS/NEMS. Atomic bonding in solids: Metallic, Ionic, Covalent, Co-ordination/dative bonds; Vander Waals interactions/Electrostatic interactions: Ion pair interactions, solvent effects, Ion-dipole and dipole – dipole interactions, Hydrogen bonding - hydrophobic interactions. MO theory for simple molecules , Size effect of Nanomaterials: Size, shape, density, melting point, wet ability, specific surface area, solid state phase transformation and band gap variation - Quantum confinement, Effect of strain on band gap in epitaxial quantum dots.	
Unit – II	**10 Hrs**
Bonding in Nanostructures : Graphene , Fullerenes , Carbon nanotubes , Bonding in armchair, zigzag and chiral structures , n-m=3q rule , Inorganic nanotubes: Silica nanotubes, boron nitride nanotubes, nanotubes of dichalcogenides and nanotubes of metal oxides, Reactivity on nanosurfaces: Functionalization of carbon nanotubes and Graphene.	
Unit –III	**10 Hrs**
Nanoscale MOSFETs: Challenges in miniaturization, quantum effects, thin oxides, random dopant fluctuations, tunneling and subthreshold currents, power density, hot electron effects, fundamental limits of MOS operations, MODFET (Modulation Doped FET), GaN based HEMT (High Electron Mobility Field Effect Transistors).	
Unit –IV	**10 Hrs**
Molecular Nanoelectronics: Molecular nanowires, organic LEDs, organic FETs, carbon nanotube and grapheme based FETs, Silicon nanowire based FETs, Nano-bioelectronics : DNA based biosensors, protein based biosensors, materials for biosensor applications, quantum dot based bioimaging, DNA based logic and computing elements	
Unit –V	**10 Hrs**
Synthesis and characterization of Nanomaterials : Nanomaterials synthesis and applications , Chemical methods : Gas phase synthesis , Liquid phase synthesis , Plasma vapor deposition , Spray synthesis; Extrusion forging, ECAP, Characterization : Description of AFM/FFM and various measurement techniques, TEM.	

Course Outcomes: After completing the course, the students will be able to	
CO1:	Explain structure and bonding of Nanomaterials
CO2:	Demonstrate knowledge of nano electronic devices and its applications
CO3:	Synthesize and characterize nano materials
CO4:	Use nano materials for industrial applications.

Reference Books	
1	Materials Science, M.S.Vijaya,G.Rangarajan, 1st Edition, 2014, Published by McGraw Hill Education (2014) ISBN: 9780070534698
2	Materials Science and Engg., V.Ragavan, 1st Edition, 2015, Published by Prentice-Hall of India Pvt.Ltd, ISBN-10: 9788120350922
3	Nanoelectronics- principles and devices, M. Dragoman and D. Dragoman, 2nd Edition, 2008, Artech House publishers, ISBN-9781596933682.
4	Introduction to Nanotechnology, Charles P. Poole and Frank J. Owens, 1st Edition, 2003, John Wiley & Sons. ISBN-13: 978-0471079354.

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of two quizzes are conducted and each quiz is evaluated for 10 marks adding up to 20 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The three tests are conducted for 50 marks each and the sum of the marks scored from three tests is reduced to 50 marks. A minimum of two assignments are given with a combination of two components among 1) solving innovative problems 2) seminar/new developments in the related course 3) Laboratory/field work 4) mini project. **Total CIE is 20+50+30=100 Marks.**

Scheme of Semester End Examination (SEE) for 100 marks:

The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one question from each unit.

INTERNSHIP						
Course Code	**:**	**18MPE33**		**CIE Marks**	**:**	**100**
Credits	**:**	**L:T:P**	**0:0:5**	**SEE Marks**	**:**	**100**
Hours/week	**:**	**10Hrs**		**SEE Duration**	**:**	**3 Hrs**

GUIDELINES FOR INTERNSHIP

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the process of applying engineering knowledge to produce product and provide services.

(2) Explain the importance of management and resource utilization

(3) Comprehend the importance of team work, protection of environment and sustainable solutions.

(4) Imbibe values, professional ethics for lifelong learning.

1) The duration of the internship shall be for a period of 8 weeks on full time basis between II semester final exams and beginning of III semester.
2) The student must submit letters from the industry clearly specifying his / her name and the duration of the internship on the company letter head with authorized signature.
3) Internship must be related to the field of specialization or the M.Tech program in which the student has enrolled.
4) Students undergoing internship training are advised to report their progress and submit periodic progress reports to their respective guides.
5) Students have to make a presentation on their internship activities in front of the departmental committee and only upon approval of the presentation should the student proceed to prepare and submit the hard copy of the internship final report. However interim or periodic reports and reports as required by the industry / organization can be submitted as per the format acceptable to the respective industry /organizations.
6) The reports shall be printed on bond paper – 80GSM, back to back print, with soft binding – A4 size with 1.5 spacing and times new roman font size 12.
7) The broad format of the internship final report shall be as follows
    - Cover Page
    - Certificate from College
    - Certificate from Industry / Organization
    - Acknowledgement
    - Synopsis
    - Table of Contents
    - Chapter 1 - Profile of the Organization – Organizational structure, Products, Services, Business Partners, Financials, Manpower, Societal Concerns, Professional Practices,
    - Chapter 2 - Activities of the Department -
    - Chapter 3 – Tasks Performed – summaries the tasks performed during 8 week period
    - Chapter 4 – Reflections – Highlight specific technical and soft skills that you acquired during internship
    - References & Annexure

Course Outcomes:

After going through the internship the student will be able to:

CO1: Apply engineering and management principles

CO2: Analyze real-time problems and suggest alternate solutions

CO3: Communicate effectively and work in teams

CO4: Imbibe the practice of professional ethics and need for lifelong learning.

1. Scheme of Continuous Internal Evaluation (CIE):

A committee comprising of the Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide would review the presentation and the progress reports in two phases. The evaluation criteria shall be as per the rubrics given below:

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

(1) Explanation of the application of engineering knowledge in industries 35%

(2) Ability to comprehend the functioning of the organization/ departments 20%

(3) Importance of resource management, environment and sustainability 25%

(4) Presentation Skills and Report 20%

Dissertation Phase 1						
Course Code	**:**	**18MPE34**		**CIE Marks**	**:**	**100**
Credits	**:**	**L:T:P**	**0:0:5**	**SEE Marks**	**:**	**100**
Hours	**:**	**10**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

The students shall be able to

1. Understand the method of applying engineering knowledge to solve specific problems.
2. Apply engineering and management principles while executing the project
3. Demonstrate good verbal presentation and technical report writing skills.
4. Identify and solve complex engineering problems using professionally prescribed standards.

GUIDELINES

1. Major project will have to be carried out by only one student in his/her area of interest.
2. Each student has to select a contemporary topic that will use the technical knowledge of their program of specialization.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The project can be carried out on-campus or in an industry or an organization with prior approval from the Head of the Department.
5. The standard duration of the project is for 16 weeks, however if the guide and the evaluation committee of the department, after the assessment feel that the work is insufficient and it has to be extended, then the student will have to continue as per the directions of the guide and the committee.
6. It is mandatory for the student to present his/her work in one of the international conferences or publish the research finding in a reputed unpaid journal with impact factor.

Course Outcomes:

After going through this course the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate life-long learning

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in THREE Phases. The evaluation committee will comprise of: guide, two senior faculty members, one industry member and Head of the Department.

Phase	Activity	Weightage
4th week	Topic approval along with Synopsis	20%
8th week	Literature survey with Problem Statement	20%
12th week	Motivation and Objectives	20%
15th week	Preliminary report for the approval of selected topic along with methodology.	40%

CIE Evaluation shall be done with marks distribution as follows:

- Selection of the topic 10%
- Literature review and framing of objectives 25%
- Defining the brief methodology along with the algorithm development/experimental setup 25%
- Presentation 20%
- Report writing 20%

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

1. Brief write-up about the project 5%
2. Formulation of Project Objectives & Methodology 20%
3. Presentation 25%
4. Report 20%
5. Viva Voce 30%

Dissertation Phase II						
Course Code	**:**	**18MPE41**		**CIE Marks**	**:**	**100**
Credits	**:**	**L:T:P**	**0:0:20**	**SEE Marks**	**:**	**100**
Hours/Week	**:**	**40**		**SEE Duration**	**:**	**3 Hours**

Course Learning Objectives:

The students shall be able to

1. Understand the method of applying engineering knowledge to solve specific problems.
2. Apply engineering and management principles while executing the project
3. Demonstrate good verbal presentation and technical report writing skills.
4. Identify and solve complex engineering problems using professionally prescribed standards.

GUIDELINES

1. Major project will have to be done by only one student in his/her area of interest.
2. Each student has to select a contemporary topic that will use the technical knowledge of their program of specialization.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The project can be carried out on-campus or in an industry or an organization with prior approval from the Head of the Department.
5. The standard duration of the project is for 16 weeks, however if the guide and the evaluation committee of the department, after the assessment feel that the work is insufficient and it has to be extended, then the student will have to continue as per the directions of the guide and the committee.
6. It is mandatory for the student to present his/her work in one of the international conferences or publish the research finding in a reputed unpaid journal with impact factor.

Course Outcomes:

After going through this course the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics, societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate life long learning

Scheme of Continuous Internal Examination (CIE)

Evaluation will be carried out in THREE Phases. The evaluation committee will comprise of: guide, two senior faculty members, one industry member and Head of the Department.

Phase II	Activity	Weightage
5th week	Review and refinement of Objectives and methodology.	20%
10th week	Mid-term progress review shall check the compliance with the objectives and methodology presented in Phase I, review the work performed.	40%
15th week	Oral presentation, demonstration and submission of project report. Outcome and publication	40%

CIE Evaluation shall be done with marks distribution as follows:

- Review of formulation of objectives and methodology 10%
- Design and simulation/ algorithm development/experimental setup 25%
- Conducting experiments / implementation / testing / analysis 25%
- Demonstration & Presentation 20%
- Report writing 20%

Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

1. Brief write-up about the project 5%
2. Formulation of Project Objectives & Methodology 20%
3. Experiments / Analysis Performed; Results & Discussion 25%
4. Report 20%
5. Viva Voce 30%

TECHNICAL SEMINAR						
Course Code	**:**	**18MPE42**		**CIE Marks**	**:**	**50**
Credits	**:**	**L:T:P**	**0:0:2**	**SEE Marks**		**50**
Hours/Week	**:**	**4**		**SEE Duration**		**30 min**

Course Learning Objectives (CLO):

The students shall be able to:

(1) Understand the technological developments in their chosen field of interest
(2) Explain the scope of work and challenges in the domain area
(3) Analyze these engineering developments in the context of sustainability and societal concerns.
(4) Improve his/her presentation skills and technical report writing skills

GUIDELINES

1) The presentation will have to be done by individual students.
2) The topic of the seminar must be in one of the thrust areas with in-depth review and analysis on a current topic that is relevant to industry or on-going research.
3) The topic could be an extension or complementary to the project
4) The student must be able to highlight or relate these technological developments with sustainability and societal relevance.
5) Each student must submit both hard and soft copies of the presentation.

Course Outcomes:

After going through this course the student will be able to:

CO1: Identify topics that are relevant to the present context of the world
CO2: Perform survey and review relevant information to the field of study.
CO3: Enhance presentation skills and report writing skills.
CO4: Develop alternative solutions which are sustainable

2. Scheme of Continuous Internal Evaluation (CIE): Evaluation would be carried out in TWO phases. The evaluation committee shall comprise of Head of the Department / Associate Dean, Associate Professor, Assistant Professor and Guide. The evaluation criteria shall be as per the rubrics given below:

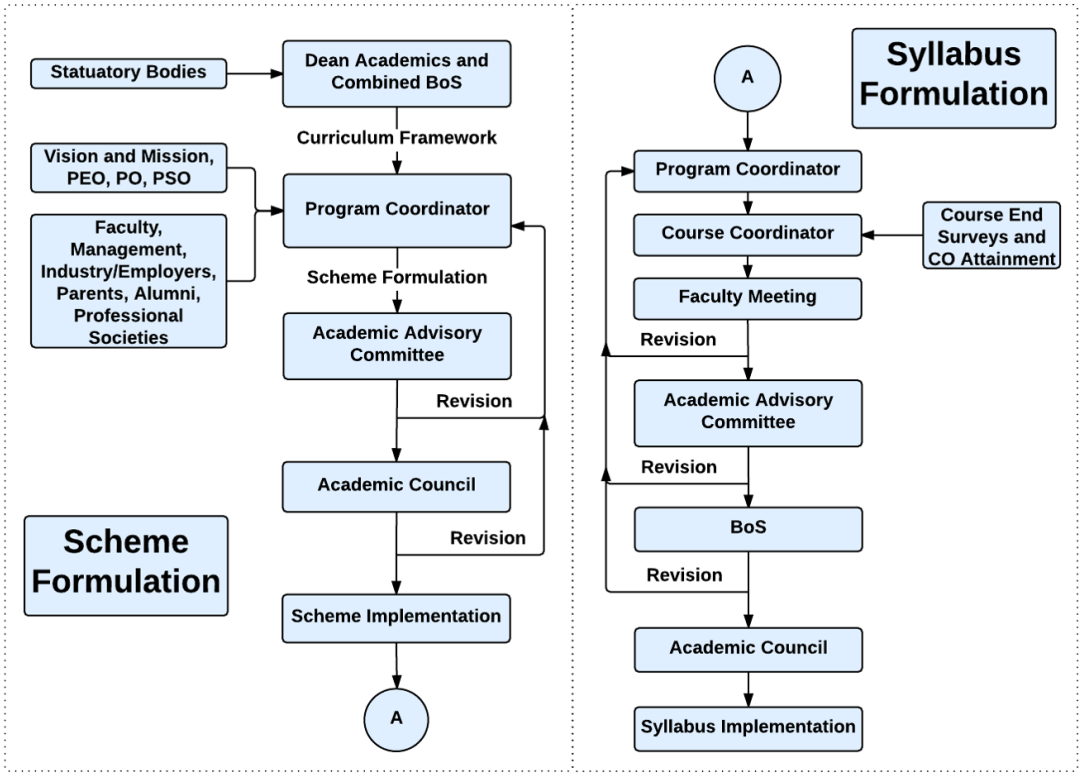
Scheme for Semester End Evaluation (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

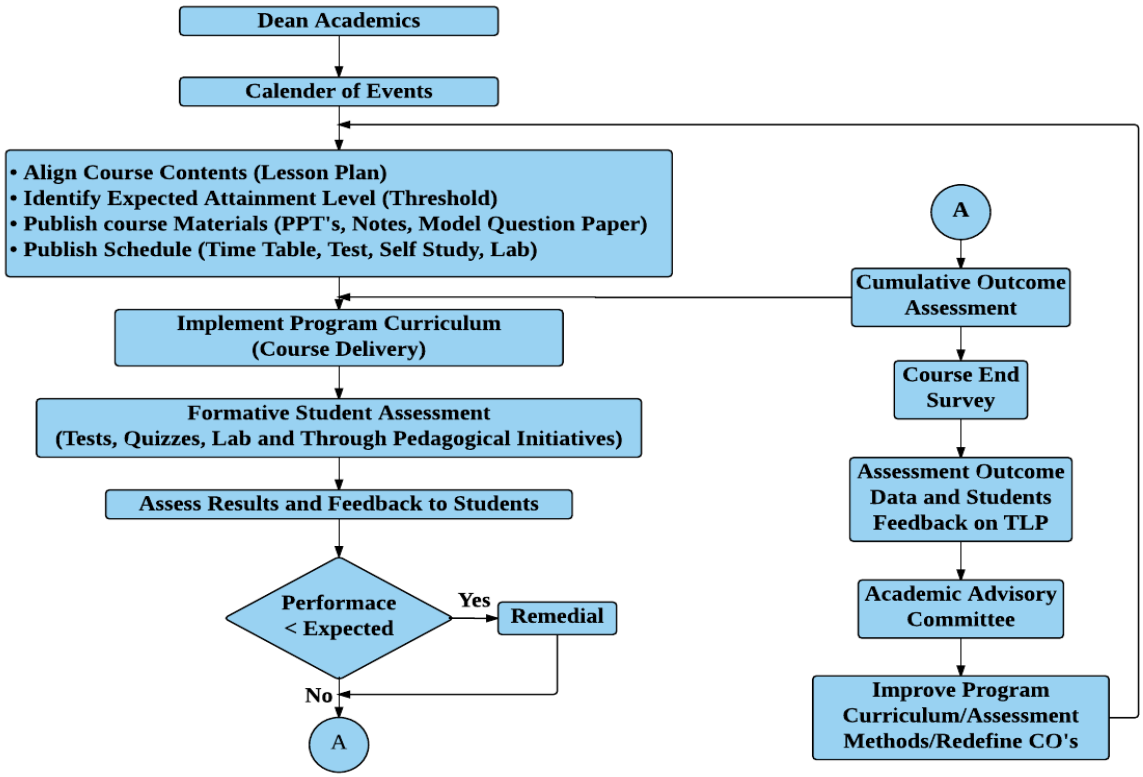
Rubrics for Evaluation:

1) Topic – Technical Relevance, Sustainability and Societal Concerns 15%
2) Review of literature 25%
3) Presentation Skills 35%
4) Report 25%

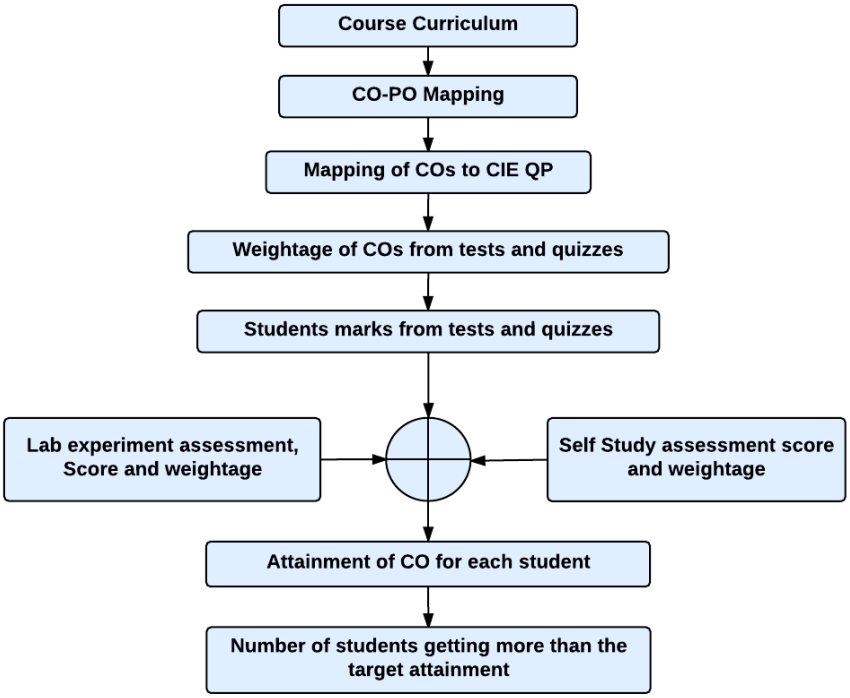
Curriculum Design Process



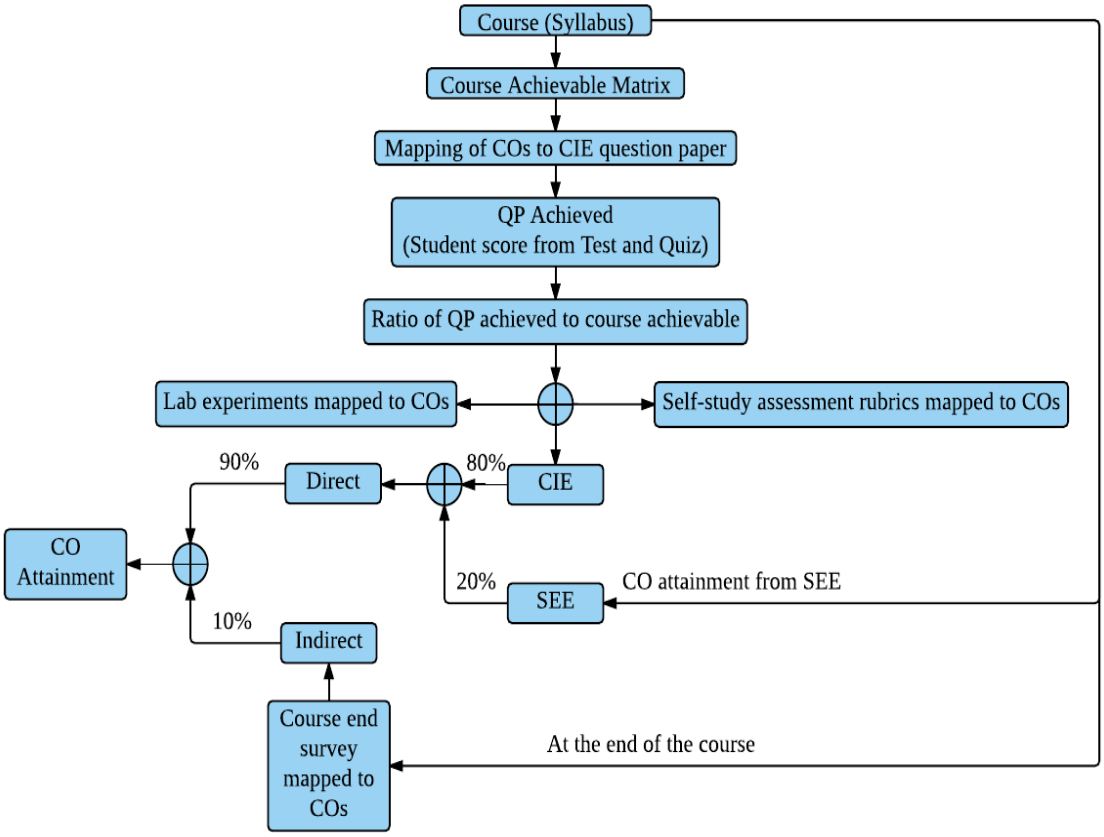
Academic Planning And Implementation



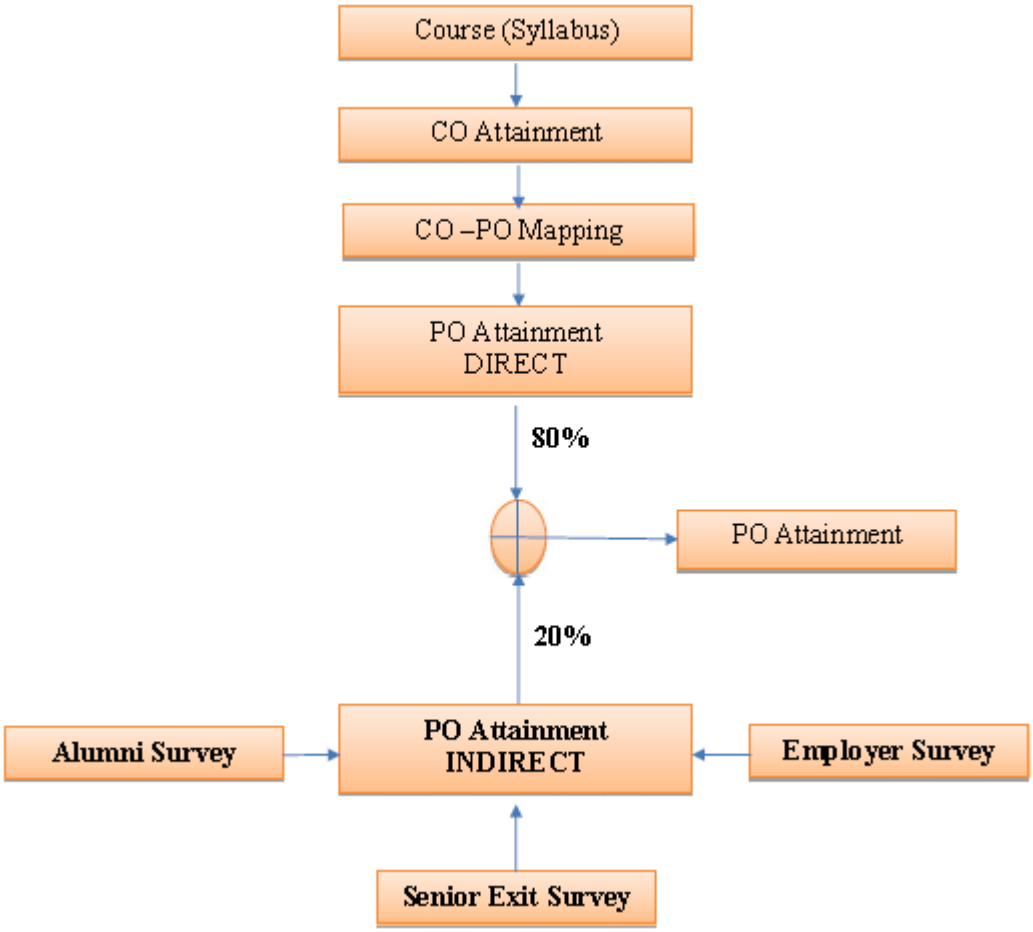
Process For Course Outcome Attainment



Final CO Attainment Process



Program Outcome Attainment Process



PROGRAM OUTCOMES (PO)

M. Tech. in Power Electronics graduates will be able to:

PO1: Able to independently carry out research /investigation and development work to solve practical problems in **Power Electronics**

PO2: Able to write and present a substantial technical report/document

PO3: Able to demonstrate a degree of mastery over **power electronics** at a level higher than the requirements in bachelor program of Electrical Engineering

PO4: Integrate **Power Electronics** with other domains to facilitate collaborative inter-disciplinary research

PO5: Acquire professional integrity and ethics, understand the responsibility for sustainable development of the society

PO6: Understand and demonstrate management skills, assess and evaluate the economic feasibility , work effectively as a leader and a team member.