


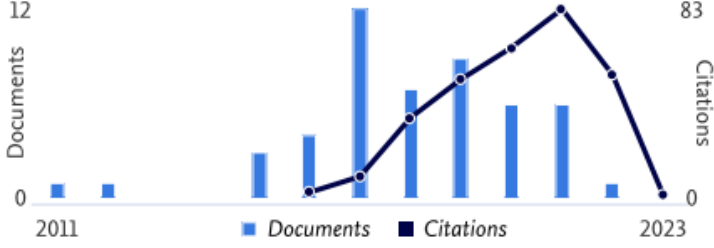





Dr. H V R Aradhya, Prof and Head, ECE, Paper Publication Details:

Papers published in Journals/Conferences: Total - - 147

S. No	Dr. HVR – Author Profile/Credentials can be viewed at	Publisher
1	<p>http://www.scopus.com/authid/detail.url?authorId=55616592800</p> <p> http://orcid.org/0000-0003-3076-9120</p> <p>ORCID: 0000-0003-3076-9120; publications: 49; citations: 267; H-index: 09</p> <p>Aradhya, H. V.Ravish</p> <p> Department of Electrical & Computer Engineering, Bengaluru, India</p> <p> https://orcid.org/0000-0003-3076-9120</p> <hr/> <p>Metrics overview Document & citation trends</p> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>50 Documents by author</p> <p>302 Citations by 224 documents</p> <p>10 h-index: View h-graph</p> </div> <div style="width: 50%;">  <p style="text-align: center;">as on 22/11/2022.</p> </div> </div>	Scopus
2	<p>https://publons.com/dashboard/records/publication/authored/</p> <p>Researcher ID: 0-6994-2016; publications: 77; citations: 56; H-index: 4</p> <div style="display: flex; align-items: center;">  <div> <p>Ravish Aradhya H. V</p> <p><i>"Aradhya H V Ravish"</i></p> <p>Web of Science ResearcherID </p> <p>0-6994-2016</p> </div> </div> <p>Faculty - Electronics and Communication Engineering, R V College of Engineering, Bangalore</p> <p>Metrics Open dashboard</p> <p>Web of Science Core Collection metrics</p> <div style="display: flex; justify-content: space-around; margin-top: 20px;"> <div style="text-align: center;"> <p>4</p> <p>H-Index</p> </div> <div style="text-align: center;"> <p>27</p> <p>Publications in Web of Science</p> </div> </div> <div style="display: flex; justify-content: space-around; margin-top: 20px;"> <div style="text-align: center;"> <p>76</p> <p>Sum of Times Cited</p> </div> <div style="text-align: center;"> <p>68</p> <p>Citing Articles</p> </div> </div> <p style="text-align: right;">as on 22/11/2022.</p>	WOS

3	<p>https://www.semanticscholar.org/author/H.-V.-Ravish-Aradhya/19255649 https://www.semanticscholar.org/author/H.-V.-Ravish-Aradhya/9377770?sort=year</p> <p>ORCID: 0000-0003-3076-9120; publications: 38; citations: 158; H-index: 7</p> <p>RAVISH ARADHYA H V RV College of Engineering, Bengaluru</p> <p>0000-0003-3076-9120 www.rvce.edu.in</p> <p>Publications 38 h-index 8 Citations 230 Highly Influential Citations 6</p> <p>as on 22/11/2022.</p>	Semantic Scholar												
4	<p>https://scholar.google.com/citations?hl=en&user=T0QNp0kAAAAJ https://scholar.google.com/citations?hl=en&user=C5X7B-AAAAAJ</p> <p>publications: 138; citations: 446; H-index: 11; i-10 index: 11</p> <p>11/21/22, 6:41 AM Ravish Aradhya H. V. - Google Scholar</p> <div style="display: flex; align-items: flex-start;">  <div style="flex-grow: 1;"> <p>Ravish Aradhya H. V.</p> <p>Professor and Associate Dean, Electronics and Communication Engineering, R. V. College of</p> <p>Low Power VLSI design and Embedded ...</p> </div> <table border="1" style="margin-left: 10px; border-collapse: collapse;"> <thead> <tr> <th></th> <th>All</th> <th>Since 2017</th> </tr> </thead> <tbody> <tr> <td>Citations</td> <td>505</td> <td>428</td> </tr> <tr> <td>h-index</td> <td>12</td> <td>12</td> </tr> <tr> <td>i10-index</td> <td>17</td> <td>13</td> </tr> </tbody> </table> </div> <p>as on 22/11/2022.</p>		All	Since 2017	Citations	505	428	h-index	12	12	i10-index	17	13	Google Scholar
	All	Since 2017												
Citations	505	428												
h-index	12	12												
i10-index	17	13												
Published by		Number												
1.	International Journals	45												
2.	International Conferences	75												
3.	National Conferences	24												
4.	National Journals	00												
5.	PhD Forum	03												
Total Number of Publishes		147												
IEEE, SPRINGER, ELSEVIER PAPERS														
1	SCI Indexed	27												
2	WOS Indexed	77												
3	Scopus Indexed	45												
4	IEEE Conferences	43												
5	SPRINGER Conferences	06												
6	ELSEVIER Conferences	02												
7	Others	60												
BEST PAPER AWARDS - - 04														
1	Journal – Paper No. 16	01												
2	Conference – Paper No. 10	01												
3	Conference – Paper No. 32 (IEEE Conference)	01												
4	PhD forum presentation @ IISc and IIT–B Conference -Paper No. 31 and Paper No. 55	03												
YEAR WISE PUBLICATIONS														

1.	Year 2022	01
2.	Year 2021	12
3.	Year 2020	12
4.	Year 2019	16
5.	Year 2018	12
6.	Year 2017	09
7.	Year 2016	16
8.	Year 2015	15
9.	Year 2014	04
10.	Year 2013	04
11.	Year 2012	15
12.	Year 2011	07
13.	Year 2010	04
14.	Year 2009	07
15.	Year 2008	01
16.	Year 2007	01
	Total Publications	147
	To be published	04

(i) International Journals: 45

1. Ravish Aradhya H. V, Ashish Kapania, “**Design Space Exploration of Power Efficient Cache Design Techniques,**” Advances in Networks and Communications, Book-1, ISBN: 978-3-642-17878-8_37, **SPRINGER Berlin Heidelberg**, Jan-2011, Vol. 132, pp. 362-371. DOI: 10.1007/978-3-642-17878-8_37. Part of the Communications in Computer and Information Science book series (CCIS, Volume 132)
(Download link: https://link.springer.com/chapter/10.1007/978-3-642-17878-8_37)
2. Ravish Aradhya H. V, B. V. Praveen Kumar, Dr. K. N Muralidhara, “**Design of Low Power Arithmetic Unit (AU) based on Reversible Logic,**” International Journal of VLSI and Signal Processing Applications (IJVSPA), Vol. 1, Issue 1, ISSN: 2231-3575, Apr-2011, pp. 30- 38.
(Download Link: <http://www.sciencedirect.com/science/article/pii/S1877705812009186>)
3. Ravish Aradhya H. V, G Mithun Kumar, Dr. K. N Muralidhara, “**Modelling of complex analog circuits with assertions and automatic processing of Waveforms,**” International Journal of Advanced Engineering Sciences and Technologies (IJAEST), Vol. No. 6, Issue No. 2, pp. 220 – 223, ISSN: 2230-7818, May-2011.
(Download Link: <https://www.researchgate.net/profile/Ravish-Aradhya-H-V/publication/260766686>)
4. Ravish Aradhya H. V, G Mithun Kumar, Dr. K. N Muralidhara, “**A Novel assertion based Methodology to verify mixed signal SOC designs in Digital and Mixed signal**

verification flow,” International Journal of Engineering Science and Technology (IJEST), ISSN: 0975–5462, Vol. No. 3, Issue No. 6, June 2011, pp. 4721-4727, June-2011.

5. H V Ravish Aradhya, B. V. Praveen Kumar, Dr. K. N Muralidhara, “**Design of Control unit for Low Power ALU Using Reversible Logic,**” International Journal of Scientific and Engineering Research, France, Volume 2, Issue 7, ISSN 2229-5518, Sep-2011, pp. 01-07.

(Download Link: <http://www.ijser.org/researchpaper%5CDesign-of-Control-unit-for-Low-Power-ALU-Using-Reversible-Logic.pdf>)

6. H V Ravish Aradhya, J. Lakshmesha, Dr. K. N Muralidhara, “**Design Optimization of Reversible Logic Universal Barrel Shifter for Low Power Applications,**” International Journal of Computer Applications, New York, USA, Volume 40, Issue 15, ISSN 0975-8887, Feb-2012, pp. 26-34. (Paper Reference ID: pxc3877379)

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7. H V Ravish Aradhya, G. Rekha, Dr. K. N Muralidhara, “**Simulation and Synthesis of Combinational Shifter using Reversible Gates,**” International Journal of Computer Applications, USA, Vol. 41, Issue 15, ISSN 0975-8887, Mar-2012, pp.26-35 (Paper Reference ID: pxc3879354).

(Download Link:

<https://pdfs.semanticscholar.org/d114/1b0ebcac839372255b37a5496a12be791887.pdf>)

8. H V Ravish Aradhya, R. Chinmaye, Dr. K. N Muralidhara, “**Design, Optimization and Synthesis of Efficient Reversible Logic Binary Decoder,**” International Journal of Computer Applications (IJCA), New York, USA, ISSN- 0975-8887, Vol. 46, Issue. 6, May-2012, pp.45-51 (Paper Reference ID: pxc3879354).

(Download Link: <http://research.ijcaonline.org/volume46/number6/pxc3879354.pdf>)

9. H V Ravish Aradhya, H. R. Madan, M. Girish Kumar, V. Ebenezer, “**Considerations of FinFET Based 6T SRAM Cells,**” International Journal of Science Research, Vol. 01, Issue 03, Dec-2012, pp. 134-136.

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<http://journal.tumkuruniversity.ac.in:8080/index.php/ijsr/article/view/68>)

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11. H V Ravish Aradhya, H. R. Madan, M. Akshay Bhounsley, V. Ebenezer, “**Comparative Study of SRAM & DRAM for various CMOS process technology,**” International Journal of Science Research, Vol. 01, Issue 03, Dec-2012, pp. 141-143.

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12. H V Ravish Aradhya, H. R. Madan, Md. Luqman, K. Suresh, “**Design and Performance Analysis of 8T SRAM for Different Scaled Technologies,**” International Journal of Science Research, Vol. 01, Issue 03, Dec-2012, pp. 151-153.

(Download Link: <http://journal.tumkuruniversity.ac.in:8080/index.php/ijsr/article/view/74>)

13. H V Ravish Aradhya, J. Lakshmesha, Dr. K. N Muralidhara, “**Reduced Complexity Hybrid Ripple Carry Look Ahead Adder,**” International Journal of Computer Applications (IJCA), New York, USA, ISSN- 0975-8887, Vol. 70, Issue. 28, May-2013, pp. 13-16. (Paper Reference ID: pxc388202).

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16. Dr. H V Ravish Aradhya, et al, “**Design and Optimization of Reversible carry look ahead Adder Circuit,**” International Journal of Electronics and Communication Engineering (IJECE), ISSN: 2278-991X, Vol. 03, Issue.3, May-2014, pp. 65-72. Received “**Best Paper**” Award (Dated: 09th Dec 2014).

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17. Dr. H V Ravish Aradhya and Roopa H K, “**Comparative study of Bluetooth Testing Automation Tools on Android,**” International Journal of Scientific Engineering and Technology Research, ISSN: 2319-8885, Vol. 3, Issue.15, June-2014, pp. 3196-3198.

(Download Link: <http://ijsetr.com/uploads/425316IJSETR1639-545.pdf>)

18. Dr. H V Ravish Aradhya, et al, “**Design and Verification of Analog Phase Locked Loop Circuit,**” International Journal of Combined Research and Development (IJCRD), ISSN: 2321-225X, Vol. 02, Issue.6, June-2014, pp. 01-05.

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(Download Link: <https://www.ijsr.net/conf/NCKITE2015/162.pdf>)
21. Dr. H V Ravish Aradhya, B. V. Vishwas, “**A Novel SRAM Cell Design for Low Power Applications,**” International Journal of Engineering Research and Technology (IJERT), ISSN: 2278-0181, Vol. 04, Issue. 06, June-2015, pp. 1146-1149.
(Download Link: <http://www.ijert.org/view-pdf/13570/a-novel-sram-cell-design-for-low-power-applications>)
22. Dr. H V Ravish Aradhya, et al, “**GNRFET based 8-Bit ALU,**” International Journal of Electronics and Communication Engineering (IJECE), ISSN: 2278-991X, Vol. 05, Issue. 01, Jan-2016, pp. 65-72. Impact Factor (JCC) - 2015:3.6986; Index Copernicus Value (ICV) - 2015:3.0; NAAS Rating: 3.06.
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24. Ravish Aradhya H. V, Sachin M. Revannanavar, “**Analysis, Physical Design and Power Optimization of Block Signal Estimator for High Speed Serial Interface,**” International Journal of Science and Research (IJSR), ISSN (Online): 2319-7064, Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391, Aug 2017. Vol. 06, Issue. 08, pp. 916-920. (Download Link: <https://www.ijsr.net/archive/v6i8/ART20176029.pdf>)
25. Ravish Aradhya H. V, Manjunatha Rao V, “**Clock Power Optimization in VLSI design at Advanced Technology Nodes,**” International Journal of Computer Applications (IJCA), ISSN: 0975 – 8887, Vol. 169, Issue. 09, July 2017, pp. 29-34.
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26. Ravish Aradhya H. V, Apoorva Raghunandan, “**Performance Analysis of Advanced Adders Under Changing Technologies,**” International Journal of Innovations in

- Engineering and Technology (IJET), Vol. 12, Issue 2, January 2019, ISSN: 2319-1058, pp. 87-94. <http://dx.doi.org/10.21172/ijet.122.15>
(Download Link: <https://ijet.com/wp-content/uploads/2019/05/151.pdf>)
27. Ravish Aradhya H. V, Shreyas H S, Arunkumar P Chavan, “**Design and Analysis of Low Power VCO Enabled Quantizer for CT Sigma Delta ADC,**” Indian Journal of Public Health Research & Development (IJPHRD), Vol. 10, Issue 5, Jun 2019, ISSN: 0976-0245, E-ISSN:0976-5506, pp. 921-927. DOI: [10.5958/0976-5506.2019.01197.5](https://doi.org/10.5958/0976-5506.2019.01197.5)
(Download link: <http://www.indianjournals.com/ijor.aspx?target=ijor:ijphrd&volume=10&issue=5&article=174>)
28. Ravish Aradhya H. V, Nehal B, “**Design of Field Area Network on Advanced Metering Infrastructure,**” International Journal of Emerging Technologies and Innovative Research (JETIR), Vol. 12, Issue 2, January 2019, ISSN: 2349-5162, pp. 87-94.
29. Ravish Aradhya H. V, Bharath B. Shetty, “**User Service REST API using Spring Boot,**” International Journal of Computer Sciences and Engineering (IJCSE), Vol. 12, Issue 2, May 2019, ISSN: 2347-2697, pp. 87-94.
30. Ravish Aradhya H. V, Gagan A, “**Logic Structure Reduction Scheme for FINFET based TSPC Flip-Flop,**” International Journal of Engineering Research and Technology (IJERT), Vol. 8, Issue 6, Jun 2019, ISSN: 2278-0181, pp. 431-435. (Download link: <https://www.ijert.org/research/logic-structure-reduction-scheme-for-finfet-based-tspc-flip-flop-IJERTV8IS060349.pdf>)
31. Ravish Aradhya H. V, Mohana, “**Object Detection and Classification Algorithms using Deep Learning for Video Surveillance Applications,**” International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 8, Issue 8, Jun 2019, ISSN: 2278-3075, pp. 386-395. (Scopus Indexed) [Download link: <https://www.ijitee.org/wp-content/uploads/papers/v8i8/H6362068819.pdf>]
32. Mohana, Ravish Aradhya H V, “**Object Detection and Tracking using Deep Learning and Artificial Intelligence for Video Surveillance Applications,**” International Journal of Advanced Computer Science and Applications(IJACSA); West Yorkshire Vol. 10, Iss. 12, Jun 2019, pp. 517-530, e-ISSN: 2156-5570, p-ISSN: 2158-107X, Dec-2019. DOI:10.14569/IJACSA.2019.0101269 (Scopus Indexed).
[Download link: https://thesai.org/Downloads/Volume10No12/Paper_69-Object_Detection_and_Tracking_using_Deep_Learning.pdf]
33. Pragna G, Ravish Aradhya H V, “**Review on Skilled Optimization of Voltage Controlled Oscillator,**” International Journal of Research and Analytical Reviews (IJRAR), Vol. 7, Issue. 2, pp. 330-334, e-ISSN: 2348-1269, p-ISSN: 2349-5138, Jun 2020 (UGC Approved-Journal No: 43602(19)). DOI: <http://www.ijrar.org/IJRAR19L1566.pdf>
[Download link: https://ijrar.org/viewfull.php?&p_id=IJRAR19L1566]
34. Abhishek R. Deshmukh, Ravish Aradhya H V, “**Experimental analysis of performance metrics for configuration of AutoScaling Groups,**” International Research Journal of

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[Download link: <http://sersc.org/journals/index.php/IJAST/article/view/24645/13005>]
36. Manjunath K M, Muralidhara K M, Ravish Aradhya H V, “**Incrementer and Decrementer of an N-Bit Input, by a Value 'M' Circuit Design and Analysis for Various Parameters,**” Journal of Critical Reviews (JCR), Vol. 7, Issue 05, June 2020, ISSN: 2394-5125, pp. 1781-1794. (Scopus indexed). doi: [10.31838/jcr.07.05.302](https://doi.org/10.31838/jcr.07.05.302)
[Download link: <https://drive.google.com/file/d/1Rfa8cMoQjMJOJVeXdrPHJcGaVbSdeCAB/view> or
<http://www.jcreview.com/fulltext/197-1595575457.pdf?1596341407> or
<http://www.jcreview.com/fulltext/197-1595575457.pdf?1596342177>]
37. Kiran G Shetty, H V Ravish Aradhya, “**Comparison of Dynamic Voltage Scaling(DVS) of Core Voltage Using the Onboard Voltage Regulator and External Voltage Regulator via I2C Protocol in Automotive Microcontroller,**” Journal of University of Shanghai for Science and Technology, ISSN: 1007-6735, Volume: 23, Issue: 6, (Scopus Indexed), pp: 794-804, <https://jusst.org/comparison-of-dynamic-voltage-scalingdvs-of-core-voltage-using-the-on-board-voltage-regulator-and-external-voltage-regulator-via-i2c-protocol-in-automotive-micro-controller/>, Jun 2021. (WOS and Scopus Indexed-IEEE)
(Download Link: <https://jusst.org/wp-content/uploads/2021/06/Comparison-of-Dynamic-Voltage-ScalingDVS-of-Core-Voltage-Using-the-On-board-Voltage-Regulator-and-External-Voltage-Regulator-via-I2C-Protocol-in-Automotive-Microcontroller.pdf>)
38. Kiran G Shetty, H V Ravish Aradhya, “**Instruction Based Power Estimation Method in AURIX Microcontroller,**” Journal of University of Shanghai for Science and Technology, ISSN: 1007-6735, Volume: 23, Issue: 6, (Scopus Indexed), pp: 784-793, <https://jusst.org/instruction-based-power-estimation-method-in-aurix-micro-controller/>, Jun 2021.
(Download Link: <https://jusst.org/wp-content/uploads/2021/06/Instruction-Based-Power-Estimation-Method-in-AURIX-Microcontroller.pdf>) (WOS and Scopus Indexed-IEEE)
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(Download Link: <https://jusst.org/wp-content/uploads/2021/06/A-Python-based-Design-Verification-Methodology.pdf>)
40. Ravish Aradhya H V, Deekshith Nayak, “**Orchestrating a Stateful application using Operator,**” Journal of University of Shanghai for Science and Technology, ISSN: 1007-

6735, Volume: 23, Issue: 6, (Scopus Indexed), pp: 514-520, <https://jusst.org/orchestrating-a-stateful-application-using-operator/>, Jun 2021.

(Download Link: <https://jusst.org/wp-content/uploads/2021/06/Orchestrating-a-stateful-application-using-Operator.pdf>) (WOS and Scopus Indexed-IEEE)

41. Ravish Aradhya H V, Karthik S Kulkarni, “**MAC Unit Optimization for Area, Power and Timing Constraints,**” International Journal for Research in Applied Science & Engineering Technology (IJRASET), ISSN: 2321-9653, Volume: 9, Issue: 5, pp: 2030-2035, <https://doi.org/10.22214/ijraset.2021.34753>, May 2021.
(Download Link: <https://www.ijraset.com/fileserve.php?FID=34753>)
42. Ravish Aradhya H V, Kishan Maladkar, “**Design and Implementation of a 32-bit Floating Point Unit,**” International Journal for Research in Applied Science & Engineering Technology (IJRASET), ISSN: 2321-9653, Volume: 9, Issue: 6, pp: 731-736, <https://doi.org/10.22214/ijraset.2021.35052>, Jun 2021.
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43. Ravish Aradhya H V, Neethu S, “**Detection of DDoS Attacks in SDN,**” ECS Transactions (IOPscience), ISSN: 1938-5862, 1938-6737, Vol. 107, No. 1, pp: 18305-18313 <https://doi.org/10.1149/10701.18305ecst>, Apr 2022.
44. Ravish Aradhya H V, Arunkumar P Chavan, “**Ultra Low Power Hybrid Voltage Controlled oscillator for Data Acquisition System**” International Journal of Emerging Trends & Technology in Computer Science (IJETTCS), ISSN: 2278-6856, pp. **1938-6737**, Vol: 11, Issue: 4, July-2022 DOI: <https://doi.org/10.2749/IJETTCS.1008.2284>. (**Scopus indexed**)
(Download Link: <https://www.ijraset.com/fileserve.php?FID=35052>)??
45. Ravish Aradhya H V, Arunkumar P Chavan, “**Design of 5.1GHz Ultra-Low Power and Wide Tuning Range Hybrid Oscillator**” International Journal of Electrical and Computer Engineering (IJECE) -2022 (Q2 Journal in press). (**Scopus indexed**)
46. Ravish Aradhya H V, Sushanth G, “**Hardware in Loop Network Simulators - An Insight Overview,**” International Journal of Advanced Computer Science and Applications (IJACSA) August 2022, Edition (Volume 13 No 8). (Q2 Journal in press). (**Scopus indexed**)
47. publication

(ii) International Conferences: 75

1. H. V. Ravish Aradhya, Prasad P. Kamat, Dr. K. N. Muralidhara, “**Multi Core ALU – a low power approach,**” in the proceedings of International Conference on Computer, Communication and Instrumentation (3CI-07); RVCE, Bangalore-59, India, 23-25 Nov, 2007.

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20. Ravish Aradhya H. V and Karnati Gopi Manohar, **“Realization of universal gates of Multiple Valued Logic (MVL) using CMOS technology,”** National conference on "Engineering, Technology and Management, 22-23 April 2016, R. V. College of Engineering, Bengaluru 560059.

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24. Ravish Aradhya H V, Arunkumar P Chavan, “**Design and analysis of component for VCO enabled quantizer using Different stages of ring oscillator in CT sigma delta ADC,**” National conference on knowledge dissertation of PG projects and research’s work May 7th and 8th 2018, RVCE, Bengaluru.
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PhD Forum – Presentations:

1. Mohana, Ravish Aradhya H. V, “**Elegant and Efficient Algorithms for Real Time Implementation of Object Detection, Classification, Tracking and Counting using FPGA Zynq XC7Z020 for Automated Video Surveillance Applications,**” 10th **IEEE** Advanced Networks and Telecommunications Systems (ANTS-2016), 6-9 November 2016, J. N. Tata Auditorium, *Indian Institute of Science* (IISc), Bangalore, India.
2. Mohana, Ravish Aradhya H. V, “**Design and Implementation of Object Detection, Classification, Tracking, Counting and Classification Algorithms using Artificial Intelligence for Automated Video Surveillance Applications,**” 24th International Conference on Advanced Computing Communications (ADCOM-2018), 21st – 23rd September 2018, at the IIIT-Bangalore, India.
3. Mohana, Ravish Aradhya H. V, “**Design of Efficient Algorithms for Video Surveillance Applications using Artificial Intelligence,**” 25th **IEEE** Advanced Computing and Communications Conference (ADCOM 2019), 5-7 September 2019, at International Institute of Information Technology (IIIT-B), Bangalore, India.

Awards and Appreciations:

1. Recipient of “**Best Research Paper Award**” from *International Academy of Science, Engineering and Technology* in International Journal of Electronics and Communication Engineering (IJECE), ISSN: 2278-991X, Dec-2014. IF-3.329, for the paper titled “**Design and Optimization of Reversible carry look ahead Adder Circuit.**” (PhD research outcome).
2. Recipient of “**Best Research Paper Award**” from *IEEE-International Conference on Engineering and Technology* (ICETECH-2015), Mar-2015. IF-3.329, for the paper titled “**Design of square spiral Nano-antenna in infra-red region for Solar Energy Harvesting,**” conducted by Rathinam Institute of Technology, Coimbatore, Tamilnadu, India. IEEE Explorer: 978-1-4799-7678-2/15/\$31.00, ©2015 IEEE, (Conference Record Number: #35961), 20th March 2015, pp:1026-1031.
3. Recipient of “**Best Research Paper Award**” from *IEEE-International Conference on Innovative Mechanisms for Industry Applications* (ICIMIA-2017), 21-23 Feb 2017, for the paper titled “**Implementation of Highly Efficient Sorting Algorithm for Median Filtering using FPGA Spartan-6,**” conducted by Dayananda Sagar College of Engineering, Bengaluru, India. 978-1-5090-5960-7/17/\$-31.00, ©2017 IEEE, ISBN: 978-1-5090-5959-1, (Conference Record Number: #35961), 21-23 Feb 2017, pp. 265-269.

Best Teacher Awards:

1. Recipient of “Best Teacher Award” from Carrier Launcher (India), Bangalore, May 2006
2. Recipient of “Best Teacher Award” from ISTE-RVCE Chapter, Sep-2019