RV College of Engineering®

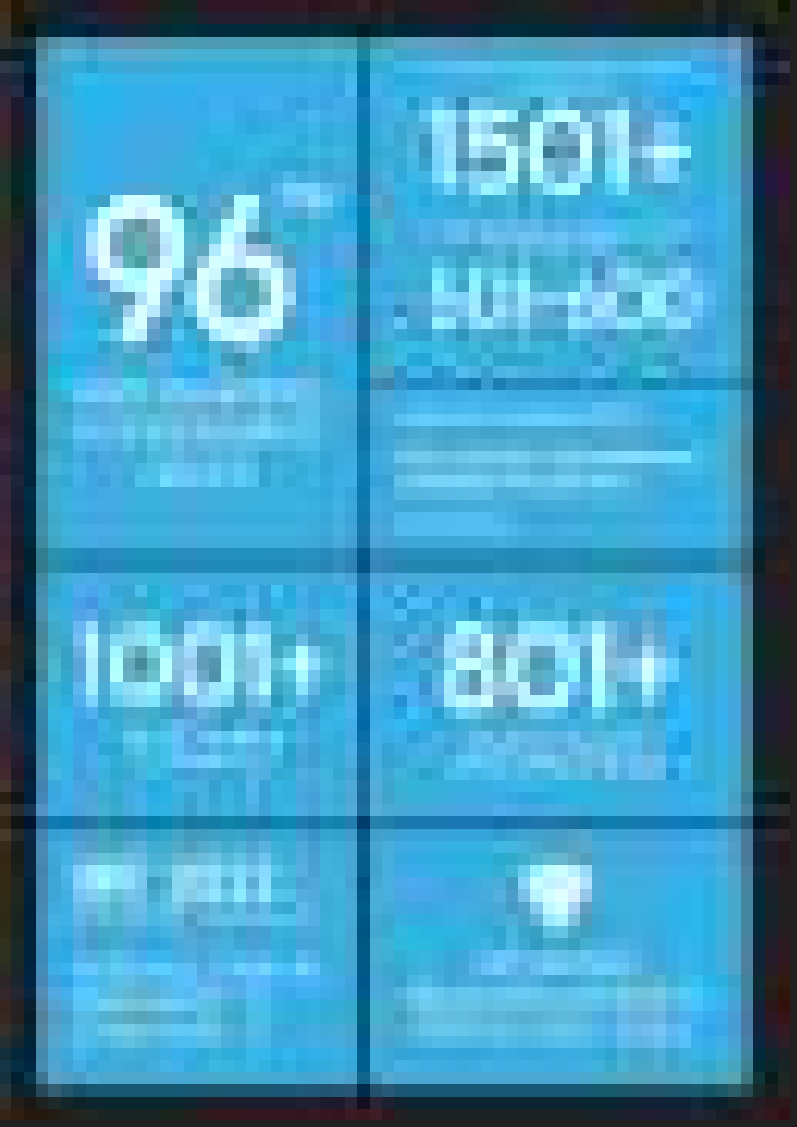
Master of Technology (M.Tech)
in

VLSI DESIGN & EMBEDDED SYSTEM (MVE)

Scheme And Syllabus Of I & IV Semester
(2022 Scheme)

B.E. Programs : AI, AS, BT, CH, CS, CV, CD, CY, EC, EE, EI, ET, IM, IS, ME.
M. Tech (13) MCA, M.Sc. (Engg.)
Ph.D. Programs : All Departments are recognized as
Research Centres by VTU Except AI & AS

2024



CURRICULUM STRUCTURE

61 CREDITS
PROFESSIONAL CORES (PC)

23 CREDITS
BASIC SCIENCE

22 CREDITS
ENGINEERING SCIENCE

18 CREDITS
PROJECT WORK / INTERNSHIP

12 CREDITS*
OTHER ELECTIVES & AEC

12 CREDITS
PROFESSIONAL ELECTIVES

12 CREDITS
HUMANITIES & SOCIAL SCIENCE

160
CREDITS TOTAL

*ABILITY ENHANCEMENT COURSES (AEC), UNIVERSAL HUMAN VALUES (UHV), INDIAN KNOWLEDGE SYSTEM (IKS), YOGA.

17
Centers of Excellence

11
Centers of Competence

1381
Publications On Web Of Science

397
Publications On Web Of Science

1699
Citations

78
Patents Filed

38
Patents Granted

58
Published Patents

11
Skill Based Laboratories Across Four Semesters

MOUS: 90+WITH INSDUSTRIES / ACADEMIC INSTITUTIONS IN INDIA & ABROAD

EXECUTED MORE THAN RS.40 CRORES WORTH SPONSORED RESEARCH PROJECTS & CONSULTANCY WORKS SINCE 3 YEARS

RV College of Engineering®
Mysore Road, RV Vidyaniketan Post,
Bengaluru - 560059, Karnataka, India

principa

Master of Technology in

VLSI DESIGN & EMBEDDED SYSTEM

SCHEME & SYLLABUS of I TO IV SEMESTER 2022 SCHEME

Glossary of Abbreviations

1.	AS	Aerospace Engineering
2.	BS	Basic Sciences
3.	BT	Biotechnology
4.	CH	Chemical Engineering
5.	CHY	Chemistry
6.	CIE	Continuous Internal Evaluation
7.	CS	Computer Science & Engineering
8.	CV	Civil Engineering
9.	EC	Electronics & Communication Engineering
10.	EE	Electrical & Electronics Engineering
11.	EI	Electronics & Instrumentation Engineering
12.	ET	Electronics & Telecommunication Engineering
13.	GE	Global Elective
14.	HSS	Humanities and Social Sciences
15.	IM	Industrial Engineering & Management
16.	IS	Information Science & Engineering
17.	L	Laboratory
18.	MA	Mathematics
19.	MBT	M. Tech in Biotechnology
20.	MCE	M. Tech. in Computer Science & Engineering
21.	MCN	M. Tech. in Computer Network Engineering
22.	MCS	M. Tech. in Communication Systems
23.	MDC	M. Tech. in Digital Communication
24.	ME	Mechanical Engineering
25.	MHT	M. Tech. in Highway Technology
26.	MIT	M. Tech. in Information Technology
27.	MMD	M. Tech. in Machine Design
28.	MPD	M. Tech in Product Design & Manufacturing
29.	MPE	M. Tech. in Power Electronics
30.	MSE	M. Tech. in Software Engineering
31.	MST	M. Tech. in Structural Engineering
32.	MVE	M. Tech. in VLSI Design & Embedded Systems
33.	N	Internship
34.	P	Projects (Minor / Major)
35.	PHY	Physics
36.	SDA	Skill Development Activity
37.	SEE	Semester End Examination
38.	T	Theory
39.	TL	Theory Integrated with Laboratory
40.	VTU	Visvesvaraya Technological University

POSTGRADUATE PROGRAMS

Sl. No	Core Department	Program	Code
1.	BT	M. Tech in Biotechnology	MBT
2.	CS	M. Tech in Computer Science & Engineering	MCE
3.	CS	M. Tech in Computer Network Engineering	MCN
4.	CV	M. Tech in Structural Engineering	MST
5.	CV	M. Tech in Highway Technology	MHT
6.	EC	M. Tech in VLSI Design & Embedded Systems	MVE
7.	EC	M. Tech in Communication Systems	MCS
8.	EE	M. Tech in Power Electronics	MPE
9.	ET	M. Tech in Digital Communication	MDC
10.	IS	M. Tech in Software Engineering	MSE
11.	IS	M. Tech in Information Technology	MIT
12.	ME	M. Tech in Product Design & Manufacturing	MPD
13.	ME	M. Tech in Machine Design	MMD

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

VISION

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering

MISSION

1. To impart quality technical education to produce industry-ready engineers with a research outlook.

2. To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.

3. To create centres of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.

4. To develop entrepreneurial skills among the graduates to create new employment opportunities

PROGRAMME OUTCOMES (PO)

M. Tech in **VLSI Design and Embedded Systems** graduates will be able to:

PO1: Independently carry out research/investigation and development work to solve the practical problems related to VLSI Design and Embedded Systems.

PO2: Write and present a substantial technical report/document in the field of VLSI Design and Embedded Systems

PO3: Demonstrate a degree of mastery over the area of VLSI Design and Embedded Systems. The mastery should be level higher than the requirements of bachelor's in Electronics & Communication Engineering program.

PO4: Abstract the requirements of modern microelectronics and smart systems to offer innovative solutions with available IPs and interfaces.

PO5: Design and develop VLSI and Embedded modules with good economics to meet Quality of Service.

PO6: Acquire professional and intellectual integrity, research ethics and execute socio-concern projects related to modern VLSI and Embedded Systems.

INDEX

M.Tech in VLSI Design & Embedded Systems: MVE

I SEMESTER M.Tech

Sl. No.	Course Code	Course Title	Credit Allocation L	T/ SDA	P	Total	BoS	Category	CIE Duration (H)	Max Marks CIE	SEE Duration (H)	Max Marks SEE
1	MVE201T	Digital System Design with FPGA	3	1	0	**4**	EC	Theory	1.5	100	3	100
2	MVE202I	Digital IC Design	3	0	1	**4**	EC	Theory+Lab	1.5	100	3	100
3	MVE203T	Advanced Embedded System Design	3	1	0	**4**	EC	Theory	1.5	100	3	100
4	MVE204L	ARM CPUs Programming Lab	1	0	1	**2**	EC	Lab	1.5	50	3	50
5	MVE301AX	Elective A (Professional Elective)	3	0	0	**3**	EC	Theory	1.5	100	3	100
6	MVE302BX	Elective B (Professional Elective)	3	0	0	**3**	EC	Theory	1.5	100	3	100

Note: For the course code 22HSS42, Students need to select one ONLINE MOOC course as recommended by HSS BoS. This course can be selected anytime between I to III semester and it will be evaluated during IV semester.

Code	Elective A (Professional Elective)	Code	Elective B (Professional Elective)
MVE301A1	Low Power VLSI Design	MVE302B1	Static Timing Analysis
MVE301A2	ASIC Design	MVE302B2	System On Chip Design
MVE301A3	VLSI Digital Signal Processing	MVE302B3	IC Technology
MVE301A4	Real Time Embedded Systems	MVE302B4	IOT System Design & Architecture
MVE301A5	Semiconductor Device Modelling	MVE302B5	VLSI for Data Conversion Circuits

II SEMESTER M.Tech

Sl. No.	Course Code	Course Title	Credit Allocation L	T/ SDA	P	Total	BoS	Category	CIE Duration (H)	Max Marks CIE	SEE Duration (H)	Max Marks SEE
1	MIM431T	Research Methodology	3	0	0	**3**	IM	Theory	1.5	100	3	100
2	MVE331I	Analog IC Design	3	0	1	**4**	EC	Theory+Lab	1.5	100	3	100
3	MVE332T	System Verilog for Design & Verification	3	0	0	**3**	EC	Theory	1.5	100	3	100
4	MCS333CX	Elective C (Professional Elective)	3	0	0	**3**	EC	Theory	1.5	100	3	100
5	**22XXX2DXXT**	**Elective G (Global Elective)**	3	0	0	**3**	Res. BoS	Theory	1.5	100	3	100
6	MVE431L	Analog Layout Design Lab	1	0	1	**2**	EC	Lab	1.5	50	3	50
7	MHS131T	Professional Skills Development-I	2	0	0	**2**	HSS	Theory*	1.5	50	2	50

** External Agency will be conducting the classes and both CIE and SEE will be evaluated by the Agency.*

Code	Elective C (Professional Elective)
MCS333C1	Development of Modern SoCs for Wireless, Wireline and IOT applications
MVE333C2	.VLSI Memory Chip Design
MVE333C3	Robotics and Industrial Automation
MVE333C4	Automotive Electronics
MVE333C5	Physical Design

Elective G (Global Elective)			
MBT331G	Bioinspired Engineering	MET331G	Tracking and Navigation Systems
MBT332G	Health Informatics	MIM331G	Project Management
MCS331G	Business Analytics	MIS331G	Database and Information Systems
MCV331G	Industrial and Occupational Health and Safety	MIS332G	Management Information Systems
MCV332G	Intelligent Transportation Systems	MMA331G	Statistical and Optimization Methods
MEC331G	Electronic System Design	MME331G	Industry 4.0
MEC332G	Evolution of Wireless Technologies		

III SEMESTER M.Tech

Sl. No.	Course Code	Course Title	Credit Allocation				BoS	Category	CIE Duration (H)	Max Marks CIE	SEE Duration (H)	Max Marks SEE
			L	T/ SDA	P	Total						
1	MVE361T	Algorithms for VLSI Design Automation	3	1	0	**4**	EC	Theory	1.5	100	3	100
2	MVE337DX	Elective D (Professional Elective)	3	1	0	**4**	EC	Theory	1.5	100	3	100
3	MVE461N	Internship	0	0	6	**6**	EC	Internship	1.5	50	3	50
4	MVE461P	Minor Project	0	0	6	**6**	EC	Project	1.5	50	3	50

Code	Elective D (Professional Elective)
MVE337D1	VLSI Testing
MVE337D2	High Speed Digital Design
MVE337D3	RFIC Design
MVE337D4	Signal Processing & ML on Microcontrollers
MVE337D5	MEMS and Smart Systems

IV SEMESTER M.Tech

Sl. No.	Course Code	Course Title	Credit Allocation				BoS	Category	CIE Duration (H)	Max Marks CIE	SEE Duration (H)	Max Marks SEE
			L	T/ SDA	P	Total						
1	MVE491P	Major Project	0	0	18	**18**	EC	Project	1.5	100	3	100
2	MHS191	Professional Skills Development-II	2	0	0	**2**	HSS	NPTEL	--	50	ONLINE	50
Student need to submit the certificate for the evaluation of Course code MHS191												

SEMESTER: I						
Course Code	:	MVE201T	**Digital System Design with FPGA**	CIE Marks	:	100
Credits L-T-P	:	3-1- 0		SEE Marks	:	100
Hours	:	42L + 28T	*(Professional Core - 1)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Soumya K B			

UNIT - I **9 Hrs**

Introduction to Verilog and Design Methodology: Verilog IEEE standards, Verilog Data Types: Net, Register and Constant. Verilog Operators, Number representation and Verilog ports,Simulation and Synthesis, Test-benches. Verilog Primitives. Logic Simulation, Design Verification, and Test Methodology: Four-Value Logic and Signal Resolution in Verilog, Test Methodology Signal Generators for Test benches, Sized Numbers.

Introduction to Design Methodology: Digital Systems and Embedded Systems, Real-world circuits. Design Methodology: Design Flow-Architecture, Functional design and verification, Synthesis, Physical design. Design

Optimization-Area, Timing and Power, System representation.

UNIT - II **9 Hrs**

Number Basics and Verilog Modelling Styles: Number Basics: Unsigned and Signed Integers, Fixed-point and Floating-point Numbers. Boolean Functions and Boolean Algebra, Verilog models for Boolean switching function, Binary Coding.

Behavioural Modelling: Latches and Level-Sensitive Circuits in Verilog, Cyclic Behavioural Models of Flip-Flops and Latches, Behavioural Models of Multiplexers, Encoders, Decoders and Arithmetic circuits. Dataflow Modelling: Boolean Equation-Based Models of Combinational Logic, Propagation Delay and Continuous Assignments. Linear-Feedback Shift Register. Tasks & Functions.

Structural Modelling: Design of Combinational Logic, Verilog Structural Models, Top-Down Design and Nested

Modules. (Hands on using Xilinx Vivado tool)

UNIT - III **8 Hrs**

Synthesis of Digital Sub-systems: Synthesis of Combinational Sub-systems: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Three-state Devices and Bus Interfaces. Synthesis of Sequential Sub-systems: Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines, Registered Logic, State Encoding, Synthesis of Implicit State Machines,

Registers and Counters. (Hand on using Xilinx Vivado)

UNIT - IV **8 Hrs**

System Implementation and Fabrics:CPLD vs FPGA Architecture - Programming Technologies-Chip I/O-Programmable Logic Blocks- Fabric and Architecture of FPGA. Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture – ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture, Hardcore and Softcore FPGA. (Examples such as counter, sequence detector, sequence generated etc are implemented on Airtex-7 FPGA

board)

UNIT - V **8 Hrs**

Processor Design and System Development: Design of Processor Architectures: Functional Units for Addition, Subtraction and Multiplication (overview). Design: Hierarchical Decomposition STG-Based Controller Design, Efficient STG-Based Sequential Binary Multiplier. Interfacing Concepts: Embedded Computer Organization, Instruction and Data, Memory Interfacing. I/O Interfacing: I/O devices, I/O controllers, Parallel Buses, Serial

Transmission.

Course Outcomes:

After going through this course the student will be able to:

CO1	:	Define IEEE-1364 standard and identify different styles of modelling to build digital systems.
CO2	:	Analyze digital systems and build small scale applications using Interfacing concepts.
CO3	:	Design and verify the behavior of digital circuits using digital flow.
CO4	:	Demonstrate the skill on cost-effective system designs through proper selection of implementation.

Reference Books

1. Advanced Digital Design With the Verilog HDL, Michael D. Ciletti, 2nd Edition, 2015, PHI, ISBN: 978–0–07–338054–4.

2. Digital Design: An Embedded Systems Approach Using VERILOG, Peter J. 1st Edition, 2010, Ashenden,
Elsevier, ISBN: 978-0-12-369527-7

3. Digital Systems Design Using Verilog, 1st Edition, 2015, Charles Roth, Lizy K. John, ByeongKil Lee,Cengage
Learning, ISBN-10: 1285051076

4. Fundamentals ofDigital Logic with Verilog Design, Stephen Brown and ZvonkoVranesic, 6th Edition, 2014,
McGraw Hill publication, ISBN: 978–0–07–338054–4

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full
question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE202I	**Digital IC Design**	CIE Marks	:	100
Credits L-T-P	:	3-0-1		SEE Marks	:	100
Hours	:	42 L + 28P	*Theory & Practice - (Professional Core - 2)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Kariyappa B S			

UNIT - I	**9 Hrs**
CMOS inverter: MOSFET- static & dynamic behavior, Static CMOS Inverter: static and dynamic Behavior, Components of Energy and Power CMOS Combinational Logic Circuit Design: Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic. Dynamic CMOS Design: Dynamic Logic Design Considerations. Speed and Power Dissipation of Dynamic logic, Signal integrity issues, Cascading Dynamic gates.	
UNIT - II	**9 Hrs**
CMOS Sequential Logic Circuit Design: Static Latches and Registers. Dynamic Latches and Registers. Pulse Based Registers. Sense Amplifier based registers. Pipelining concepts. Memory & Array structures design: Memory core – ROM, SRAM, DRAM, Sense amplifiers, CAM	
UNIT - III	**8 Hrs**
Arithmetic building blocks design: Data paths in digital processor architectures – Adder, binary adder, static adder, mirror adder, TG based adder, carry bypass adder, linear and square root carry select adder, carry lookahead adder, Multiplier- array, carry save multiplier, Barrel shifter and Logarithmic shifter.	
UNIT - IV	**8 Hrs**
Interconnects: Interconnect Impact, Resistive, Capacitive and Inductive Parasitics, Crosstalk Control, Timing Issues: Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and Impact on Performance.	
UNIT - V	**8 Hrs**
Clock Distribution and Self-Timed Circuit Design: Clock Distribution techniques, Latch based clocking. Self-Timed Circuit Design: Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling.Synchronizers and Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop.	
LABORATORY	**28 Hrs**
• MOS device Characterization • CMOS Static Inverter Characteristics • CMOS Inverter Dynamic Characteristics • CMOS 2 Input NAND Gate, CMOS 2 Input NOR Gate, Compound/Complex Gates & Pre-Layout Simulation • CMOS Inverter, NAND and NOR Layout & Post-Layout Simulation • Realize 2-bit multiplier circuit using Half adder and AND gate. • Realize 6T and 8T SRAM. Pre-Layout Simulation and Post layout simulation • Realization of N Bit counter • Analysis of Timing reports of a given design • Case Study: ASIC Design flow	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Investigate device, circuit & system aspects of digital IC design
CO2	:	Analyze the functionality of digital integrated circuits & systems
CO3	:	Design digital integrated circuit & systems

CO4	:	Evaluate the different performance parameters of a digital integrated circuits & systems

Reference Books

1. Jan M.Rabaey, Anantha Chadrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", (2/e), Pearson 2016, ISBN-13: 978-0130909961

2. Erik Brunvand, "Digital VLSI Chip Design with Cadence and Synopsys CAD Tools", 1st Edition, Pearson 2009, ISBN: 9780321547996

3. CMOS VLSI Design, Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, 2006, Pearson Education, ISBN: 0321149017

4. Sung MO Kang, Yousuf Leblebici, "CMOS Digital Integrated Circuits"; Tata McGrawHill, (3/e), 2003, ISBN: 0-7923-7246-8

Scheme of Continuous Internal Evaluation (CIE): 10 + 30 + 30 + 30 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The average of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 30 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (10), Video based seminar /presentation /demonstration (20) adding upto 30 marks.

Laboratory: Conduction of laboratory exercises, Lab report & observation & analysis (30 Marks), Lab Test (10 Marks) & Innovative Experiment/Concept Design & Implementation (10 Marks) adding up to 50 Marks. The final marks will be reduced to 30 Marks.

Scheme of Semester End Examination (SEE) for 100 marks: Each unit consists of TWO Questions of 16 Marks each. Answer FIVE full questions selecting one from each unit (from 1 to 5). Question No. 11 is compulsory (Laboratory component) for 20 Marks.

Rubric for CIE & SEE for Integrated Theory courses with Laboratory

RUBRIC of CIE			***RUBRIC of SEE***		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Mark**
1	Quizzes - Q1 & Q2	10	Each unit consists of TWO questions of 16 Marks each. Answer FIV full questions selecting ONE from each unit (1 to 5). Question No. 11 is compulsory (Laboratory component) for 20 Mark		
2	Tests - T1 & T2	30			
3	Experiential Learning - EL1 & EL2	30	1 & 2	Unit-1: Question 1 or 2	16
4	Laboratory	30	3 & 4	Unit-2: Question 3 or 4	16
	Total Marks	100	5 & 6	Unit-3: Question 5 or 6	16
NO SEE for Laboratory			7 & 8	Unit-4: Question 7 or 8	16
			9 & 10	Unit-5: Question 9 or 10	16
			11	Laboratory Component (Compulsory)	20
				Total Marks	1

SEMESTER: I						
Course Code	:	MVE203T	**Advanced Embedded System Design**	CIE Marks	:	100
Credits L-T-P	:	3- 1 - 0		SEE Marks	:	100
Hours	:	42L + 28T	*(Professional Core - 3)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Govinda Raju M			

UNIT - I	**9 Hrs**
Introduction to Embedded System Design Introduction, Characteristics of Embedding Computing Applications, Concept of Real time Systems, Challenges in Embedded System Design, Design Process: Requirements, Specifications, Hardware Software Partitioning, Embedded System Architecture Instruction Set Architectures with examples, Memory system Architecture: caches, Virtual Memory, Memory Management, I/O sub system: Busy wait I/O, DMA, Interrupt Driven I/O, Co-Processor & Hardware Accelerators, Processor performance Enhancement: Pipelining, Superscalar Execution, Multi Core CPUs, CPU Power Consumption, Benchmarking Standards: MIPS, MFLOPS, Coremark	
UNIT - II	**9 Hrs**
Designing Embedded System Hardware –I CPU Bus: Bus Protocols, Bus Organization, Introduction to SATA,PCI,PCI-e, Memory Devices and their Characteristics: RAM, EEPROM, Flash Memory, DRAM,DDR,; I/O Devices: Timers and Counters, Watchdog Timers, Interrupt, Controllers, DMA Controllers, A/D and D/A Converters, LEDs,OLEDs	
UNIT - III	**8 Hrs**
Designing Embedded System Hardware –II Programmed IO, Memory Mapped IO, Interfacing Protocols: SPI, I2C, CAN, Reset Circuits, Designing with Processors: System Architecture, FPGA based Design, Processor Selection Criteria	
UNIT - IV	**8 Hrs**
Designing Embedded System Software –I Application Software, System Software, Use of High-Level Languages, Integrated Development Environment tools: Editor, Compiler, Linker, Automatic Code Generators, Debugger, Board Support Library, Chip Support Library, Analysis and Optimization: Execution Time, Energy & Power, Program Size; Program Validation & Verification, Embedded System Coding Standards: MISRA C 2012/CERT	
UNIT - V	**8 Hrs**
Designing Embedded System Software –II OS based Design, Real Time Kernel, Process& Thread, Inter Process Communications, Synchronization, Case Study: RTX-ARM/FreeRTOS, Evaluating and Optimizing Operating System Performance: Response time Calculation, Interrupt Latency, Time Loading, Memory, Loading, Case Study: Embedded Control Applications-Software Coding of a PID Controller, PID Tuning, IoT based Resource Monitoring	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Interpret hardware & software of an embedded systems for real time applications with suitable processor architecture, memory and communication interface.
CO2	:	Design embedded software & hardware to meet given constraints pertaining to both operational and non operational attributes.

CO3	:	Demonstrate the concurrent execution of different operations with support of real time operating systems.
CO4	:	Engage in usage tools to formulate, design and analyze different Applications realized with embedded processors.

Reference Books

1. Embedded Systems – A contemporary Design Tool, James K Peckol, 2nd edition, John Weily, 2008, ISBN: 0-444-51616-6

2. Introduction to Embedded Systems, Shibu K V, 1st edition, Tata McGraw Hill Education Private Limited, 2009, ISBN: 10: 0070678790

3. Embedded Software Primer, David E.Simon, Addison Wesley, 2nd edition, John Weily, 2002, ISBN-13: 978-0201615692

4. The Intel Micro-processors, Architecture, Programming and Interfacing, Barry B.Brey, 6th Edition, Pearson Education, 2008, ISBN-10: 8131726223

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE204L	**ARM CPUs Programming Lab**	CIE Marks	:	50
Credits L-T-P	:	1 - 0 - 1		SEE Marks	:	50
Hours	:	14L + 28P	*(Coding / Skill Laboratory)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Govinda Raju M			

Content	28 Hrs

Experiments on bare metal programming:

1. Write application program to interface LEDs and push buttons to GPIOs of LPC 1857 cortex M3 evaluation board and demonstrate polling-based IO operation.
2. Write Systick_handler to accurately control the delay between toggling of LEDs to support interrupt driven IO.
3. Write driver for ADC0 in LPC 1857 MCU. Display digital value on GLCD and demonstrate analog sensor interface. 4. Write I2C driver for LPC1857. Develop APIs to support I2C. 5. Write driver to support LM75a digital temperature sensor through I2C. Test the functionality by displaying temperature values on GLCD.
6. Write application program to realize FIR filter on STM32F4 cortex M4 development board. Test the filtering operation on signal generated from function generator and interfaced to STM32F4 development board through WolfsonPI codec.

Experiments using RTOS

1. Create a multitasking application program to demonstrate creation of tasks. Task1 is expected to control the blinking two LEDs and Task2 is to change font and colour of the textual display on GLCD concurrently. 2. Create multitasking program to demonstrate task synchronization. Task1 is expected to display LED blinking pattern and Task2 display textual message on GLCD. 3. Create a multitasking program to demonstrate event flags to synchronize task execution. Create four tasks to simulate the operation of stepper motor driver. 4. Create multitasking program to demonstrate IPC using mailbox. Create a task to read a digital value from ADC and send to another task executing concurrently through mailbox. Synchronize the execution of tasks. 5. Create a 'Blinky' project using RL-ARM real time Kernel to simulate the operations of step-motor driver. Use four LEDs blinking to simulate the activation of the four output driver stages. Create other two tasks executing concurrently and competing for GLCD. The first task displays status of LEDs blinking on GLCD and second task displays a string with changing colour of font and background.

Course Outcomes:

After going through this course the student will be able to:

CO1	:	Interpret the information provided in data sheets and schematic diagram to write driver code for different interfaces for micorocontorllers.
CO2	:	Design embedded software to meet given constraints pertaining to both operational and non operational attributes.
CO3	:	Demonstrate the use of real time operating system to support multitasking for concurrent execution of different operations.
CO4	:	Engage in usage of tools to code application programs by using constructs provided by compiler and middleware software packages.

Reference Books

1. Embedded Systems – A contemporary Design Tool, James K Peckol, 2nd edition, John Weily, 2008, ISBN:
0-444-51616-6

2. Introduction to Embedded Systems, Shibu K V, 1st edition, Tata McGraw Hill Education Private Limited, 2009, ISBN: 10: 0070678790

3. Embedded Software Primer, David E.Simon, Addison Wesley, 2nd edition, John Weily, 2002, ISBN-13: 978-0201615692

4. The Intel Micro-processors, Architecture, Programming and Interfacing, Barry B.Brey, 6th Edition, Pearson Education, 2008, ISBN-10: 8131726223

Scheme of Continuous Internal Evaluation (CIE- Laboratory) : Only LAB Course 30 + 10 + 10 = 50. The Laboratory session is held every week as per the timetable and the performance of the student is evaluated in every session. The average of marks over number of experiments conducted over the weeks is considered for 30 Marks i.e (Lab Report, Observation & Analysis). The students are encouraged to implement additional innovative experiments in the lab (10 marks). At the end of the semester a test is conducted for 10 Marks (Lab Test). This adds to 50 Marks.

Scheme of Semester End Examination (SEE- Laboratory) : Only LAB Course 40 + 10 =50. Students will be evaluated for Write-up, Experimental Setup, Experiment Conduction with Results, Analysis & Discussions for 40 Marks and Viva will be conducted for 10 Marks adding to 50 Marks.

Only LAB Courses with 50 Marks

RUBRIC FOR CIE			RUBRIC FOR SEE	
Sl.No	Content	Marks	Content	Marks
1	Write Up, Setup, Conduction Results, Analysis & Discussions	30	1. Write Up, Setup, Conduction 2. Results, Analysis & Discussions	40
2	Innovative Experiment/Concept Design & Implementation	10		
3	Laboratory Internal	10	Viva Voce	10
	Total Marks	50	Total Marks	50

SEMESTER: I						
Course Code	:	MVE301A1	**Low Power VLSI Design**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective A (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr. Srividya P				

UNIT - I	**9 Hrs**
Introduction to Low power:Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices. Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.	
UNIT - II	**9 Hrs**
Power estimation methods **Simulation Power analysis:** SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. **Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.	
UNIT - III	**8 Hrs**
Low Power Design at Circuit level and Logic Level: Low Power Design at Circuit level: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Low Power Design at Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.	
UNIT - IV	**8 Hrs**
Low power Design at Architecture/System Level and Clock distribution: Low power Architecture & Systems: Architectural level estimation & synthesis, Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network	
UNIT - V	**8 Hrs**
Algorithm Level low power Methods: Introduction, design flow, Algorithmic level analysis & optimization. Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Acquire the knowledge of the device physics, principles of analysis tools, circuits levels, logic levels and clock distribution techniques for low power designs.
CO2	:	Identify, formulate, and solve engineering system design problems using low power VLSI design approaches and engineering tools.
CO3	:	Use the techniques and skills in system designing through modern engineering tools such as Logic works SPICE and description languages such as Verilog.
CO4	:	Design a digital system to meet the desired performance with realistic constraints.

Reference Books

1. Low Power Design Methodologies, Jan M. Rabaey and MassoudPedram, Kluwer Academic Publishers, 5th reprint, ISBN 978-1-46 13-5975-3, 2002.

2. Practical Low Power Digital VLSI Design, Gary K. Yeap, Kluwer Academic Publishers, ISBN 978-1-4613-7778-8, 2002.

3. Low-Power CMOS VLSI Circuit DesignKaushik Roy and Sharat Prasad, John Wiley, 2000. ISBN 13 9788126520237

4. Low-Power VLSI Circuits and Systems,Ajit Pal, Springer publications, ISBN: ISBN 978-81-322-1936-1, 2015

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE301A2	**ASIC Design**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective A (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Prof. Sujatha Hiremath				

UNIT - I	**9 Hrs**
Introduction to ASICs: ASIC Design Flow, Introduction to ASICs, Types of ASICs: Full Custom ASIC, Semi-custom based ASIC, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channelless gate array, Structured gate array, Programmable logic devices, Combinational Logic Cell – Sequential logic cell	
UNIT - II	**9 Hrs**
Datapath logic cells: Data Path Elements, Adders, Multipliers, Arithmetic operators. I/O Cell, Cell Compilers. ASIC Library Design: Transistors as Resistors, Transistor parasitic Capacitance. Logical effort: Predicting delay, logical area, logical efficiency, logical paths, multistage cells, optimum delay, and optimum no. of stages. Library cell design.	
UNIT - III	**8 Hrs**
ASIC Construction: Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor-planning tools, Measurement of Delay in Floor-planning, Floor-planning Tools, Channel Definition, I/O and power planning, and clock planning. Placement Terms and Definitions, Measurement of Placement Goals and Objectives, Placement algorithms, iterative placement improvement, Time driven placement methods.	
UNIT - IV	**8 Hrs**
Clock Tree Synthesis and Routing: Goals of CTS, Brief introduction to CTS optimization process, Global Routing, Measurement of Interconnect Delay, Global Routing between blocks, Global Routing inside Flexible Blocks, Back annotation. Detailed Routing: Measurement of Channel Density, Algorithms, Left-Edge Algorithm, Area-Routing Algorithms, Special Routing, Circuit Extraction and DRC.	
UNIT - V	**8 Hrs**
Programmable ASICs: Programmable Asics, Programmable ASIC Logic Cells & Programmable ASIC I/O Cells Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT 1 Module - Xilinx LCA - Altera FLEX - Altera MAX Logic expanders, Power Dissipation in Complex PLDs.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Acquire the knowledge of logic design, physical design design including technology choice, constraints, tool-flow etc.
CO2	:	Apply the optimization techniques in terms of speed and area.
CO3	:	Develop the algorithms required physical design of ASIC flow and implementing the design using FPGA
CO4	:	Create a constrain file required for the back end process of ASIC design.

Reference Books

1.J.S.Smith, " Application – Specific Integrated Circuits", Pearson,2003

2. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996

3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004
4. Andrew B. Kahng , Jens Lienig Igor L. Markov, Jin Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer Dordrecht Heidelberg London New York, 2011

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5].		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE301A3	**VLSI Digital Signal Processing**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective A (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr. Abhay Deshpande				

UNIT - I	**9 Hrs**
Introduction to Digital Signal Processing Systems Introduction, Typical DSP algorithms, DSP Application demands, Scaled CMOS Technologies, Representations of DSP algorithms.	
UNIT - II	**9 Hrs**
Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel processing for low power using Candence tool.	
UNIT - III	**8 Hrs**
Algorithmic strength reduction in filters and transforms Introduction, Parallel FIR filters, Discrete Cosine Transform and Inverse DCT, Parallel Architectures for Rank-Order Filters.	
UNIT - IV	**8 Hrs**
Pipelined and parallel Recursive and Adaptive Filters Introduction, Combined pipelining and parallel processing for IIR filters, Low power IIR digital filter design using pipelining and parallel processing on Cadence, pipelined Adaptive Digital filter design.	
UNIT - V	**8 Hrs**
Programmable Digital Signal Processor Introduction, Evaluation and important features of programmable VLSI-DSP processor, application of VLSI-DSP processor in the field of Wireless Communication, Multimedia Signal Processing etc.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Analyze DSP architectures and CMOS technologies.
CO2	:	Apply pipelining, parallel processing and retiming in DSP.
CO3	:	Design pipelined and parallel recursive adaptive filters.
CO4	:	Develop applications using general purpose digital signal processors.

Reference Books

1. Keshab K. Parthi , "VLSI Digital Signal Processing Systems :Design and implementation" Wiley 1999, 3rd Edition, ISBN: 81-265-1098-6

2. Rulph chasseing, "Digital Signal Processing and Applications " with C6713 and C6416 DSK, Wiley 2005, 2nd
edition, ISBN: 978-0470138663

3. Nasser Kehtarnavaz, "Digital Signal Processing System Design: Lab view based hybrid programming", Academic press 2008, 2nd edition, ISBN: 978-0123744906.

4. Naim Dahnoun "Digital Signal Processing Implementation" Prentice Hall, 2000, ISBN: 978-0201619164

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE301A4	**Real Time Embedded Systems**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective A (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Govinda Raju M			

UNIT - I	**9 Hrs**
Introduction: Overview, Architecture of Real Time Systems: Hardware and Software, Real Time Services. System Resources: Resource Analysis, Real Time Service Utility, Cyclic Executives, Timing Constraints and Modelling of Timing Constraints, Applications of Real Time System.	
UNIT - II	**9 Hrs**
Processing: Scheduling Classes, Scheduler Concepts, Pre-emptive Fixed Priority Policy, Feasibility, Rate Monotonic LUB, Necessary & Sufficient Feasibility, Dead Line Monotonic, Dynamic Priority Policies. I/O Resources: WCET, Intermediate I/O, Execution Efficiency.	
UNIT - III	**8 Hrs**
RTOS Services: Task Creation, Inter Task Communication: Pipes, Message Queues, Mail Box, Memory Mapped Objects; Critical Section, Shared Data Problem, Synchronization: Semaphores, Mutex; Remote Procedure and Sockets. Real Time Memory Management: Process Stack Management, Dynamic Allocation	
UNIT - IV	**8 Hrs**
Handling Resource Sharing and Dependencies Among Real-Time Tasks Resource Sharing among Real-Time Tasks, Priority Inversion, Priority Ceiling Protocol (PCP), Priority Inheritance Protocol (PIP), Highest Locker Protocol (HLP), Types of Priority Inversion Under PCP, Racing, Deadlock, Live lock, Starvation.	
UNIT - V	**8 Hrs**
Examples of Real Time OS: VxWorks: Task Management, Scheduling, Primitive Kernel Services, Application Program development using APIs, Introduction to AI for scheduling	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Aquire the concepts of real-time system and real-time operating system.
CO2	:	Analyse the given requirements, design hardware & software for real time systems.
CO3	:	Apply tools for real time firm ware development & performance analysis.
CO4	:	Design real time applications using RTOS to meet timing Constraints.

Reference Books

1. Real-Time Embedded Systems and Components, Sam Siewert, 2007, Cengage Learning India Edition, ISBN:
9788131502532 2
2. Real-Time Systems: Theory and Practice, Rajib Mall, 2007, Pearson, ISBN 978-81-317-0069-3
3. Real-Time Concepts for Embedded Systems, Qing Li and Carolyn Yao, 2003 CMP Books, ISBN:1578201241
4. Technical Reference Manuals: VxWorks, Posix.

SEMESTER: I						
Course Code	:	MVE301A5	**Semiconductor Device Modelling**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective A (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Ramavenkateswaran N			

UNIT - I	**9 Hrs**
Charge Carriers and Transport Modelling Crystal Structure, Semiconductor Models, Carrier Properties, State and Carrier Distributions, Equilibrium Carrier Concentrations, Drift, Diffusion, Recombination-Generation, Equations of State, Modelling & Simulation examples.	
UNIT - II	**9 Hrs**
PN Junction Diodes:pn Junction Electrostatics, Preliminaries, Quantitative Electrostatic Relationships, I-V Characteristics, The Ideal Diode Equation, Deviations from the Ideal, Small-Signal Admittance, Reverse-Bias Junction Capacitance, Forward-Bias Diffusion Admittance, MS Contacts and Schottky Diodes, Solar cells and LEDs.	
UNIT - III	**8 Hrs**
BJT: Electrostatics, Performance Parameters, Ideal Transistor Analysis, General Solution, Simplified Relationships, Ebers-Moll Equations and Model, Deviations from the Ideal, Modern BJT Structures.	
UNIT - IV	**8 Hrs**
MOS: Electrostatics, Capacitance-Voltage Characteristics, Quantitative ID/VD Relationships, Square-Law Theory, Bulk-Charge Theory, a.c. Response, Small-Signal Equivalent Circuits, Cutoff Frequency, Small-Signal Characteristics	
UNIT - V	**8 Hrs**
Emerging electron devices (Qualitative approach): Introduction, HEMT, HBT, Fin-FET. Nanowire-FET, quantum and molecular devices, energy storage and harvesting Electronics devices	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Apply semiconductor models to analyse carrier densities and carrier transport.
CO2	:	Analyse basic governing equations to analyse semiconductor devices.
CO3	:	Design the p-n junction, Schottky barrier diodes and emerging semiconductor devices.
CO4	:	Model & Simulate microelectronic devices using software tools.

Reference Books

1. Robert F. Pierret, "Semiconductor Device Fundamentals", Pearson, 2006, ISBN 9780201543933.
2. Y.P. Tsividis, Colin McAndrew, "Operation and modelling of the MOS Transitor", 3rd Edition, 2014, Oxford
Univ Press, ISBN:978-0195170153.
3. Yuan Taur, Tak H. Ning, "Fundamentals of Modern VLSI Devices", 2ndedition , 2013Cambridge University
Press, ISBN: 978-1107635715.
4. Semiconductor Simulation Tools, “https://nanohub.org/groups/semiconductors”

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions
with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE302B1	**Static Timing Analysis**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective B (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr. Shylashree N				

UNIT - I	**9 Hrs**
Introduction: Basics of timing concepts- Propagation delay, slew, timing arcs,min and max timing paths, clock domains. Delay Concepts for Digital Designing: Types of Delays in Digital Circuits, Different Cause for Delay Timing parameters of digital circuits: Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design, Clock Concepts The STA Environment- timing path groups, modeling of external attributes, virtual clocks, refining the timing analysis, point-to-point specification	
UNIT - II	**9 Hrs**
Resources for Static Timing Analysis Flow:Libraries,Netlist, Parasitics for Delay Calculation:Device Parasitics, Interconnects, Parasitic Extraction Formats, linear v/s. non-linear delay model. Clock Network Optimization:Metrics, clock skew-scheduling,handling variability. Parallel Timing Optimization:Circuit partitioning for independent timing regions. Post-Silicon Timing Validation:Introduction,sources of post-silicon timing failure, post-silicon tuning	
UNIT - III	**8 Hrs**
Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis,Strategy of Crosstalk on Nanometre Design: Cause for Crosstalk on Integrated Circuits, Cross talk Prevention Methods	
UNIT - IV	**8 Hrs**
Constraints for STA:Clock Constraints, Other Timing Constraints, 5.2.2 External Delays of DUA,Timing Exceptions:Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate	
UNIT - V	**8 Hrs**
Timing Violations and Verification:Slack, Critical Path of Timing Report, Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Recovery and Removal Violation Check, Input/output Timing Path Checks ,DRC Violation Check, Multi Speed Clock Domain,Crosstalk Checks,Techniques to Fix Timing Violation:Techniques to Fix Setup Violations,Techniques to Fix Hold Violations,Time borrowing.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Apply the basic concepts of STA to evaluate the delay of the circuit and analyze the generated report to identify critical issues and bottle neck for the violation and suggest the techniques to make the design to meet timing.
CO2	:	Identify cell delays from a library and calculate output slew degradation and use wire-load information to calculate net delays. Also analyze cross talk effect on timing analysis.
CO3	:	Write the own constraints file and create the environment required for the given design and its specification to undergo for analysis using perl/TCL scripts.
CO4	:	Set timing constraints, including clocks and external delay and analyze report to identify timing problems.

Reference Books

1.Static Timing Analysis for Nanometer Designs: A Practical Approach, J.Bhasker, R.Chadha, 2009, Springer,
ISBN:978-0-387-93820-2.

2. Static Timing Analysis for VLSI circuits, R.Jayagowri, Pushpendra S.Yadav,2018, MEDTECH,A Division of Scientific International, ISBN: 978-9-38-721006-6.

3. Timing Analysis and Optimization of Sequential Circuits, Naresh Maheshwari and Sachin S.Sapatnekar, 1999, Springer Science, Business Media, LLC, Library of Congress Cataloging-in-Publication Data, ISBN:978-1-4615-5637-4

4. Constraining Designs for Synthesis and Timing Analysis - A Practical Guide to Synopsys Design Constraints (SDC), Sridhar Gangadharan and Sanjay Churiwala, Springer Science , Business Media, LLC, Library of
Congress Cataloging-in-PublicationData,2013,ISBN:978-1-4614-3269-2

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full
question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE302B2	**System on Chip Design**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective B (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr. Kiran V				

UNIT - I	**9 Hrs**
Review of Moore's law and CMOS scaling, benefits of System On Chip integration in terms of cost, power, and performance. Comparison on System on Board, System on Chip, and System-in-Package. Typical goals in SoC design cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.	
UNIT - II	**9 Hrs**
System On Chip Design Process: A canonical SoC Design, SoC Design flow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software co design, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc	
UNIT - III	**8 Hrs**
Embedded Memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.	
UNIT - IV	**8 Hrs**
Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in anNoC. Packet switching and wormhole routing.	
UNIT - V	**8 Hrs**
MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs,Multichip Packages and chipset based design, Performance and flexibility for MPSoCs design Case Study: A Low Power Open Multimedia Application Platform for LTE.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Learn about the blocks in the system on chip design and its performance.
CO2	:	Analyze the design flow and verification of IPs used in system on chip.
CO3	:	Exposure the concepts of different memory and interconnection methods in SoC
CO4	:	Design & Develop the algorithms required for the design of IP and SoC and Exposure to the concept of MPSoCs

Reference Books

1. SudeepPasricha and NikilDutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.

2. Rao R. Tummala, MadhavanSwaminathan, "Introduction to system on package sopMiniaturization of the Entire Syste", McGraw-Hill, 2008.

3. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley Student Edition.

4. Michael Keating, Pierre Bricaud, "Reuse Methodology Manual for System on Chip designs", Kluwer Academic
Publishers, 2nd edition, 2008.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE		
Sl.No	**Content**	**Marks**
1	Quizzes - Q1 & Q2	20
2	Tests - T1 & T2	40
3	Experiential Learning - EL1 & EL2	40
	Total Marks	100

RUBRIC for SEE		
Q. No	**Contents**	**Marks**
Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
1 & 2	Unit-1: Question 1 or 2	20
3 & 4	Unit-2: Question 3 or 4	20
5 & 6	Unit-3: Question 5 or 6	20
7 & 8	Unit-4: Question 7 or 8	20
9 & 10	Unit-5: Question 9 or 10	20
	Total Marks	100

SEMESTER: I						
Course Code	:	MVE302B3	**IC Technology**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective B (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr. Ramavenkateswaran N				

UNIT - I	**9 Hrs**
An Introduction to Microelectronic Fabrication: Semiconductor Substrates, Crystallography and Crystal Structure, Crystal Defects, Czochralski Growth, Bridgman Growth of GaAs, Float Zone Growth, Wafer Preparation and Specifications	
UNIT - II	**9 Hrs**
Hot Processingand Ion Implantation: Diffusion, Fick's Diffusion Equation in One Dimension, Atomistic Models of Diffusion, Analytic Solutions of Fick's Law, Diffusion Coefficients for Common Dopants, Analysis of Diffused Profiles, Diffusion in SiO2, Simulations of Diffusion Profiles	
UNIT - III	**8 Hrs**
Thermal Oxidation: The Deal–Grove Model of Oxidation, The Linear and Parabolic Rate Coefficients, The Initial Oxidation Regime, The Structure of SiO2, Oxide Characterization, The Effects of Dopants During Oxidation and PolysiliconOxidation, Silicon Oxynitrides, Alternative Gate Insulators, Oxidation Systems, Numeric Oxidations	
UNIT - IV	**8 Hrs**
Ion Implantation: Idealized Ion Implantation Systems, Coulomb Scattering,Vertical Projected Range, Channeling and Lateral Projected Range, Implantation Damage, Shallow Junction Formation, Buried Dielectrics, Ion Implantation Systems: Problems and Concerns, Numerical Implanted Profiles	
UNIT - V	**8 Hrs**
Resistivity: Two-Point Versus Four-Point Probe, Wafer Mapping, Resistivity Profiling, Contactless Methods, Conductivity Type,Contact Resistance and Schottky Barriers, Metal-Semiconductor Contacts,Contact Resistance, Measurement Techniques, Schottky Barrier Height,Comparison of Methods	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Aquire the concepts of fabrication process and characterization techniques of IC technology.
CO2	:	Analysis of different process parameters in IC fabrications.
CO3	:	Define different standard operating procedure in IC fabrication.
CO4	:	Evaluate different analytic techniques in fabrication process.

Reference Books

1. Stephen A. Campbell, "Fabrication Engineering at the Micro and Nanoscale", Third Edition, University of Minnesota, Oxford University Press, 2008.

2. Dieter K. Schroder, "Semiconductor Material and Device Characterization", Wiley - IEEE, 2006.

3. Yuan Taur, Tak H. Ning, "Fundamentals of Modern VLSI Devices", 2ndedition , 2013 Cambridge University Press, ISBN: 978-1107635715.

4. Richard Jaeger, "Introduction to Microelectronic Fabrication": Volume 5, Modular Series on Solid State Deviced, 13 November 2001.
Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100 **QUIZZES:** Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks. **TESTS:** Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks. **EXPERIENTIAL LEARNING:** Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.
Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5].		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE302B4	**IOT System Design and Architecture**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective B (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Govinda Raju M			

UNIT - I	**9 Hrs**
IOT Essentials Evolution of IoT, IoT characteristics, IoT enabling technologies, Planning for an IoT solution, IoT use case development - Need and goals, IoT Architecture reference model, Functional blocks of IoT- Communication and security Model, Service oriented architecture, Event-driven architecture, Applications and standards. IoT Communication Architecture and Protocols Communication models for IoT, 6LoWPAN, IPv4/IPv6, IoT communication protocols - MQTT, CoAP, LoRaWAN, RTLS, RPL, Communication APIs	
UNIT - II	**9 Hrs**
IoT Security and Privacy IoT risks and security challenges, IoT security architecture - A trust model, Restricting network access through security groups- Specific user access control, Data confidentiality and availability, User Authentication/Authorization methods, Block chain for IoT security and privacy.	
UNIT - III	**8 Hrs**
Data Analytics Need for data analytics, Data generation, Data pre-processing, Handling imbalanced data sets, Missing values, Outliers, Intelligent IoT systems –Supervised and Unsupervised machine learning algorithms, Deep learning for IoT- Predictive analytics, Python functions and modules for data analytics, Big Data analytics and frameworks.	
UNIT - IV	**8 Hrs**
Data Analytics in Cloud Layered cloud architecture for data analytics, Elasticity in cloud for data warehousing, Virtualization for Data-center automation, Real-time cloud data analytics tools, AI Services-Data based decisions, Cloud data lake, Exploratory data analysis, Open source cloud platforms and services. Edge Computing Introduction to Edge/Fog computing, Edge nodes and gateway, Node to edge interfaces, Protocol and standards for edge devices, IoT edge architecture, IoT supported hardware-Raspberry pi, ARM Cortex Processors, Software Platforms for IoT Edge - Raspbian Pi OS, RIOT, Python packages for edge computing, Edge security, Real time applications of edge computing.	
UNIT - V	**8 Hrs**
IoT Architecture: Use Cases Roadmap for complete IoT solution, Open source IoT platforms, IoT solution to Health care, Automotive applications, Smart IoT architecture for Retail, Logistics and Farming, Intelligent IoT architecture for Home automation, Industry applications, Smart city and other applications to cater the societal requirements.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Assimilate the technologies that enable IoT and interpret the different components in IoT architecture.
CO2	:	Envision the IoT communication architecture models and the protocol stack for the cost-effective design of IoT applications on different platforms.
CO3	:	Analyze cloud platform services to perform IoT data analytics and make the system intelligent.
CO4	:	Perceive the data analytics tools and gain knowledge to devise an intelligent IoT system.

Reference Books
1. Internet of Things- A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015.
2. Cloud Computing Security: Foundations and Challenges, John R. Vacca, CRC Press, 2016.
3. Internet of Things and Big Data Analytics towards Next-Generation Intelligence, Dey, Hassanien, Bhatt, Ashour and Satapathy, Springer, 2018.
4. Designing the Internet of Things, Adrian McEwen & Hakim Cassimally, Wiley, 2013.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: I						
Course Code	:	MVE302B5	**VLSI for Data Conversion Circuits**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42L	*Elective B (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Chinmaye R			

UNIT - I	**9 Hrs**
Basic Sampling Circuits NMOS, PMOS and Transmission Gate switch, Distortion due to switch, Speed and Precision considerations, Charge injection, Clock feedthrough, Thermal noise in sample and holds, Charge injection cancellation – Dummy switch, complementary switches, differential circuits, Bottom plate sampling, Gate bootstrapped switch.	
UNIT - II	**9 Hrs**
Building Blocks of Data Conversion Systems – Operational Amplifiers Two stage Opamp, design of buffer stage, Operational Transconductance Amplifier, compensating the Opamp for stability, characterizing the Opamp open loop gain, common mode range, common mode rejection ratio, power supply rejection ratio. CMOS Comparators: Regenerative latch, comparator metastability, Strong-ARM Latch Design	
UNIT - III	**8 Hrs**
Switched Capacitor Amplifiers Common mode feedback (CMFB) – resistive CM detector, CMFB compensation, single- stage differential opamp. Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers, Non idealities in SC Amplifiers – Finite gain, DC offset, Gain-Bandwidth Product. Fully differential SC circuits, DC negative feedback in SC circuits. Switched-capacitor CMFB: design, analysis.	
UNIT - IV	**8 Hrs**
Analog to Digital Converter- Static specifications: INL, DNL; Dynamic specifications: SNDR, DR, SFDR, linearity.Flash ADC, SAR ADC, Pipelined ADC, Sigma Delta ADC.	
UNIT - V	**8 Hrs**
Digital to Analog Converter Static performance of DAC – DAC transfer characteristics, Ideal DAC transfer curve, offset, gain error, monotonicity, DNL and INL. Nyquist DAC architectures - Binary-weighted DAC, Unit- element (or thermometer-coded) DAC, Segmented DAC, Resistor-string, current-steering, Current cell design in current steering DAC, charge-redistribution DACs, High speed DACs.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Analyse and Design Sample and Hold circuits
CO2	:	Analyse Switched Capacitor Amplifiers and its non idealities.
CO3	:	Design various types of ADC/DAC for a given specification
CO4	:	Evaluate the different performance parameters of ADC/ DAC

Reference Books

1. Behzad Razavi, “Principles of Data Conversion System Design” Wiley-IEEE Press,1994
2. Fundamentals of Microelectronics, Behzad Razavi, 2nd Edition, 2013, Wiley, ISBN-10: 1118156323
3. Electronic Devices and Circuits , Jacob Millman, Christos C Halkias&Satyabrata Jit, 2nd edition, 2008, Tata
McGraw Hill publication,. ISBN: 0070634556
4. David A.Johns, Ken Martin, “Analog Integrated Circuit Design” John Wiley & Sons Inc. 1997

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5].		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II						
Course Code	:	**MIM431T**	**RESEARCH METHODOLOGY**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Common Course to all M.Tech Programs*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Rajeswara Rao K V S			

UNIT - I	8 Hrs
Research Problem: Problem Solving – General Problem Solving, Logical Approach, Soft System Approach, Creative Approach, Group Problem Solving Techniques for Idea Generation. Formulation of Research Problems – Approaches to Research Problem, Exploration for Problem Identification, Hypothesis Generation and Formulation of the problem.	
UNIT - II	9 Hrs
Research Design: Experimental Design – Principles of Experiment, Laboratory Experiment, Experimental Design, Quasi Experimental Design, Action. Research, Validity and Reliability of Experiment and Quasi Experiments. Ex Post Facto Research – Exploratory Research, Historical Research, Descriptive Research, Field Studies, Survey Research, Qualitative Research Methods.	
UNIT - III	8 Hrs
Research Design for Data Acquisition: Measurement Design – Primary types of Measurement scales, Validity and Reliability Measurement, Sample Design – Non-Probability Sampling, Probability Sampling. Data Collection Procedures – Sources of secondary data, Primary data collection methods, Validity and Reliability of data collection procedures.	
UNIT - IV	9 Hrs
Data Analysis: Exploratory Data Analysis, Statistical Estimation, Hypothesis Testing, Parametric Tests, Non-Parametric Tests, Multiple Regression, Factor Analysis, Cluster Analysis	
UNIT - V	8 Hrs
Research Proposal: Purpose, Types, Development of Proposal, Evaluation of Research Proposal. Report Writing: Pre-writing consideration, Format of Reporting, Briefing, Best practices for Journal writing.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Recognize the principles and concepts of research types, data types and analysis procedures.
CO2	:	Apply appropriate method for data collection and analyze the data using statistical principles.
CO3	:	Express research output in a structured report as per the technical and ethical standards.
CO4	:	Develop a research design for the given engineering and management problem context.

Reference Books:

1. Krishnaswami, K.N., Sivakumar, A. I. and Mathirajan, M., Management Research Methodology, Integration of Principles, Methods and Techniques, 17th Impression, Pearson India Education Services Pvt. Ltd, 2018. ISBN: 978-81-7758-563-6

2. William M. K. Trochim, James P. Donnelly, The Research Methods Knowledge Base, 3rd Edition, Atomic
Dog Publishing, 2006, ISBN: 978-1592602919

3. Kothari C.R., Research Methodology Methods and Techniques, 4th Edition, New Age International Publishers, 2019, ISBN: 978-93-86649-22-5.
4. Levin, R.I. and Rubin, D.S., Statistics for Management, 8th Edition, Pearson Education: New Delhi, 2017, ISBN-13- 978-8184957495.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes – Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests – T1 & T2	40			
3	Experiential Learning – EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II						
Course Code	:	MVE331I	**Analog IC Design**	CIE Marks	:	100
Credits L-T-P	:	3-0-1		SEE Marks	:	100
Hours	:	42L + 28P	*Theory & Practice - (Professional Core - 3)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr.Shylashree N			

UNIT - I	**9 Hrs**
MOS transistors: Components available in a CMOS process, MOS small signal models, concept of fT,noisemodel. Single stage Amplifiers: Basic concepts, dc analysis, small signal analysis and noise analysis of common source and common gate stage, power, bandwidth, impedance and frequency scaling of circuits, Frequency response of CS amplifier, Cascode stage-Folded Cascode. Current Mirror: Basic Current Mirrors, Cascode current Mirrors, amplifiers biased at constant currents.	
UNIT - II	**9 Hrs**
Differential Amplifiers: Single ended and differential operation, Common mode response, differential pair with active loads, Gilbert cell Operational Amplifier:One stage op-amp,two stage op-amp,Telescopic Cascode opamp,Telescopic Cascode opamp frequency response, Folded Cascode op-amp-dc gain, Telescopic and folded Cascode opamp, PSRR, Two stage opamp-topology, frequency response, gain boosting, common mode feedback.	
UNIT - III	**8 Hrs**
Noise:Resistors,MOSFET,Inputandoutputreferrednoise,basicamplifierstages– CSand CGstage Feedback:Non-idealities-finite dc gain,effect of additional poles & zeros,sense and return mechanisms, feedback topologies, Effect of loading.	
UNIT - IV	**8 Hrs**
Stability analysis and Frequency compensation: Stability of Feedback: Basic Concepts, Instability and the Nyquist Criterion. Frequency Compensation: Concepts and Techniques for Frequency Compensation–Domin ant pole, Miller Compensation Band gap reference: Band gap reference, Constant current and constant gm bias generators, reducing supply sensitivity Low drop out regulators: Basic requirements and constraints	
UNIT - V	**8 Hrs**
Analog Filters: Classification of filters, transfer function of filters, Second order filters, active filters – sallen and key filters, KHN biquad. Phase Locked Loops : Simple Phase locked loop, Charge pump PLL, Non-ideal effects - Jitter & Phase noise,Applications	
LABORATORY	28 Hrs
1. Studyof DCandsmallsignalmodelsof aMOSTransistor 2. Design of MOS current sources and mirrors 3. Design of single stage amplifiers–CS Amplifier with different loads 4. Design of aMOS Differential amplifier with an active load 5. Design of a cascode amplifier, double cascode and triple cascode amplifier 6. Design of Telescopic opamp 7. Design ofa2-stageCMOSOp-Amp 8. Design of Band GapReference circuit 9. Post-layout simulation of any two circuits	

Course Outcomes:

After going through this course the student will be able to:

CO1	:	Apply the knowledge of MOSFET based discrete amplifier to investigate various designs.
CO2	:	Analyze the functionality of analog circuit and systems.
CO3	:	Design and implement analog integrated circuits.

CO4	:	Evaluate the different performance parameter of analog integrated circuits.

Reference Books

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi,McGraw Hill Edition, 2002, ISBN:0-07-238032-2

2. CMOS Circuit Design, Layout and Simulation, R.Jacob Baker, Harry W. Liand David E.Boyce, IEEE Press, 2002, ISBN:81-203-1682-7

3. Analysis and design of Analog Integrated Circuits, Gray, Hurst, Lewis, and Meyer: 4thEdition, John Wiley &Sons, ISBN-10:0470245999

4. CMOS Analog Circuit Design, Phillip E. Allen and Douglas R. Holberg, 2ndEdition Oxford University Press, February 2002,ISBN:9780199765072

Scheme of Continuous Internal Evaluation (CIE): 10 + 30 + 30 + 30 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The average of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 30 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (10), Video based seminar
/presentation /demonstration (20) adding upto 30 marks.

Laboratory: Conduction of laboratory exercises, Lab report & observation & analysis (30 Marks), Lab Test (10 Marks) & Innovative Experiment/Concept Design & Implementation (10 Marks) adding up to 50 Marks. The final marks will be reduced to 30 Marks.

Scheme of Semester End Examination (SEE) for 100 marks: Each unit consists of TWO Questions of 16 Marks each. Answer FIVE full questions selecting one from each unit (from 1 to 5). Question No. 11 is compulsory (Laboratory component) for 20 Marks.

Rubric for CIE & SEE for Integrated Theory courses with Laboratory

RUBRIC of CIE			***RUBRIC of SEE***		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Mark**
1	Quizzes - Q1 & Q2	10	Each unit consists of TWO questions of 16 Marks each. Answer FIV full questions selecting ONE from each unit (1 to 5). Question No. 11 is compulsory (Laboratory component) for 20 Mark		
2	Tests - T1 & T2	30			
3	Experiential Learning - EL1 & EL2	30	1 & 2	Unit-1: Question 1 or 2	16
4	Laboratory	30	3 & 4	Unit-2: Question 3 or 4	16
	Total Marks	100	5 & 6	Unit-3: Question 5 or 6	16
NO SEE for Laboratory			7 & 8	Unit-4: Question 7 or 8	16
			9 & 10	Unit-5: Question 9 or 10	16
			11	Laboratory Component (Compulsory)	20
				Total Marks	1

SEMESTER: II							
Course Code	:	MVE332T	**System Verilog for Design and Verification**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42 L	*(Professional Core - 4)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr. Chinmaye R				

UNIT - I	**9 Hrs**

Introduction to SystemVerilog as a Verification Lamguage(HDVL): SystemVerilog standards, SystemVerilog key enhancements for hardware design. Advantages of System Verilog over Verilog, Data Types: Verilog data types, System Verilog data types, integer type and Non-integer type. Integer Type: 2 - State Data types, Bit, byte, shortint, int, longint; 4 - State data types, reg, logic, integer. Non-Integer Type: time, shortreal, real, realtime. Enumerated data types, User Defined data types, Struct data types, Interfaces, Packages, Type Conversion: Dynamic casting, Static Casting, Strings, Memories: Arrays, Dynamic Arrays, Multidimensional Arrays, Packed Arrays, Associative Arrays, Queues, Array Methods, Tasks and Functions: Verilog Tasks and Functions, Enhancements in S.V, Void Functions, Return Statement, Passing Arguments, Arguments Passing by Name,
Default Arguments, Passing Arguments by Value, Passing Arguments by Reference.

UNIT - II	**9 Hrs**

Testbench building and Connecting to DUT: Verilog interface signals - Limitations of Verilog interface signals, SystemVerilog interfaces, SystemVerilog port connections, Interface instantiation 2.4. Interfaces Arguments, Interface Modports, Interface References, Tasks and functions in interface, Verilog Event Scheduler, SystemVerilog Event Scheduler, Clocking Block, Input and Output Skews, Typical Testbench Environment,
Verification plan.

UNIT - III	**8 Hrs**

OOPs Concepts, Constrained Randomization & Threads and Inter-process
Communication: OOP Concepts
Overview of Classes, Properties and Methods in the Classes, Instance/Object Creation, New Constructor, Null Object handles, Accessing Members, this Keyword, Creating an Object, Objects
Assignments, Copying an Object: Shallow Copy, Deep Copy.
Inheritance: Concept of Inheritance, Super Keyword, Static properties, Overriding Methods, Polymorphism - $cast, Virtual Classes, Parameterized Classes. Constrained Randomization
Random Variables - rand and randc, Randomize( ) Method - Pre/Post Randomize( ) methods, Constraints in the class, Rand_mode and constraint_mode, Constraint and Inheritance, Constraint Overriding, Set Membership, Distribution Constraints, Conditional Constraints - . implication (->),. if/else, Inline Constraints.
Threads and Inter-process Communication
Threads, Fork-Join/Join_any/Join_none, Communication –BuildingaTestbenchwithThreadsandIPC.

UNIT - IV	**8 Hrs**

Universal Verification Methodology and Formal Verification
Introduction to Open Verification Methodology and Universal Verification Methodology, Overview of OVM, UVM Base Classes and Simulation Phases in OVM and UVM macros. Environment structure of OVM and UVM, Connecting DUT and Testbench. Introduction to Formal verification andTypes of Formal techniques, Formal equivalence checking and Formal property checking, Class based Verification.

UNIT - V	**8 Hrs**

Functional Coverage andAssertion Based Verification: Functional Coverage
Coverage Definition, Code Coverage, Functional Coverage: Cover Group, Creating Cover Group Instances, Coverpoints, Bins - . implicit bins, . Explicit bins, Bin creation, Vector and Scalar bins, Cross products, Intersect, Select Expressions, Conditional Expression (iff), Illegal bins, Ignore bins, Coverage Analysis, Covergroup Built-in Methods-.Sample(), .get_coverage(),
.get_instance_coverage(), .set_instance_name(string), .start(), . stop() Assertion Based Verification
Introduction, Types of Assertions - . Immediate, . Concurrent, Assertion Properties - . Writing Properties,

Sequences - . Sequence Composition, . and, or, intersect, Advanced SVA Features - . Expect, Binding, Assertion Coverage
Course Outcomes: After going through this course the student will be able to:

CO1	:	Demonstrate the use SystemVerilog data types for digital system design and functional verification.
CO2	:	Demonstrate the skill on writing test-benches for design digital systems and connecting them with the design.
CO3	:	Verify and Analyze the complete systems through robust verification method such as assertion based verification and class based verification.
CO4	:	Design and verify the digital systems such as FIFOs, memories, ATM interfaces, etc. using the learnt methods and demonstrate the skills.

Reference Books

1. C Spear, "SystemVerilog for Verification-A Guide to Learning the Testbench Language Features," Springer Science, IEEE press, ISBN-13: 978-0387-2703-64, 2006.

2. Stuart Sutherland, Simon Davidmann and Peter Flake, "SystemVerilog for Design - A Guide to Using SystemVerilog for Hardware Design and Modeling," 2E, Springer Science, ISBN-13: 978-0387-3339-91, 2006.

3. IEEE Computer Society, "IEEE Standard for SystemVerilog-Unified Hardware Design, Specification and Verification," IEEE Press, ISBN: 978-0-7381-6129-7, 2009

4. Doulos, "SystemVerilog golden reference guide-A concise guide to SystemVerilog IEEE Standard-1800-2009," Version 5.0, ISBN: 0-9547345-9-9, 2012.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE

Sl.No	Content	Marks
1	Quizzes - Q1 & Q2	20
2	Tests - T1 & T2	40
3	Experiential Learning - EL1 & EL2	40
	Total Marks	100

RUBRIC for SEE

Q. No	Contents	Marks
Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
1 & 2	Unit-1: Question 1 or 2	20
3 & 4	Unit-2: Question 3 or 4	20
5 & 6	Unit-3: Question 5 or 6	20
7 & 8	Unit-4: Question 7 or 8	20
9 & 10	Unit-5: Question 9 or 10	20
	Total Marks	100

SEMESTER: II						
Course Code	:	MCS333C1	**Development of Modem SoCs for Wireless, Wireline and IOT Applications**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42 L	*Elective C (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. S Ravishankar			

UNIT - I	**9 Hrs**
Algorithms for single carrier communications and Multicarrier Communication modems Algorithms for MIMO Applications, Single carrierChannel estimation for DSL , Wi-Fi and cellular standards	
UNIT - II	**9 Hrs**
DSL standards for Transreceiver, Synchronization, Channel estimation, Mapping standards to Modem SoC hardware and firmware, DSL standards for Testing	
UNIT - III	**8 Hrs**
802.11 standards for Transreceiver, Synchronization,Channel estimation, Mapping standards to Modem SoC hardware and firmware, 802.11 standards for Testing	
UNIT - IV	**8 Hrs**
LTE standards for Transreceiver, Synchronization,Channel estimation, Protocol Stacks Mapping standards to Modem SoC hardware and firmware, LTE standards for Testing	
UNIT - V	**8 Hrs**
Development Life Cycle for a Modem, Three case studies of SoCfor Modem Implementation. Scenarios for Mobility management in networks, Session initialization management and in-service monitoring in networks, IOT Applications	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Aquire the concepts of synchronization and channel estimation algorithms for DSL, WiFi and LTE.
CO2	:	Associate the standards sections to Training, Initialization and show time with in-service monitoring algorithms
CO3	:	Analyse typical SoC platforms in terms of their hardware and software capabilities to implement algorithms with task scheduling.
CO4	:	Develop runtime code to evaluate performance of a training, Initialization and showtime on the typical SoCs.

Reference Books

1. ITU-T TELECOMMUNICATION STANDARDIZATION SECTOR , “Asymmetric digital subscriber line transceivers 2 (ADSL2) G.992.3 , April 2009.

2. IEEE Standard for Information Technology Telecommunications and Information Exchange between Systems Local and Metropolitan Area Networks— Specific Requirements Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, IEEE Std 802.11™-2020

3. European Telecommunications Standards Institute (ETSI), “ 5G; NR;Base Station (BS) radio transmission and reception (3GPP TS 38.104 version 16.4.0 Release 16)”, July 2020

4. ADSL: Standards, Implementation, and Architecture, by Charles K. Summers CRC Press, CRC Press LLC, ISBN: 084939595x Pub Date: 06/21/99

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

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Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
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1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II						
Course Code	:	MVE333C2	**VLSI Memory Chip Design**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42 L	*Elective C (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr.Shylashree N			

UNIT - I **9 Hrs**

An Introduction to Memory Chip Design: The Internal Organization of Memory Chips, Categories of Memory Chip, General Trends in DRAM Design and Technology, General Trends in SRAM Design and Technology.
Non-Volatile Memory Design: Main Features of Non-Volatile Memories, Program, Erase, Distributions and Cycles, Read Mode Architecture, Write Mode Architecture, Erase Mode Architecture, Elements of Reliability, Influence of Temperature and Supply Voltage.

UNIT - II **9 Hrs**

DRAM Circuits: Introduction, The catalog Specifications of the Standard DRAM, The Basic Configuration and Operation of the DRAM Chip, Fundamental Chip Technologies, The Multidivided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits.

UNIT - III **8 Hrs**

Low-Power Memory Circuits:Introduction, Sources and Reduction of Power Dissipation in a RAM Subsystem, Sources of Power Dissipation in the RAM Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits. The Organization of the Memory Array:Introduction: EPROM Memories, Flash Memory Organization: The Sectors,An Array of Sectors, Other Types of Array.

UNIT - IV **8 Hrs**

Program and Erase Algorithms:Memory Architecture from the Program-Erase Functionality Point of View, User Command to Program and Erase, Program Algorithm for Bi-Level Memories, Program Algorithm for Multilevel Memories, Erase Algorithm, Test Algorithms. Circuits Used in Program and Erase Operations:Introduction, Dual Voltage Devices, Charge Pumps, Different Types of Charge Pumps, High Voltage Limiter, Charge Pumps for Negative Voltages, Voltage Regulation Principles, Gate Voltage Regulation, Drain Voltage Regulation and Temperature Dependence.

UNIT - V **8 Hrs**

Program and Erase Controller:FSM Controller, STD Cell Implementation of the FSM, PLA Implementation of the FSM, Microcontroller. Redundancy and Error Correction Codes:Redundancy, Redundancy & Read Path, Yield, UPROM Cells, The First Read After Power On Reset, Error Correction Codes.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Aquire the knowledge about memory chip design and its technology
CO2	:	Explore various design strategies to be followed for designing DRAM circuits
CO3	:	Design and optimize semiconductor memory cell for a given specification
CO4	:	Design memory array of a given size and measure various performance metrics.

Reference Books

1. VLSI-Design of Non-Volatile Memories: G.Campardo, R.Micheloni and D.Novosel, 2007, Springer, ISBN-10:8181288076, ISBN-13 : 978-8181288073

2. VLSI Memory Chip Design, KiyooItoh, Soft cover reprint of hardcover 1st ed. 2001 edition, Springer, ISBN-10 : 3642087361, ISBN-13 : 978-3642087363

3. Embedded Memory Design for Multi-core and system on chip, Baker Mohammad,Softcover reprint of the original 1st ed. 2014 edition,Springer, ISBN-10 : 1493948016, ISBN-13 : 978-1493948017.

4. Cache and Memory Hierarchy Design: A Performance Directed Approach, StevenPrzyblylski, Morgan Kaufmann (30 June 1990), ISBN-10 : 1558601368, ISBN-13 : 978-1558601369.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

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EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II						
Course Code	:	MVE333C3	**Robotics and Industrial Automation**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42 L	*Elective C (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Abhay Deshpande			

UNIT - I	**9 Hrs**
Introduction: Automation and Robotics, Historical Development, Definitions, Basic Structure of Robots, Robot Anatomy, Complete Classification of Robots, Fundamentals about Robot Technology, Factors related to use Robot Performance, Basic Robot Configurations and their Relative Merits and Demerits, the Wrist & Gripper Subassemblies. Kinematics of Robot Manipulator: Introduction, General Mathematical Preliminaries onVectors& Matrices, Direct Kinematics problem, Geometry Based Direct kinematics problem, Coordinate and vector transformation using matrices, Rotation matrix, Inverse Transformations, Problems.	
UNIT - II	**9 Hrs**
Trajectory Planning: – Introduction, Trajectory Interpolators, Basic Structure of TrajectoryInterpolators, Cubic Joint Trajectories. General Design Consideration on Trajectories:- 4-3-4 & 3-5-3 Trajectories. (SLE: Admissible Motion Trajectories) Dynamics of Robotic Manipulators: Introduction,. Preliminary Definitions, GeneralizedRobotic Coordinates, Jacobian for a Two link Manipulator, Euler Equations, TheLagrangian Equations of motion.	
UNIT - III	**8 Hrs**
Robot Sensing & Vision: Various Sensors and their Classification, Use of Sensors and SensorBased System in Robotics, Machine Vision System, Description, Sensing, Digitizing, Image Processing and Analysis and Application of Machine Vision System, Robotic Assembly Sensors and Intelligent Sensors. Industrial Applications: Objectives, Automation in Manufacturing, Robot Application inIndustry, Task Programming, Robot Intelligence and Task Planning, Modern Robots, Future Application and Challenges and Case Studies. (SLE: Goals of AI Research, AI Techniques)	
UNIT - IV	**8 Hrs**
Modeling and control: Kinematic modeling of multi-link flexible robots, Dynamics and control of flexible link manipulators. Overview of PLC Hardware, numeric data handling, system addressing, and programming software. Robot Manipulator Control Using PLC with Position Based and Image Based Algorithm. Case Study.	
UNIT - V	**8 Hrs**
Programmable Digital Signal Processor Introduction, Evaluation and important features of programmable VLSI-DSP processor, application of VLSI-DSP processor in the field of Wireless Communication, Multimedia Signal Processing etc.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Analyze the process Modeling hierarchies, theoretical and empirical models.
CO2	:	Apply different Feedback & feed forward control techniques for theoretical and empirical models.
CO3	:	Comprehend the Decoupling controller, Instrumentation for process monitoring and preparation of P&I diagrams
CO4	:	Develop Statistical process control, supervisory control, direct digital control, distributed control, PC based automation.

Reference Books

1. Fu, Lee and Gonzalez , “Robotics, control vision and intelligence”. McGraw Hill International, 2007,2nd edition, ISBN: 978-0071004213.

2. John J. Craig, “Introduction to Robotics”- Addison Wesley Publishing, 2010, 3rd edition, ISBN: 978-0201543612

3. Ghosal A, "Fundamental concepts and Analysis", Oxford University Press2008, 2nd edition, ISBN: 978-0195673913

4. Sebastian Thrun, "Probabilistic Robotics", The MIT Press, 2005, 2nd edition, ISBN:978-0262201629

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Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

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3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II						
Course Code	:	MVE333C4	**Automotive Electronics**	CIE Marks	:	100
Credits L-T-P	:	3- 0 - 0		SEE Marks	:	100
Hours	:	42 L	*Elective C (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr. Usha Rani K R				

UNIT - I	**9 Hrs**
Fundamentals of Automotive: Evolution and Use of Electronics in Automotive, Automotive Systems, The Engine, Engine Control, Internal Combustion Engines, Spark Ignition Engines and Alternative Engines. Ignition System, Ignition Timing, Drivetrain, Suspensions, Brakes and Steering Systems. Basics of electronic engine control: Motivation for Electronic Engine Control, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition.	
UNIT - II	**9 Hrs**
Automotive Sensors and Actuators: Automotive Control System Applications of Sensors and Actuators, Sensors: Air Flow Sensor, Engine Crankshaft Angular Position Sensor, Throttle Angle Sensor, Temperature Sensor, Sensors for Feedback Control, Sensors for Driver Assistance System: Radar, Lidar, Video Technology. Actuators: Solenoids, Piezo Electric Force Generators, Fluid mechanical Actuators, Electric Motors and Switches.	
UNIT - III	**8 Hrs**
Digital Engine Control Systems: Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed Loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System. Vehicle Motion Control: Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS), Electronic Suspension System, Electronic Steering Control.	
UNIT - IV	**8 Hrs**
Automotive Communication Systems: Automotive networking: Bus systems, Technical principles, network topology. Buses in motor vehicles: CAN, Flex Ray, LIN, Ethernet, IP, PSI5, MOST, D2B and DSI. Automotive Embedded Software Development Fundamentals of Software and software development lifecycles. Overview of AUTOSAR methodology and principles of AUTOSAR Architecture. Introduction Internet of Vehicles, V2V.	
UNIT - V	**8 Hrs**
Diagnostics and Safety in Automotive: Timing Light, Engine Analyzer, Electronic Control System Diagnostics: Onboard diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems, Case study on ON-BOARD, OFF-BOARD diagnostics. Battery- types and maintenance, Alternators in vehicles, Starting motor systems, Electrical circuits and wiring in vehicles, vehicle network and communication buses – Digital engine control systems, Introduction to automotive controllers, On-Board Diagnostics (OBD). Introduction to electric vehicles. Experiential Learning Topics: Advances in Automotive Electronic Systems: Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Navigation: Navigation Sensors, Radio Navigation, dead reckoning navigation, Video based driver assistance systems, Night vision Systems.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Acquire the knowledge of automotive domain fundamentals, need of Electronics and communication interfaces in Automotive systems.
CO2	:	Apply various types of sensors, actuators and Motion Control techniques in Automotive systems
CO3	:	Analyze digital engine control systems and Embedded Software's and ECU's used in automotive systems.
CO4	:	Evaluate the concepts of Diagnostics, safety and advances in Automotive electronic Systems.

Reference Books

1. Bosch,"Automotive Electrics and Automotive Electronics. System and components ,Networking and Hybrid drive", Fifth edition, Springer view 2014

2. Understanding Automotive Electronics, Williams. B. Ribbens, 6th Edition, 2003, Elsevier science, Newness publication, ISBN-9780080481494.

3. NajamuzZaman , " Automotive Electronics Design Fundamental" first edition, Springer 2015.

4. Hillier's, "Fundamentals of Motor Vehicle Technology on Chassis and Body Electronics", Fifth Edition, Nelson Thrones, 2007

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EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

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Rubric for CIE & SEE Theory courses

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3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
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			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

Semester: II						
PHYSICAL DESIGN **Elective C: (Professional Elective)**						
Course Code	:	**MVE333C5**		**CIE**	:	100 Marks
Credits: L:T:P	:	3:0:0		**SEE**	:	100 Marks
Total Hours	:	42 L		**SEE Duration**	:	03 Hours

Unit-I	**10 Hrs**
Introduction Review of Combinational & Sequential Logic circuit, VLSI design Flow, Verilog/VHDL basics, CMOS circuit and layout design, CMOS logic gate design, Basic physical design of simple gates, CMOS logic structures. **Sequential Logic Synthesis** Introduction, Basics of FSM concept, Describe logic synthesis process, Explain procedure involved in logic synthesis of combinational and sequential circuits, Classify multilevel logic synthesis and technology mapping, Clocking strategies.	
Unit – II	**08 Hrs**
Floorplan Technology File, Circuit Description, Design Constraints, Design Planning, Power Planning, Macro Placement, Design of Floorplan **Placement** Global Placement, Detail Placement.	
Unit –III	**08 Hrs**
Routing Global Routing, Detail Routing, Clock tree synthesis, Power Analysis. **RC Extraction** Resistance extraction, Capacitance extraction, Inductance and impedance (RLC) extraction.	
Unit –IV	**08 Hrs**
UPF fundamentals, concepts of Logic Equivalence Check (LEC) and Design Low Power Checks (CLP). **Static Timing Analysis** Foundry Library; Liberty format, Gates: Propagation Delays, Flops: Propagation Delay, Setup time, hold Time, contamination delay, Recovery time, Removal time, Clock frequency, Jitter, Skew(source & network latency), Timing Paths, Multi-input path, Clock Budget, Multi-Clock, Multi-Cycle Path, False Path, Retiming	
Unit –V	**08 Hrs**
Physical Verification Study of CMOS Technologies, DRC and Manufacturing Issues, Basic physical design of simple gates, combinational and sequential circuits DRC, LVS, Study of Antenna Rules, Layer Density Rules, Resolution Enhancement Rules. **Design For Testing** Introduction to Digital Testing - Fault modelling, Fault Simulation, Testing for Single stuck faults, Design for Testability (DFT), Scan based designs – Compression Techniques, Built-In - Self-Test (BIST), Boundary Scan Test (IEEE 1149.1)	

Physical Design Value Added Lab:

1. Write register transfer logic level code using Verilog for combinational and sequential digital systems.
2. Analyse combinational and sequential logic circuits by simulating.
3. Write Constraints and Perform logic synthesis of Verilog logic designs.
4. Generate the synthesized netlist and analyse critical path delay, area, power, and performance of the digital system.
5. Perform Low Power checks (CLP) & Logic Equivalence Checks (LEC) using the design (RTL/Netlist)
6. Perform physical design flow: Use floorplan, placement, clock tree synthesis and routing steps.
7. Back annotation: Extract resistance, capacitance, inductance and simulate the design.

Static timing analysis checks:
Setup/Hold/Max_Transition/Max_Cap/Noise/Cross Talk/Min_Pulse_Width
Physical Verification checks: DRC/ERC/SOFT/LVS/ANTENNA/DENSITY
Design For Test: Scan Insertion, ATPG, MBIST, BSCAN implementation and verification

Course Outcomes: After completing the course, the students will be able to	
CO1:	Explain the principles of physical design, including floor planning, placement, and routing, which are essential for creating efficient and reliable integrated circuits.
CO2:	Analyse physical design problems and employ appropriate automation algorithms for partitioning, floor planning, placement, and routing.
CO3:	Perform clock tree synthesis, power optimization, and low-power design, which are essential for designing complex integrated circuits.
CO4:	Apply the various techniques used to verify the correctness of the physical design, including design rule checking (DRC), layout versus schematic (LVS) checks, and electrical rule checking (ERC) and scan chain insertion.

Reference Books	
1.	Physical Design Essentials: An ASIC Design Implementation Perspective, Khosrow Golshan, 1st Edition, Springer, ISBN-10: 44194219X, ISBN-13: 978-1441942197.
2.	Static Timing Analysis for Nanometer Designs, J. Bhashkar and Rakesh Chadha, 2009th Edition, Springer-Verlag New York Inc, ISBN-10:0387938192, ISBN-13:978-0387938196.
3.	CMOS Digital Integrated Circuits Analysis and Design, Sung-Mo Kang and Yusuf Leblebici, 41st Edition, December 2002, McGraw-Hill Higher Education, ISBN-10: 9780071243421 ISBN-13: 978-0071243421.
4.	Digital Systems Testing andTestable Design, M. Abramovici, M. A. Breuer, and A. D. Friedman, Computer Science Press, 1990, ISBN: 0-7167-8179-4.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100
QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.
TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding up to 100 Marks. Final test marks will be reduced to 40 Marks.
EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding up to 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

RUBRIC for CIE

Sl.No	Content	Marks
1	Quizzes - Q1 & Q2	20
2	Tests - T1 & T2	40
3	Experiential Learning - EL1 & EL2	40
	Total Marks	100

RUBRIC for SEE

Q. No	Contents	Marks
Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
1 & 2	Unit-1: Question 1 or 2	20
3 & 4	Unit-2: Question 3 or 4	20
5 & 6	Unit-3: Question 5 or 6	20
7 & 8	Unit-4: Question 7 or 8	20
9 & 10	Unit-5: Question 9 or 10	20
	Total Marks	100

SEMESTER: II

Course Code	:	MBT331G	**BIOINSPIRED ENGINEERING**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hr
Faculty Coordinator:			Dr Nagashree Rao and Dr Ashwani Sharma			

UNIT - I **8 Hrs**

Introduction to Bio-inspired Engineering: Macromolecules, Stem cells; types and applications. Synthetic Biology; Bottom-up' and 'top-down' engineering approaches. Synthetic/ artificial life. Biological Clock, Genetic Algorithms.

UNIT - II **9 Hrs**

Principles of bioinspired materials: Biological and synthetic materials, Self-assembly, hierarchy and evolution. Biopolymers, Bio-steel, Bio-composites, multi-functional biological materials. Thermal Properties. Antireflection and photo-thermal biomaterials, Microfluidics in biology, Invasive and non-invasive thermal detection inspired by skin

UNIT - III **9 Hrs**

Lessons from Nature:Bioinspired Materials and mechanism: Firefly-Bioluminescence, Cockleburs –Velcro, Lotus leaf - Self-cleaning materials, Gecko - Gecko tape, Whale fins - Turbine blades, Box Fish / Bone - Bionic car, Shark skin - Friction reducing swim suits, Kingfisher beak - Bullet train, Coral - Calera cement, Forest floor / Ecosystem functioning - Flooring tiles, Morpho butterfly- Structural color, Namib beetle- Water collecting, Termite mound passive cooling, Birds/Insects- flights/ aerodynamics, Mosquito inspired micro needle.

UNIT - IV **8 Hrs**

Biomedical Inspiration-Concept and applications: Organ system- Circulatory- artificial blood, artificial heart, pacemaker. Respiratory- artificial lungs. Excretory- Artificial kidney and skin. Artificial Support and replacement of human organs: artificial liver and pancreas. Total joint replacements- artificial limbs. Visual prosthesis -artificial eye/ bionic eye.

UNIT - V **8 Hrs**

Biomimetics: Inventions in nature for Human Innovation: Photosynthesis and Photovoltaic cells, Bionic/Artificial leaf. Bio-ink and 3D-Bioprinting. Cellular automata. Biosensors: Artificial tongue and nose. Biomimetic echolation. Insect foot adaptations for adhesion. Thermal insulation and storage materials. Bees and Honeycomb Structure. Artificial Intelligence, Neural Networking and bio-robotics.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Elucidate the concepts and phenomenon of natural processes
CO2	:	Apply the basic principles for design and development of bioinspired structures
CO3	:	Analyse and append the concept of bio-mimetics for diverse applications
CO4	:	Designing technical solutions by utilization of bio-inspiration modules.

Reference Books:

1. D. Floreano and C. Mattiussi, Bio-Inspired Artificial Intelligence: Theories, Methods and Technologies, 1st edition, MIT Press, 2008, ISBN: 9780262062718

2. Guang Yang, Lin Xiao, and Lallepak Lamboni. Bioinspired Materials Science and Engineering. 1st edition, John Wiley, 2018, ISBN: 978-1-119-3903362

3. M.A. Meyers and P.Y. Chen. Biological Materials, Bioinspired Materials, and Biomaterials, 1st edition, Cambridge University Press, 2014, ISBN 978-1-107-01045.

4. Tao Deng. Bioinspired Engineering of Thermal Materials, 1st edtion, Wiley-VCH Press, 2018. ISBN: 978-3-527-33834-4.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER: II

Course Code	:	MBT332G	**HEALTH INFORMATICS**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr A H Manjunatha Reddy			

UNIT - I	**8 Hrs**
Introduction, Healthcare data, information and knowledge: Data types, data conversion, clinical data warehouse, data analytics, challenges, role of informatics in analytics, future trends	
UNIT - II	**8 Hrs**
Electronic health records: Introduction, scope for the e health records, challenges, examples, logical steps to selecting and implementing EHR	
UNIT - III	**8 Hrs**
Data standards and medical coding: Introduction, medical content standards, termonology standards, transport standards, medical coding and reimbursement, future trends,	
UNIT - IV	**9 Hrs**
Healthcare Enterprise: Overview of Health Informatics: Introduction, Key players in HI, organizations involved, barriers, programs, organizations and career, HI Resources	
UNIT - V	**9 Hrs**
Health Information privacy and security: Introduction, basic security principles, authentication and identity management, data security in the cloud and client/server management	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Understand the basic principles of Health informatics.
CO2	:	Data capture to data transformation and to analysis.
CO3	:	Creation of E health records, identify the challenges.
CO4	:	Improvise the significant factors as per the spatio-temporal requirements.

Reference Books:

1. Robert E. Hoyt Ann K. Yoshihashi, Health Informatics, Practical guide for Healthcare and Information Technology Professionals, 6th edition, Informatics Education, 2014, ISBN: 978-0-9887529-2-4
2. Kathryn J. Hannah Marion J. Ball, Health Informatics, Springer Series edition, Springer, 2005, ISBN: 1-85233-826-1
3. William R Hersh, Health Informatics, a Practical guide, 8th edition. 2022, ISBN 978-1-387-85475-2
4. Pentti Nieminen. Medical informatics and data analysis 1st edition, MDPI AG, 2021, ISBN-13 : 978-3036500980

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER: II

Course Code	:	MCS331G	**BUSINESS ANALYTICS**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Azra Nasreen and Dr. Badarinath K			

UNIT - I **9 Hrs**

Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling.

UNIT - II **9 Hrs**

Trendiness and Regression Analysis Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT - III **8 Hrs**

Organization Structures of Business analytics Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, Predictive Analytics, Predicative Modelling, Predictive analytics analysis.

UNIT - IV **8 Hrs**

Forecasting Techniques Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

UNIT - V **8 Hrs**

Decision Analysis Formulating Decision Problems, Decision Strategies with and without Outcome, Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Apply the concepts and methods of business analytics to solve business problems
CO2	:	Analyse, model and solve decision problems in different settings
CO3	:	Interpret results/solutions and identify appropriate courses of action for a given business scenario
CO4	:	Demonstrate skills like investigation, effective communication, working in team/Individual and following ethical practices by implementing solutions to decision making problems

Reference Books:

1. Business analytics Principles, Concepts, and Applications FT Press Analytics, Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, 1st Edition, 2014, ISBN-13: 978-0133989403, ISBN-10: 0133989402

2. The Value of Business Analytics: Identifying the Path to Profitability, Evan Stubs , John Wiley & Sons, |DOI:10.1002/9781118983881,1st Edition 2014, ISBN:978111898388

3. Business Analytics, James Evans, Pearsons Education 2nd Edition, ISBN-13: 978-0321997821 ISBN-10: 0321997824

4. Predictive Business Analytics Forward Looking Capabilities to Improve Business, Gary Cokins and Lawrence Maisel, Wiley; 1st Edition, 2013, ISBN: 978-1-118-17556-9 .

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

SEMESTER: II

Course Code	:	MCV331G	**INDUSTRIAL AND OCCUPATIONAL HEALTH AND SAFETY**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr.V.AnanthaRam			

UNIT - I **08Hrs**

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and fire fighting, equipment and methods.

UNIT - II **09Hrs**

Occupational health and safety: Introduction, Health, Occupational health: definition, Interaction between work and health, Health hazards, workplace, economy and sustainable development, Work as a factor in health promotion. Health protection and promotion Activities in the workplace: National governments, Management, Workers, Workers' representatives and unions, Communities, Occupational health professionals. Potential health hazards: Air contaminants, Chemical hazards, Biological hazards, Physical hazards, Ergonomic hazards, Psychosocial factors, Evaluation of health hazards: Exposure measurement techniques, Interpretation of findings recommended exposure limits. Controlling hazards: Engineering controls, Work practice controls, administrative controls. Occupational diseases: Definition, Characteristics of occupational diseases, Prevention of occupational diseases.

UNIT - III **09Hrs**

Hazardous Materials characteristics and effects on health: Introduction, Chemical Agents, Organic Liquids, Gases, Metals and Metallic Compounds, Particulates and Fibers, Alkalies and Oxidizers, General Manufacturing Materials, Chemical Substitutes, Allergens, Carcinogens, Mutagens, Reproductive Hazards, Sensitizers and Teratogens, Recommended Chemical Exposure Limits. Physical Agents, Noise and Vibration, Temperature and Pressure, Carcinogenicity, Mutagenicity and Teratogenicity. Ergonomic Stresses: Stress-Related Health Incidents, Eyestrain, Repetitive Motion, Lower Back Pain, Video Display Terminals.

UNIT - IV **08 Hrs**

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT - V **08 Hrs**

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, over hauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Explain the Industrial and Occupational health and safety and its importance.
CO2	:	Demonstrate the exposure of different materials, occupational environment to which the employee can expose in the industries.
CO3	:	Characterize the different type materials, with respect to safety and health hazards of it.

SEMESTER: II

Course Code	:	MCV332G	**INTELLIGENT TRANSPORTATION SYSTEMS**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Dr.Sunil S				

UNIT - I **8 Hrs**

Introduction: –Historical Background, Definition, Future prospectus, ITS training and educational needs. Fundamentals of Traffic Flow and Control- Traffic flow elements, Traffic flow models, Shock waves in Traffic streams, Traffic signalization and control principles, Ramp metering, Traffic simulation

UNIT - II **9 Hrs**

ITS User services-User services bundles, Travel and Traffic management, Public Transportation Operations, Electronic Payment, Commercial Vehicles Operations, Emergency Management, Advanced Vehicle Control and safety systems, Information Management, Maintenance and construction Management. ITS Architecture-Regional and Project ITS
Architecture, Need of ITS architecture, concept of Operations, National ITS Architecture, Architecture development tool

UNIT - III **9 Hrs**

Technology Building Blocks for ITS-Introduction, Data acquisition, Communication Tools, Data Analysis, and Traveller Information. Various detection, identification and collection methods for ITS. ITS Applications and their benefits-Freeway and incident management systems, Advanced arterial traffic control systems, Advanced Public Transportation Systems,
Multimodal Traveller Information systems

UNIT - IV **8 Hrs**

ITS Planning-Transportation planning and ITS, Planning and the National ITS Architecture, Planning for ITS, Integrating ITS into Transportation Planning, relevant case studies. ITS Standards-Standard development process, National ITS architecture and standards, ITS standards application areas, National Transportation Communications for ITS Protocol, Standards
testing

UNIT - V **8 Hrs**

ITS Evaluation – Project selection at the planning level, Deployment Tracking, Impact Assessment, Benefits by ITS components, Evaluation Guidelines, Challenges and Opportunities. ITS for Law Enforcement: Introduction, Enhance and
support the enforcement traffic rules and regulations, ITS Funding options and ITS case studies

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Identify and apply ITS applications at different levels
CO2	:	Illustrate ITS architecture for planning process
CO3	:	Examine the significance of ITS for various levels
CO4	:	Compose the importance of ITS in implimentions

Reference Books:

1. Pradip Kumar Sarkar and Amit Kumar Jain, "Intelligent Transport Systems", PHI Learning Private Limited, Delhi,2018,ISBN-9789387472068

2. Choudury M A and Sadek A, "Fundamentals of Intelligent Transportation Systems Planning" Artech House publishers (31March 2003); ISBN-10: 1580531601

3. Bob Williams, "Intelligent transportation systems standards", Artech House, London, 2008. ISBN-13: 978-1-59693-291-3

4. Asier Perallos, Unai Hernandez-Jayo, Enrique Onieva, Ignacio Julio García Zuazola "Intelligent Transport Systems: Technologies and Applications" Wiley Publishing ©2015, ISBN:1118894782 9781118894781

SEMESTER: II

Course Code	:	MEC331G	**ELECTRONIC SYSTEM DESIGN**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Prof. Ravishankar Holla				

UNIT - I **9 Hrs**

Design Process & its Fundamentals: Life Cycle of Electronic Products, Design and Development Process, Guidance for Product Planning, Design and Development, Technical Drawings, Circuit Diagrams, Computer-Aided Design (CAD)

UNIT - II **9 Hrs**

System Architecture and Protection Requirements: Introduction - Terminology, Functions and Structures, Systems Design Architecture, Electronic System Levels, System Protection Experiential Learning: (4 quizzes on the below mentioned topics other than CIE) Reliability Analysis: Introduction, Calculation Principles, Exponential Distribution, Failure of Electronic, Components, Failure of Electronic Systems, Reliability Analysis of Electronic Systems, Recommendations for Improving Reliability of Electronic Systems

UNIT - III **8 Hrs**

Thermal Management and Cooling: Introduction - Terminology, Temperatures and Power Dissipation, Calculation Principles, Heat Transfer, Methods to Increase Heat Transfer, Application Examples in Electronic Systems, Recommendations for Thermal Management of Electronic Systems, Cooling systems, liquid, air and non cooling systems.

UNIT - IV **8 Hrs**

Electromagnetic Compatibility (EMC):
Introduction, Coupling Between System Components, Grounding Electronic Systems, Shielding from Fields, Electrostatic Discharge (ESD), Recommendations for EMC-compliant Systems Design

UNIT - V **8 Hrs**

Recycling Requirements and Design for Environmental Compliance: Introduction - Motivation and the Circular Economy, Manufacture, Use, and Disposal of Electronic Systems in the Circular Economy, Product Recycling in the Disposal Process, Material Recycling in the Disposal Process, Design and Development for Disassembly, Material Suitability in Design and Development, Recommendations for Environmentally Compliant Systems

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Realize the fundamentals of Design, Architecture, thermal management, EMC and Recycling requirements of Electronic System Design
CO2	:	Analyze the various application wise design requirements in Electronic systems along with the related concepts of implementations, standards and Compliances.
CO3	:	Use modern open source tools to realize the various concepts of Electronic system design
CO4	:	Engage in self-study through assignments, simulations, case studies and projects

Reference Books:

1. Fundamentals of Electronic Systems Design, Jens Lienig, Hans Brümmer 2017, Springer International Publishing, ISBN 978-3-319-55839-4, DOI:10.1007/978-3-319-55840-0

2. “Embedded System Design”, Marwedel, Peter, Springer Nature, 10.1007/978-3-030-60910-8

3. “Electromagnetic Compatibility Engineering”, Henry W. Ott, WILEY Publication, ISBN: 978-0-470-18930-6

4. "Handbook of Electronic Systems Design" by Charles A. Harper, McGraw-Hill Inc.,US , 0070266832, 978-0070266834

SEMESTER: II

Course Code	:	MEC332G	**EVOLUTION OF WIRELESS TECHNOLOGIES**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Mahesh A			

UNIT - I **9 Hrs**

Introduction to cellular systems: Overview of Cellular Systems and evolution 2G/3G/4G/5G, Cellular Concepts – Frequency reuse, Co-channel and Adjacent channel Interference, C/I, Handoff, Blocking, Erlang Capacity, Bluetooth, WiFi, WWAN and PAN.

UNIT - II **9 Hrs**

Fundamentals of wireless communication: Wireless Channel, Wireless propagation, Link budget, Free-space path loss, Noise figure of receiver, Multipath fading, Shadowing, Fading margin, Shadowing margin, Wireless Channel Capacity, OFDM and LTE, Large Scale Propagation effects and Channel Models

UNIT - III **8 Hrs**

Fundamentals of 5G architecture: Difference between 4G and 5G, 5G Architecture, Planning of 5G Network, Quality of Service, Radio Network, Requirements, Security, SIM in 5G Era, Specifications, Standardization, Terminal States

UNIT - IV **8 Hrs**

mmWave and Visible Light Communications: Back ground and concept of mmWave Communications, Frequency bands, propagation characteristics, channel models, applications and challenges in 5G

UNIT - V **8 Hrs**

Future Generations: Future Generations(where is the 6G?), Health Considerations, Identifiers, Interfaces, ,Key Derivation, Location Based Services, Massive Internet of Things, Measurements, Network Functions Virtualization, Network Slicing, Open Source, , User Equipment, Vehicle-to-Vehicle communications (V2V),Virtual Reality (VR/AR/XR). Case study- Bharath Stack

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Demonstrate their understanding on functioning of wireless communication system and evolution of different wireless communication systems and standards
CO2	:	Compare different technologies used for wireless communication systems.
CO3	:	Demonstrate an ability explain recent techniques for Wireless Communication systems
CO4	:	Update the latest trends in wireless communications

Reference Books:

1. Theodore S. Rappaport, “Wireless Communications: Principles and Practice”, Pearson, 2nd Edition.

2. Aditya K Jagannatham, “Principles of Modern Wireless Communications”, McGraw Hill, 2017

3. Robin Chataut, Robert Akl, “Massive MIMO Systems for 5G and beyond Networks—Overview, Recent Trends, Challenges, and Future Research Direction” Sensors, May 2020

4. A. N. Uwaechia and N. M. Mahyuddin, A Comprehensive Survey on Millimeter Wave, Communications for Fifth-Generation Wireless Networks: Feasibility and Challenges, in IEEE, Access, vol. 8, pp. 62367-62414, 2020

SEMESTER: II

Course Code	:	MIM331G	**PROJECT MANAGEMENT**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Vikram N Bahadurdesai			

UNIT - I **8 Hrs**

Introduction: Project Planning, Need of Project Planning, Project Life Cycle, Roles, Responsibility and Team Work, Project Planning Process, Work Breakdown Structure (WBS), Introduction to Agile Methodology.

UNIT - II **8 Hrs**

Capital Budgeting: Capital Investments: Importance and Difficulties, phases of capital budgeting, levels of decision making,facets of project analysis, feasibility study – a schematic diagram, objectives of capital budgeting

UNIT - III **9 Hrs**

Project Costing: Cost of Project, Means of Finance, Cost of Production, Working Capital Requirement and its Financing, Profitability Projections, Projected Cash Flow Statement, Projected Balance Sheet, Multi-year Projections, Financial Modeling, Social Cost Benefit Analysis

UNIT - IV **8 Hrs**

Tools & Techniques of Project Management: Bar (GANTT) chart, bar chart for combined activities, logic diagrams and networks, Project evaluation and review Techniques (PERT) Critical Path Method (CPM), Computerized project management

UNIT - V **9 Hrs**

Project Management and Certification: An introduction to SEI, CMMI and project management institute USA – importance of the same for the industry and practitioners. PMBOK 6 - Introduction to Agile Methodology, hemes / Epics / Stories, Implementing Agile. Domain Specific Case Studies on Project Management: Case studies covering project planning, scheduling, use of tools & techniques, performance measurement.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Explain project planning activities that accurately forecast project costs, timelines, and quality.
CO2	:	Evaluate the budget and cost analysis of project feasibility.
CO3	:	Analyze the concepts, tools and techniques for managing projects.
CO4	:	Illustrate project management practices to meet the needs of Domain specific stakeholders from multiple sectors of the economy (i.e. consulting, government, arts, media, and charity organizations).

Reference Books:

1. Prasanna Chandra, Project Planning Analysis Selection Financing Implementation & Review, Tata McGraw Hill Publication, 8th Edition, 2010, ISBN 0-07-007793-2.

2. Project Management Institute, A Guide to the Project Management Body of Knowledge (PMBOK Guide), 5th Edition, 2013, ISBN: 978-1-935589-67-9

3. Harold Kerzner, Project Management A System approach to Planning Scheduling & Controlling, John Wiley & Sons Inc., 11th Edition, 2013, ISBN 978-1-118-02227-6.

4. Rory Burke, Project Management – Planning and Controlling Techniques, John Wiley & Sons, 4th Edition, 2004, ISBN: 9812-53-121-1

SEMESTER: II

Course Code	:	MIS331G	**DATABASE AND INFORMATION SYSTEMS**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Prof.Smitha G R				

UNIT - I **8 Hrs**

Advanced Database Models, Systems, and Applications : Enhanced Data Models: Introduction to Active, Temporal, Spatial, Multimedia, and Deductive Databases . Distributed Database Concepts : Distributed Database Concepts, Data Fragmentation, Replication, and Allocation Techniques for Distributed Database Design, Overview of Concurrency Control and Recovery in Distributed Databases

UNIT - II **8 Hrs**

Introduction to Information Retrieval and Web Search : Information Retrieval (IR) Concepts Retrieval Models, Types of Queries in IR Systems , Text Preprocessing , Inverted Indexing, Evaluation Measures of Search Relevance ,Web Search and Analysis, Trends in Information Retrieval .

UNIT - III **8 Hrs**

Information Systems, Organizations and Strategy: Organizations and information systems, How information systems impact organization and business firms, Using information systems to gain competitive advantage, management issues, Ethical and Social issues in Information Systems: Understanding ethical and Social issues related to Information Systems, Ethics in an information society, The moral dimensions of information society. A Case study on business planning.

UNIT - IV **9 Hrs**

Achieving Operational Excellence and Customer Intimacy: Enterprise systems, Supply chain management(SCM) systems, Customer relationship management(CRM) systems, Enterprise application. E-commerce: Digital Markets Digital Goods: E-commerce and the internet, E-commerce-business and technology, The mobile digital platform and mobile E-commerce, Building and E-commerce web site. A Case study on ERP.

UNIT - V **9 Hrs**

Managing Knowledge:
The knowledge management landscape, Enterprise-wide knowledge management system, Knowledge work systems, Intelligent techniques. Enhancing Decision Making: Decision making and information systems, Business intelligence in the enterprise. Business intelligence constituencies. Building Information Systems: Systems as planned organizational change, Overview of systems development.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Understand the different models for Infromation Retrieval.
CO2	:	Appricieate the technology of Information Retrieval and Web Search
CO3	:	To understand the basic principles and working of information technology.
CO4	:	Describe the role of information technology and information systems in business.

Reference Books:

1. Kenneth C. Laudon and Jane P. Laudon: Management Information System, Managing the Digital Firm, Pearson Education, 14th Global edition, 2016, ISBN:9781292094007.

2. Fundamentals of Database Systems, Ramez Elmasri, Shamkant B. Navathe, 7th Edition, 2016, Published by Pearson, Copyright © , ISBN-10: 0133970779

3. James A. O' Brien, George M. Marakas: Management Information Systems, Global McGraw Hill, 10th Edition, 2011, ISBN: 978-0072823110.

4. Database Management Systems, Raghu Ramakrishnan and Johannes Gehrke, 3rd Edition, 2003, McGraw-Hill, ISBN: 9780071231510

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

SEMESTER: II						
Course Code	:	MIS331G	**DATABASE AND INFORMATION SYSTEMS**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr Mamatha G S			

UNIT - I	**8 Hrs**
Advanced Database Models, Systems, and Applications : Enhanced Data Models: Introduction to Active, Temporal, Spatial, Multimedia, and Deductive Databases . Distributed Database Concepts : Distributed Database Concepts, Data Fragmentation, Replication, and Allocation Techniques for Distributed Database Design, Overview of Concurrency Control and Recovery in Distributed Databases	
UNIT - II	**8 Hrs**
Introduction to Information Retrieval and Web Search : Information Retrieval (IR) Concepts Retrieval Models, Types of Queries in IR Systems , Text Preprocessing , Inverted Indexing, Evaluation Measures of Search Relevance ,Web Search and Analysis, Trends in Information Retrieval .	
UNIT - III	**8 Hrs**
Information Systems, Organizations and Strategy: Organizations and information systems, How information systems impact organization and business firms, Using information systems to gain competitive advantage, management issues, Ethical and Social issues in Information Systems: Understanding ethical and Social issues related to Information Systems, Ethics in an information society, The moral dimensions of information society. A Case study on business planning.	
UNIT - IV	**9 Hrs**
Achieving Operational Excellence and Customer Intimacy: Enterprise systems, Supply chain management(SCM) systems, Customer relationship management(CRM) systems, Enterprise application. E-commerce: Digital Markets Digital Goods: E-commerce and the internet, E-commerce-business and technology, The mobile digital platform and mobile E-commerce, Building and E-commerce web site. A Case study on ERP.	
UNIT - V	**9 Hrs**
Managing Knowledge: The knowledge management landscape, Enterprise-wide knowledge management system, Knowledge work systems, Intelligent techniques. Enhancing Decision Making: Decision making and information systems, Business intelligence in the enterprise. Business intelligence constituencies. Building Information Systems: Systems as planned organizational change, Overview of systems development.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Understand the different models for Infromation Retrieval.
CO2	:	Appricieate the technology of Information Retrieval and Web Search
CO3	:	To understand the basic principles and working of information technology.
CO4	:	Describe the role of information technology and information systems in business.

Reference Books:

1. Kenneth C. Laudon and Jane P. Laudon: Management Information System, Managing the Digital Firm, Pearson Education, 14th Global edition, 2016, ISBN:9781292094007.

2. Fundamentals of Database Systems, Ramez Elmasri, Shamkant B. Navathe, 7th Edition, 2016, Published by Pearson, Copyright © , ISBN-10: 0133970779

3. James A. O' Brien, George M. Marakas: Management Information Systems, Global McGraw Hill, 10th Edition, 2011, ISBN: 978-0072823110.

4. Database Management Systems, Raghu Ramakrishnan and Johannes Gehrke, 3rd Edition, 2003, McGraw-Hill, ISBN: 9780071231510

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE		
Sl.No	**Content**	**Marks**
1	Quizzes - Q1 & Q2	20
2	Tests - T1 & T2	40
3	Experiential Learning - EL1 & EL2	40
	Total Marks	100

RUBRIC for SEE		
Q. No	**Contents**	**Marks**
	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).	
1 & 2	Unit-1: Question 1 or 2	20
3 & 4	Unit-2: Question 3 or 4	20
5 & 6	Unit-3: Question 5 or 6	20
7 & 8	Unit-4: Question 7 or 8	20
9 & 10	Unit-5: Question 9 or 10	20
	Total Marks	100

SEMESTER: II						
Course Code	:	MIS332G	**MANAGEMENT INFORMATION SYSTEMS**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:		Prof. Vanishree K				

UNIT - I	**8 Hrs**
Overview: Introduction: Professional Software Development, Software Engineering Ethics, Case studies. Software Processes: Models, Process activities, Coping with Change, Process improvement. The Rational Unified Process. Computer Aided Software Engineering. Agile Software Development: Introduction to agile methods, Agile development techniques, Agile project management and scaling agile methods. Information Systems in Global Business Today: The role of information systems in business today, Perspectives on information systems, Contemporary approaches to information systems	
UNIT - II	**9 Hrs**
Requirements Engineering and System Modeling: Software Requirements: Functional and Non-functional requirements. Requirements Elicitation, Specification, Validation and Change. System Modeling: Context models, Interaction models, Structural models, Behavioural models, Model driven architecture. Information Systems, Organizations and Strategy: Organizations and information systems, How information systems impact organization and business firms, Using information systems to gain competitive advantage, management issues	
UNIT - III	**9 Hrs**
Development and Testing: Design and implementation: Object oriented design using UML, Design patterns, Implementation issues, Open-source development. Software Testing: Development testing, Test-driven development, Release testing, User testing. Securing Information Systems: System vulnerability and abuse, Business value of security and control, Establishing framework for security and control, Technology and tools for protecting information resources. A case study on cybercrime.	
UNIT - IV	**8 Hrs**
Advanced Software Engineering: Dependable systems: Dependability properties, Sociotechnical systems, dependable processes, formal methods and dependability, A15 Availability and reliability, reliability requirements, Reliability measurements E-commerce: Digital Markets Digital Goods: E-commerce and the internet, E-commerce-business and technology, A Case study on ERP.	
UNIT - V	**8 Hrs**
Software Management: Project Management: Risk Management, Managing People, Teamwork, Project Planning: Software Pricing, Plan driven development, Project Scheduling, Agile planning, Estimation Techniques, COCOMO cost modeling. Building Information Systems: Systems as planned organizational change, Overview of systems development.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Understand and apply the fundamental concepts of software engineering for information systems.
CO2	:	Develop the knowledge about software engineering for management of information systems.
CO3	:	Interpret and recommend the use information technology to solve business problems.
CO4	:	Apply a framework and process for aligning organization's IT objectives with business strategy.

Reference Books:

1. Kenneth C. Laudon and Jane P. Laudon: Management Information System, Managing the Digital Firm, Pearson Education, 14th Global edition, 2016, ISBN:9781292094007.

2. Ian Sommerville,— Software Engineering, 9th Edition, Pearson Education, 2013, ISBN: 9788131762165

3. W.S. Jawadekar: Management Information Systems, Tata McGraw Hill, 2006, ISBN: 9780070616349.

4. James A. O' Brien, George M. Marakas: Management Information Systems, Global McGraw Hill, 10th Edition, 2011, ISBN: 978-0072823110

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			***RUBRIC for SEE***		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II							
Course Code	:	MMA331G	**STATISTICAL AND OPTIMIZATION METHODS**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. PRAKASH R			

UNIT - I **9 Hrs**

Random Vectors:
Probability models of N random variables, Vector notation, Marginal probability functions, Independence of random variables and random vectors, Functions of random vectors, Expected value vector and Correlation matrix, Gaussian random vectors, Expected values of sums, Probability density function of the sum of two random variables, Moment Generating Functions (MGF), MGF of the sum of independent random variables, Characteristic function and Probability generating function.

UNIT - II **8 Hrs**

Estimation: Point estimation, Estimator and estimate, Criteria for good estimates - unbiasedness, consistency, efficiency and sufficiency, Variance of a point estimator, Methods of point estimation - Method of moments and Method of maximum likelihood, Bayesian estimation of parameters.

UNIT - III **9 Hrs**

Inferential Statistics: Principles of Statistical Inference, Formulation of the problems with examples. Test of hypothesis - Null and alternative hypothesis, Procedure for statistical testing, Type I and Type II errors: level of significance, Rejection regions and power, Standard Normal null distribution (Z-test), Z-tests for means and proportions, Duality: two-sided tests and two-sided confidence intervals, P-value, Inference about variances, Special tests of significance for large and small samples (F, Chi – square, Z, t – test).

UNIT - IV **8 Hrs**

Fuzzy Optimization:
Basic concepts of fuzzy sets - Operations on fuzzy sets, Fuzzy relation equations, Fuzzy logic control, Fuzzification, Defuzzificatiuon, Knowledge base, Decision making logic, Membership functions, Rule base.
Artificial Neural Networks: Introduction - Neuron model, Multilayer perceptions - Back propagation algorithm and its variants, Loss functions in artificial neural networks, Stochastic gradient descent method.

UNIT - V **8 Hrs**

Machine Learning Algorithms:
Data mining, Hierarchy Clustering, k-Means Clustering, Distance Metric, Data mining for Big data, Characteristics of Big data, Statistical nature of Big data, Support Vector Machines, Statistical Learning Theory, Linear Support Vector Machine, Kernel functions and Nonlinear Support Vector Machines.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Illustrate the fundamental concepts of statistics, random variables, estimation, inferential statistics, fuzzy optimization and machine learning algorithms.
CO2	:	Derive the solution by applying the acquired knowledge of random variables, estimation, inferential statistics, fuzzy optimization and machine learning algorithms to the problems of engineering applications.
CO3	:	Evaluate the solution of the problems using appropriate statistical and probability techniques to the real world problems arising in many practical situations.
CO4	:	Compile the overall knowledge of statistics, probability distributions and estimation, tests of hypothesis and optimization gained to engage in life – long learning.

Reference Books:

1. Roy D. Yates, David J. Goodman, “Probability and Stochastic Processes”, 3rd Edition, An Indian Adaptation, Wiley, 2021, ISBN: 9789354243455.

2. Douglas C. Montgomery and George C. Runger, “Applied Statistics and Probability for Engineers”, 7th Edition, John Wiley & Sons, 2019, ISBN: 9781119570615.

3. Trevor Hastie Robert Tibshirani Jerome Friedman, “The Elements of Statistical Learning - Data Mining, Inference, and Prediction”, 2nd Edition, Springer, 2009 (Reprint 2017), ISBN-10: 0387848576, ISBN-13: 9780387848570.

4. Michael Baron, “Probability and Statistics for Computer Scientists”, 2nd Edition, CRC Press, 2014, ISBN- 13: 978-1-4822-1410-9.

5. Shai Shalev-Shwartz and Shai Ben-David “Understanding Machine Learning: From Theory to Algorithms”, 1st Edition, Cambridge University Press, 2014, ISBN: 978-1-107-05713-5.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
SL No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II						
Course Code	:	MME331G	**INDUSTRY 4.0**	CIE Marks	:	100
Credits L-T-P	:	3-0-0		SEE Marks	:	100
Hours	:	42L	*Elective G (Global Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Gopalakrishna H D			

UNIT - I **8 Hrs**

Fundamentals of Industry 4.0
Introduction, Industry 4.0, RAMI 4.0 (Reference Architecture Model Industry 4.0), Servitization, Product Service-System (PSS) Industry 4.0 across the Sectors Introduction, Transportation 4.0: Multimodal Transportation Systems, Rail 4.0, Digital Transformation of Railways, Logistics 4.0 (Implications), Fundamentals of Industry 4.0, Introduction, Industry 4.0, RAMI 4.0 (Reference Architecture Model Industry 4.0), Servitization, Product Service-System (PSS)
Industry 4.0 across the Sectors
Introduction, Transportation 4.0: Multimodal Transportation Systems, Rail 4.0, Digital Transformation of Railways, Logistics 4.0 (Implications)

UNIT - II **8 Hrs**

The Concept of the IIoT: Modern Communication Protocols, Wireless Communication Technologies, Proximity Network Communication Protocols, TCP/IP, API: A Technical Perspective, Middleware Architecture.

UNIT - III **8 Hrs**

Data Analytics in Manufacturing: Introduction, Power Consumption in manufacturing, Anomaly Detection in Air Conditioning, Smart Remote Machinery Maintenance Systems with Komatsu, Quality Prediction in Steel Manufacturing.
Internet of Things and New Value Proposition, Introduction, Internet of Things Examples, IoTs Value Creation Barriers: Standards, Security and Privacy Concerns.
Advances in Robotics in the Era of Industry 4.0, Introduction, Recent Technological Components of Robots, Advanced Sensor Technologies, Artificial Intelligence, Internet of Robotic Things, Cloud Robotics.

UNIT - IV **9 Hrs**

Additive Manufacturing Technologies and Applications: Introduction, Additive Manufacturing (AM) Technologies, Stereo lithography, 3DP, Fused Deposition Modeling, Selective Laser Sintering, Laminated Object Manufacturing, Laser Engineered Net Shaping, Advantages of Additive Manufacturing, Disadvantages of Additive Manufacturing.
Advances in Virtual Factory Research and Applications, The State of Art, The Virtual Factory Software , Limitations of the Commercial Software.

UNIT - V **9 Hrs**

Augmented Reality: Definitions and application of AR, VR, MR, Limitations of AR, VR, Hardware devices and Software systems, Technical issues and challenges in AR, Industrial applications, IoT and the Need for Data Rationalization
Internet of Things (IoT), Internet of Things Vision, Internet of Things (IoT) Frameworks, Architecture of Internet of Things (IoT), Visualizing the Internet of Things (IoT), Essential Technologies of the Internet of Things (IoT), Key Technologies Involved in Internet of Things, Enablers of IoT, Collaborative Operations , Training.
Smart Factories: Introduction, Smart factories in action, Importance, Real world smart factories, The way forward.
A Roadmap: Digital Transformation, Transforming Operational Processes, Business Models, Increase Operational Efficiency, Develop New Business Models.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Understand the opportunities, challenges brought about by Industry 4.0 for benefits of organizations and individuals
CO2	:	Analyze the effectiveness of Smart Factories, Smart cities, Smart products and Smart services
CO3	:	Apply the Industrial 4.0 concepts in a manufacturing plant to improve productivity and profits
CO4	:	Evaluate the effectiveness of Cloud Computing in a networked economy

Reference Books:

1. Alasdair Gilchrist, Industry 4.0 The Industrial Internet Of Things, Apress Publisher, ISBN-13 (pbk): 978-1-4842-2046-7

2. Alp Ustundag, Emre Cevikcan, Industry 4.0: Managing The Digital Transformation, Springer, 2018 ISBN 978-3-319-57869-9.

3.Ovidiu Vermesan and Peer Friess, Designing the industry - Internet of things connecting the physical, digital and virtual worlds, Rivers Publishers, 2016 ISBN 978-87-93379-81-7

4.Christoph Jan Bartodziej, The concept Industry 4.0- An Empirical Analysis of Technologies and Applications in Production Logistics, Springer Gabler, 2017 ISBN 978-3-6581-6502-4.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: II							
Course Code	:	MVE431L	**Analog Layout Design Lab**	CIE Marks	:	50
Credits L-T-P	:	1 - 0 - 1		SEE Marks	:	50
Hours	:	28P	*(Coding / Skill Laboratory)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Arun Kumar P.Chavan			

8 Hrs

1. Design a standard cell layout of Inverter and AND gate using 45nm CMOS technology.
2. Design a standard cell layout of AOI/OAI using 45nm CMOS technology
3. Design a current mirror circuit and perform post layout simulation using 45nm CMOS technology.
4. Design a single stage differential amplifier and perform post layout simulation using 45nm CMOS technology.
5. Design a band gap reference circuit and perform post layout simulation using 45nm CMOS technology.
6. Designs a five stage single ended VCO and perform post layout simulation using 45nm CMOS technology.
7. Design a 6T Bit cell circuit and perform post layout simulation using 45nm CMOS technology.
8. Design a two stage op-amp and perform post layout simulation using 45nm CMOS technology.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Apply the knowledge in layout design concepts such as antenna effect, latch-up, Electro-Migration, IR drop and self heat.
CO2	:	Analyze the challenges in deep sub micron process using well proximity effect, LOD and Shallow trench isolation.
CO3	:	Verify chip layout design using all physical verification concepts and tools.
CO4	:	Design optimized analog circuit layouts of VCO, Memory, BGR and current mirror.

Scheme of Continuous Internal Evaluation (CIE- Laboratory) : Only LAB Course 30 + 10 + 10 = 50. The Laboratory session is held every week as per the timetable and the performance of the student is evaluated in every session. The average of marks over number of experiments conducted over the weeks is considered for 30 Marks i.e (Lab Report, Observation & Analysis). The students are encouraged to implement additional innovative experiments in the lab (10 marks). At the end of the semester a test is conducted for 10 Marks (Lab Test). This adds to 50 Marks.

Scheme of Semester End Examination (SEE- Laboratory) : Only LAB Course 40 + 10 =50. Students will be evaluated for Write-up, Experimental Setup, Experiment Conduction with Results, Analysis & Discussions for 40 Marks and Viva will be conducted for 10 Marks adding to 50 Marks.

Only LAB Courses with 50 Marks

RUBRIC FOR CIE			RUBRIC FOR SEE	
Sl.No	Content	Marks	Content	Marks
1	Write Up, Setup, Conduction Results, Analysis & Discussions	30	1. Write Up, Setup, Conduction 2. Results, Analysis & Discussions	40
2	Innovative Experiment/Concept Design & Implementation	10		
3	Laboratory Internal	10	Viva Voce	10
	Total Marks	50	Total Marks	50

SEMESTER: II						
Course Code	:	**MHS131T**	**PROFESSIONAL SKILL DEVELOPMENT- I**	CIE Marks	:	50
Credits L-T-P	:	2-0-0		SEE Marks	:	50
Hours	:	28L	*Common Course to all M.Tech Programs*	SEE Durations	:	2 Hrs
Faculty Coordinator:			Dr. C.Bindu Ashwini			

UNIT - I	4 Hrs
Communication Skills: Basics of Communication, Personal Skills & Presentation Skills – Introduction, Application, Simulation, Attitudinal Development, Self Confidence, SWOC analysis. Resume Writing: Understanding the basic essentials for a resume, Resume writing tips Guidelines for better presentation of facts. Theory and Applications.	
UNIT - II	8 Hrs
Quantitative Aptitude and Data Analysis: Number Systems, Math Vocabulary, fraction decimals, digit places etc. Simple equations – Linear equations, Elimination Method, Substitution method, Inequalities. Reasoning – a. Verbal - Blood Relation, Sense of Direction, Arithmetic & Alphabet.b. Non- Verbal reasoning - Visual Sequence, Visual analogy and classification. Analytical Reasoning - Single & Multiple comparisons, Linear Sequencing. Logical Aptitude, - Syllogism, Venn-diagram method, Three statement syllogism, Deductive and inductive reasoning. Introduction to puzzle and games organizing information, parts of an argument, common flaws, arguments and assumptions. Verbal Analogies/Aptitude – introduction to different question types – analogies, Grammar review, sentence completions, sentence corrections, antonyms/synonyms, vocabulary building etc. Reading Comprehension, Problem Solving,	
UNIT - III	6 Hrs
Interview Skills: Questions asked & how to handle them, Body language in interview, and Etiquette – Conversational and Professional, Dress code in interview, Professional attire and Grooming, Behavioral and technical interviews, Mock interviews - Mock interviews with different Panels. Practice on Stress Interviews, Technical Interviews, and General HR interviews	
UNIT - IV	5 Hrs
Interpersonal and Managerial Skills: Optimal co-existence, cultural sensitivity, gender sensitivity; capability and maturity model, decision making ability and analysis for brain storming; Group discussion(Assertiveness) and presentation skills;	
UNIT - V	5 Hrs
Motivation: Self-motivation, group motivation, Behavioral Management, Inspirational and motivational speech with conclusion. (Examples to be cited). Leadership Skills: Ethics and Integrity, Goal Setting, leadership ability.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Develop professional skill to suit the industry requirement.
CO2	:	Analyze problems using quantitative and reasoning skills
CO3	:	Develop leadership and inter personal working skills.
CO4	:	Demonstrate verbal communication skills with appropriate body language.

Reference Books:

1. The 7 Habits of Highly Effective People, Stephen R Covey Free Press, 2004 Edition, ISBN: 0743272455

2. How to win friends and influence people, Dale Carnegie General Press, 1st Edition, 2016, ISBN: 9789380914787

3. Crucial Conversation: Tools for Talking When Stakes are High, Kerry Patterson, Joseph Grenny, Ron Mcmillan 2012 Edition, McGraw-Hill Publication ISBN: 9780071772204
4. Ethnus, Aptimithra: Best Aptitude Book ,2014 Edition, Tata McGraw Hill ISBN: 9781259058738

Phase *	**Activity**
I	Test 1 is conducted after the completion of 9 hours of training programme (3 Classes). Question paper will have two parts. Part A will be Quiz for 10 Marks and Part B for 50 Marks Descriptive answers.
II	Test 2 is conducted after the completion of 18 hours of training programme (6 Classes). Question paper will have two parts. Part A will be Quiz for 10 Marks and Part B for 50 Marks Descriptive answers. Total test marks will be reduced to 30 Marks and Total Quiz marks will be 20 Marks. Final CIE would be 50 Marks
	CIE marks 20 Quiz + 30 Test = 50 Marks
Semester End Examination: SEE is conducted for 50 Marks for a duration of 2 hours.	

SEMESTER: III						
Course Code	:	MVE361T	**Algorithms for VLSI Design Automation**	CIE Marks	:	100
Credits L-T-P	:	3- 1 - 0		SEE Marks	:	100
Hours	:	42L+28T	*Professional Core - 5*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Shilpa D.R			

UNIT - I	**9 Hrs**
Architectural level design &Scheduling Algorithms:Introduction to architectural level design, A model for scheduling problems, Scheduling without and with resource constraints, Scheduling algorithms for extended sequencing models, Scheduling pipelined circuits, Resource sharing and binding.	
UNIT - II	**9 Hrs**
Data Structure and Basic Algorithms: Basic Terminology, Graph Search Algorithms, Computational Geometry Algorithms, Basic Data structures. Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms	
UNIT - III	**8 Hrs**
Floor Planning and Pin Assignment: Problem formulation, classification, Constraint based, Integer programming based, rectangular Dualization, simulated evolution floor planning algorithms. Placement: Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms	
UNIT - IV	**8 Hrs**
Global Routing: Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path-based Algorithms, Steiner tree-based Algorithms Detailed Routing: Problem formulation, Classification single Layer routing, General river routing, Single row routing	
UNIT - V	**8 Hrs**
Channel, Clock and Power Routing: Two-layer channel routing Algorithms, Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms, Introduction to compaction, shadow propagation algorithm.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Analyze each stage of VLSI design flow to develop a CAD tool for physical design.
CO2	:	Apply design knowledge to develop algorithms for VLSI design automation.
CO3	:	Evaluate the algorithms for optimizing VLSI design with respect to speed, power and area.
CO4	:	Create an optimized VLSI IC design technique using various algorithms.

Reference Books

1. Synthesis and Optimization of Digital Circuit, 1994, Giovanni De Micheli, McGraw- Hill, ISBN: 10-0070163332

2. Algorithms for VLSI Physical Design Automation, N.A. Sherwani, 2002, Kluwar Academic Publishers, ISBN: 0-7923-8393-1

3. An Introduction to VLSI Physical Design, M Sarraf Zadeh, C K Wong, 1996, McGraw Hill, ISBN:0070571945

4. Algorithms for VLSI Design Automation , S.H. Gerez, 1998, John Wiley & Sons, ISBN: 978-0-471-98489-4

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5].		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: III						
Course Code	:	MVE337D1	**VLSI Testing**	CIE Marks	:	100
Credits L-T-P	:	3- 1 - 0		SEE Marks	:	100
Hours	:	42L+28T	*Elective D (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Prof. Sujatha Hiremath			

UNIT - I	**9 Hrs**
Introduction to Testing: Role of testing VLSI circuits, VLSI trends affecting testing, Importance of testing, Testing Philosophy, yield and Reject ratio. Fault Modeling- Functional Testing, Structural Testing, Types of Fault Models, Stuck-at Faults, Bridging Faults, cross point faults, Fault Equivalence, Fault Dominance and checkpoint theorem.	
UNIT - II	**9 Hrs**
Combinational Circuit Test Generation: A Basic ATPG Algorithm, Boolean Difference, Path Sensitization Methods, Roth's D- Algorithm, PODEM. Sequential ATPG: Time Frame Expansin. Testability Measure – Controllability, Observability, and SCOAP measures for combinational and sequential circuits, Probability-based Testability Analysis.	
UNIT - III	**8 Hrs**
Fault Simulation- Fault Simulation algorithm- Serial, Parallel, Deductive and Concurrent Fault Simulation, Comparison of fault simulation. Design for Testability- Ad-hoc, Structured DFT- Scan method, Scan Design Rules, Overheads of Scan Design, partial scan methods, multiple chain scan methods.	
UNIT - IV	**8 Hrs**
Built in self-test: BIST Design rules, Test pattern generation for BIST, Output response analysis, BIST Architectures: Without scan chains, with scan chains and using Register reconfiguration. Boundary Scan Standard - TAP Controller, Test Instructions, IEEE 1149.1 standard	
UNIT - V	**8 Hrs**
Memory Testing & BIST: Introduction, RAM functional fault models & Test Algorithms, March Test. Memory BIST. Fault Diagnosis Logical Level Diagnosis, Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Apply the knowledge of testing, fault modeling & fault coverage.
CO2	:	Analysis of various fault simulation methods, different testability analysis and self testing Digital circuits.
CO3	:	Develop an algorithm for fault detection and analysis of scan design and its limitations.
CO4	:	Design of different ATPG, and knowledge about different methods of BIST and Memory BIST associated with testing.

Reference Books

1. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memoryand Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000, ISBN:0-7923-7991-8. 2

2. L. T. Wang, C. W. Wu, and X. Wen, VLSI Test Principles and Architectures, Morgan Kaufmann, 2006, ISBN-13: 978-0-12-370597-6

3. Parag.K.Lala, Digital Circuit Testing and Testability, Academic Press

4. M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing andTestable Design, Computer Science Press, 1990, ISBN: 0-7167-8179-4

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: III							
Course Code	:	MVE337D2	**High Speed Digital Design**	CIE Marks	:	100
Credits L-T-P	:	3- 1 - 0		SEE Marks	:	100
Hours	:	42L+28T	*Elective D (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Srividya P			

UNIT - I	**9 Hrs**
Introduction to high speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.	
UNIT - II	**9 Hrs**
Power distribution and Noise: Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference. Power distribution on chips, Transient Power analysis,cross talk and Ground bounce.	
UNIT - III	**8 Hrs**
Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.	
UNIT - IV	**8 Hrs**
Non Clocked & Clocked Logic styles: (i) Non clocked Logic Styles: Static CMOS structures: Static Combinatorial CMOS Logic, Pulsed Static Logic. DCVS Logic: Differential Cascode Voltage-Switched Logic, Differential Split Level Logic, Cascode Non-Threshold Logic. Non-Clocked Pass Gate Families: CMOS Pass Gate and Transmission Gate Logic, DCYS Logic with the Pass Gate, Complementary Pass Gate Logic, Swing-Restored Pass Gate Logic, Energy-Economized Pass Transistor Logic. (ii) Clocked Logic Styles: Single-Rail Domino Logic: Domino CMOS, Multiple Output Domino Logic, Compound Domino Logic, Noise Tolerant Precharge Logic. Dual-Rail Domino Structures: Differential Domino, Cross-Coupled Domino, Modified Dual-Rail Domino.	
UNIT - V	**8 Hrs**
Latching Strategies: Basic Latch Design: Storage Elements, Static and Dynamic Latches, Latch, Noise/Robust Design, Latch Implementation Latching single-ended logic: pseudo Inverter Latch, True Single Phase Clocking, Double-Edge-Triggered Flip-Flops Differential Logic: DCVS Latches, Static Ram Latches, Ratio Insensitive Differential Latch, Differential Flip-Flops	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Analyse the special requirements that are imposed on high speed digital design.
CO2	:	Analyze the characteristics of transmission lines, Power supply network and Noise sources in digital systems.
CO3	:	Apply different Clocked & non clocked digital Logics in designs
CO4	:	Evaluate the performance of various transmission lines and digital circuits.

Reference Books

1. William S. Dally & John W. Poulton, “Digital Systems Engineering”, Cambridge University Press, 1998. ISBN 0-521-59292-5.

2. Kerry Bernstein, Keith M. Carrig, Christopher M. Durham, Patrick R. Hansen, David Hogenmiller, Edward J. Nowak, Norman J. Rohrer., “High Speed CMOS Design Styles”, Kluwer Academic Publishers in 1999, ISBN 978-1-4613-7549-4.

3. Masakazu Shoji, “High Speed Digital Circuits”, Addison Wesley Publishing Company, 1996. ISBN 978-0201634839.

4. Howard Johnson & Martin Graham, "High Speed Digital Design" A Handbook of Black Magic, Prentice Hall PTR, 1993.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit [1 to 5].		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: III						
Course Code	:	MVE337D3	**RFIC Design**	CIE Marks	:	100
Credits L-T-P	:	3- 1 - 0		SEE Marks	:	100
Hours	:	42L+28T	*Elective D (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Chinmaye R			

UNIT - I	**9 Hrs**
Basic concepts in RF design - Units in RF design, Nonlinearity and Time Variance, Effects of nonlinearity – harmonic distortion, gain compression – 1 dB compression point, desensitization, blocking, cross modulation, intermodulation – third intercept point, cascaded nonlinear stages – IM spectra in a cascade. Noise in RF circuits - Representation of noise in circuits – input referred noise, Noise figure, Noise figure of cascaded stages, Noise figure of lossy circuits, Sensitivity, dynamic range – spurious free dynamic range (SFDR).	
UNIT - II	**9 Hrs**
Transceiver architectures – channel selection and band selection, Heterodyne – constant LO and constant IF downconversion, problem of image, image rejection vs channel selection, dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, issues in homodyne receivers, Image Reject – Hartley & Weaver architecture. Transmitter architectures - Direct conversion and two-step transmitters. Review of two port parameters and their significance. Nanoscale MOSFETs - Parasitic resistances (Rs, Rd, Rg), parasitic capacitances (Cgs, Cgd,), simplified and extrinsic small-signal models. High-frequency figures of merit: fT and fMAX	
UNIT - III	**8 Hrs**
Matching networks – Passive RLC circuits, impedance transformation – Quality factor, series to parallel conversion, basic matching networks- L, Pi-match networks – design example. Low noise Amplifier - Performance parameters, Problem of Input matching, CS stage with inductive load, Cascode CS stage with inductive degeneration (MOSFET circuits only), Noise figure calculation, Amplifier bandwidth extension techniques, Millimeter Wave LNAs	
UNIT - IV	**8 Hrs**
Mixer - Performance parameters, Mixer noise figures, single balanced and double balanced (active and passive) – working (MOSFET circuits only), Millimeter Wave Mixers. Oscillators - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, three point oscillators, (MOSFET circuits only), Ring oscillators.	
UNIT - V	**8 Hrs**
Phase Locked Loops - Basic concepts - Phase detector, Type I PLL, Dynamics of simple PLL, Drawbacks of simple PLL, Type II PLLs - PFD, charge pump, charge pump PLL, PFD/CP Nonidealities (concepts only) – Up and Down Skew and Width Mismatch, Charge Injection and clock feedthrough.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Investigate the functionality of a typical RF system.
CO2	:	Analyze CMOS circuits and its impact on Radio frequency and Millimeter Wave IC design.
CO3	:	Design and implement various circuit blocks for RF transceiver chain with specification.
CO4	:	Evaluate the different performance parameters used in RF design.

Reference Books

1. Behzad Razavi, "RF Microelectronics ", 2nd Edition Pearson Education, 2012, ISBN : 13:9780137134731

2.Thomas H Lee , "The Design of CMOS Radio Frequency Integrated Circuits",2nd Edition, Cambridge University Press, 2004, ISBN : 9780511817281

3. John Rogers ,CalvinPlett, "Radio Frequency Integrated Circuits Design", Artech House, 2003, ISBN : 1-58053-502-x

4. S. Voinigescu, "High-Frequency Integrated Circuits", The Cambridge RF and Microwave Engineering Series, 1st edition, 2013, ISBN : 978-0521873024

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: III							
Course Code	:	MVE337D4	**Signal Processing & ML on Microcontrollers**	CIE Marks	:	100
Credits L-T-P	:	3- 1 - 0		SEE Marks	:	100
Hours	:	42L+28T	*Elective D (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Prof. Mahendra B M			

UNIT - I	**9 Hrs**
Introduction: ARM Profiles, ARM Cortex M Family, Digital Signal Controller Vs Digital Signal Processor, CMSIS, TI Math and DSP Libraries Analog Input and Output Digital Signal Processing System, Data Representation, Stereo Codecs Input and Output, Data communication using Polling, Interrupts, DMA Practice: STM32F407 Discovery, WM5102 Codecs Programming Examples: Configuration of Codecs, Real Time Input and Output, Demonstration of Polling, Interrupts and DMA based IO. Fixed point tool box in MATLAB.	
UNIT - II	**9 Hrs**
Sampling, Reconstruction and Aliasing - Time and Frequency Domains, Fast Fourier Transform - Derivation of Radix-2 Practice: Sampling and Aliasing – Generating Sinusoids of Arbitrary Frequency, Step Response of the WM5102 Antialiasing Filter, Discrete Fourier Transform of a Sequence of Real Numbers, FFT of A Signal in Real-Time, Spectral Leakage	
UNIT - III	**8 Hrs**
Introduction: Overview of Linear Regression model and model estimations, Neural Network Model, Decision tree and Random Forests (Signal processing Perspective), Introduction to TinyML, Tensor Flow, Keras.	
UNIT - IV	**8 Hrs**
Model & Application development: ML/ DL work flow, Building and training a model, Machine Learning Tool chain, Building and training an application, Deployment on Microcontrollers.	
UNIT - V	**8 Hrs**
Tensor flow Lite for Microcontrollers: Building and training the models for applications, Optimizing Latency, Optimizing Energy Usage, Optimizing Model and Binary Size, Debugging, Privacy, Security and Deployment.	

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Identify different blocks of signal processing chain and constructs of tiny ML.
CO2	:	Evaluate the architecture of ARM CPUs to identify their suitability for realizing signal processing and ML applications.
CO3	:	Realize signal processing operations and ML applications on different architectures by making use of software libraries.
CO4	:	Design and analyze the applications to realize on embedded development boards.

Reference Books

1.Donald S Reay, Digital Signal Processing on using ARM Cortex M4, 2016, John Wiley & Sons, ISBN 978-1-118-85904-9

2. ARM-based Digital Signal Processing Lab-in-a-Box, ARM University Program, World Wide Education Program, ISBN- 10: 9780470936863

3. Technical reference manual for ARM processor cores including Cortex M, Wolfson PI Codec, Keil Products

4. Pete Warden, TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers, O'Reilly Media; 1st edition, ISBN-10 : 1492052043, ISBN-13 : 978-1492052043

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
Sl.No	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER: III						
Course Code	:	MVE337D5	**MEMS and Smart Systems**	CIE Marks	:	100
Credits L-T-P	:	3- 1 - 0		SEE Marks	:	100
Hours	:	42L+28T	*Elective D (Professional Elective)*	SEE Durations	:	3 Hrs
Faculty Coordinator:			Dr. Ramavenkateswaran N			

UNIT - I **9 Hrs**

Introduction to Micro and Smart Systems: Introduction, Microsystem vs MEMS, Smart Materials, structures and system, Integrated Microsystems, Application of Smart Materials and Microsystems. Feynman's vision, Evolution of micro-manufacturing. Multi-disciplinary aspects. Applications areas.
Commercial products.
Modelling: Scaling issues, Scaling in geometry, Scaling in rigid body dynamics, scaling in electrostatic forces, scaling in electromagnetic forces, scaling in electricity, scaling in fluid dynamics. scaling effects in the optical domain, scaling in biochemical phenomena

UNIT - II **9 Hrs**

Micro and Smart Devices and Systems: Principles Definitions and salient features of sensors, actuators, and systems. Sensors: silicon capacitive
accelerometer, piezo-resistive pressure sensor, Actuators: silicon micro-mirror arrays, magnetic micro relay, piezo-electric based inkjet print head, electro-thermal actuator. portable blood analyzer, fiber optic sensors, Electrostatic Comb drive, Microsystems at Radio frequency

UNIT - III **8 Hrs**

Materials: Introduction, Substrates and Wafers, Active substrate materials, Si as a substrate material, Si compounds, Si Piezoresistors, Gallium Arsenide, Quartz, Piezoelectric Crystals and Polymers. Micro Manufacturing and Material Processing: Silicon wafer processing, Oxidation , CVD, PVD , lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization, Silicon micromachining: surface, bulk , bonding based process flows.

UNIT - IV **8 Hrs**

Electronics Circuits for Micro and Smart Systems: Electronic Amplifiers, Signal Conditioning Circuits: Differential Amplifier, Instrumentation Amplifier, Wheatstone Bridge, Phase Locked Loop,Analog to Digital Conversion, Practical Signal Conditioning Circuits: Differential Charge Measurement, Switched Capacitor circuits, Circuits for frequency measurement shifts.

UNIT - V **8 Hrs**

Electronics, Circuits and Packaging: Micro Systems Packaging, objectives and special issues in micro system packaging, Types of Microsystem Packages ,Packaging Technologies Case study of devices Cantilevers, Pressure sensors, accelerometers, micro heater.

Course Outcomes:
After going through this course the student will be able to:

CO1	:	Describe working principles and packaging techniques in MEMS and smarts stems.
CO2	:	Analyze various sensors and actuator circuits for MEMS and smart systems.
CO3	:	Design of electronic circuits, sensor and actuators for MEMS and smart systems.
CO4	:	Evaluate the performance of electronic circuits for micro and smart systems.

Reference Books

1.MEMS & Microsystems: Design and Manufacture, Tai-Ran Tsu, Tata Mc-Graw-Hill.ISBN- 13:9780070487093

2. Micro and Smart Systems, K.J.Vinoy, G.K.Ananthasuresh, S.Gopalakrishnan, K.N.Bhat, Wiley India, ISBN: 9788126527151

3. Microsystems Design, S. D. Senturia, Kluwer Academic Publishers, Boston, USA, 2001, ISBN 0-7923-7246-8.

4. Analysis and Design Principles of MEMS Devices, Minhang Bao, Elsevier, Amsterdam, Netherlands, ISBN 0-444-51616-6.

Scheme of Continuous Internal Evaluation (CIE): 20 + 40 + 40 = 100

QUIZZES: Quizzes will be conducted in online/offline mode. Two quizzes will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). Two tests will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to 40 Marks.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. Case study-based teaching learning and Program specific requirements (15), Video based seminar/presentation/demonstration (25) adding upto 40 marks.

Scheme of Semester End Examination (SEE) for 100 marks: The question paper will have FIVE questions with internal choice from each unit. Each question will carry 20 marks. Student will have to answer one full question from each unit.

Rubric for CIE & SEE Theory courses

RUBRIC for CIE			*RUBRIC for SEE*		
SLNo	**Content**	**Marks**	**Q. No**	**Contents**	**Marks**
1	Quizzes - Q1 & Q2	20	Each unit consists of TWO questions of 20 Marks each. Answer FIVE full questions selecting ONE from each unit (1 to 5).		
2	Tests - T1 & T2	40			
3	Experiential Learning - EL1 & EL2	40	1 & 2	Unit-1: Question 1 or 2	20
	Total Marks	100	3 & 4	Unit-2: Question 3 or 4	20
			5 & 6	Unit-3: Question 5 or 6	20
			7 & 8	Unit-4: Question 7 or 8	20
			9 & 10	Unit-5: Question 9 or 10	20
				Total Marks	100

SEMESTER III							
Course Code	:	MVE461N	**INTERNSHIP**	CIE Marks	:	50
Credits L-T-P	:	0 - 0 - 6		SEE Marks	:	50
Hours/Week	:	12		SEE Durations	:	3 Hrs

Guidelines:

1. The duration of the internship shall be for a period of 6 weeks on full time basis after II semester final exams and before the commencement of III semester.
2. The student must submit letters from the industry clearly specifying his / her name and the duration of the internship on the company letter head with authorized signature.
3. Internship must be related to the field of specialization of the respective PG programme in which the student has enrolled.
4. Students undergoing internship training are advised to report their progress and submit periodic progress reports to their respective guides.
5. Students have to present the internship activities carried out to the departmental committee and only upon approval by the committee, the student can proceed to prepare and submit the hard copy of the final internship report. 6. The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be softbound in Ivory color for PG circuit
Programs and Light Blue for Non-Circuit Programs.

Course Outcomes: After going through the internship the student will be able to

CO1: Apply Engineering and Management principles to solve the problems CO2:
Analyze real-time problems and suggest alternate solutions
CO3: Communicate effectively and work in teams
CO4: Imbibe the practice of professional ethics and lifelong learning

Scheme of Continuous Internal Evaluation (CIE):

The evaluation committee shall consist of Guide, Professor, Associate Professor/Assistant Professor. The committee shall assess the presentation and the progress reports.

The evaluation criteria shall be as per the rubrics given below:

Reviews	Activity	Weightage
I	Application of Engineering knowledge in industries, ability to comprehend the functioning of the Organization/ Departments.	40%
II	Importance of Resource Management, Environment and Sustainability. Demonstration and Presentation of Internship work with Report Submission	60%

Scheme for Semester End Evaluation (SEE):

The SEE examination shall be conducted by an external examiner (domain expert) and an internal examiner. Evaluation shall be done in batches, not exceeding 6 students per batch.

SEMESTER III							
Course Code	:	MVE461P	**MINOR PROJECT**	CIE Marks	:	50
Credits L-T-P	:	0 - 0 - 6		SEE Marks	:	50
Hours/Week	:	12		SEE Durations	:	3 Hrs

Guidelines:

1. Each project group will consist of maximum of two students.
2. Each student / group has to select a contemporary topic that will use the technical knowledge of their program of study after intensive literature survey.
3. Allocation of the guides preferably in accordance with the expertise of the faculty.
4. The minor project would be performed in-house.
5. The implementation of the project must be preferably carried out using the resources available in the department/college.

Course Outcomes: After completing the course, the students will be able to

CO1: Conceptualize, design and implement solutions for specific problems.
CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply resource managements skills for projects.
CO4: Synthesize self-learning, team work and ethics.

Scheme of Continuous Internal Examination

Evaluation shall be carried out in three reviews. The evaluation committee shall consist of Guide, Professor and Associate Professor/Assistant Professor.

Phase *	Activity	Weightage
I	Approval of the selected topic, formulation of Problem Statement and Objectives with Synopsis submission	20 %
II	Mid-term seminar to review the progress of the work with documentation	40 %
III	Oral presentation, demonstration and submission of project report	40 %

* Phase wise rubrics to be prepared by the respective departments

CIE Evaluation shall be done with weightage / distribution as follows:

• Selection of the topic & formulation of Problem Statement and Objectives	10 %
• Design and simulation/ Algorithm development/ Experimental setup	25 %
• Conducting experiments/ Implementation / Testing	25 %
• Demonstration & Presentation	25 %
• Report writing	15 %

Scheme of Semester End Examination (SEE):

The evaluation will be done by ONE senior faculty from the department and ONE external faculty member from Academia / Industry / Research Organization. The following weightages would be given for the examination. Evaluation will be done in batches, not exceeding 6 students.

• Brief write up about the project 05%
• Methodology and Experimental Results & Discussion 20%
• Presentation / Demonstration of the Project 25%
• Report 20%
• Viva Voce 30%

SEMESTER IV						
Course Code	:	MVE491P	**MAJOR PROJECT**	CIE Marks	:	100
Credits L-T-P	:	0 - 0 - 18		SEE Marks	:	100
Hours/Week	:	36		SEE Durations	:	3 Hrs

Guidelines:

1. Major Project is to be carried out for a duration of 18 weeks
2. Students must adhere to the Project Presentation Schedule, report to their guide on a weekly basis and get their Project diary signed by their guide 4. Students must execute the Major Project individually and not in teams.
5. It is mandatory for the students to present/publish their project work in National/International Conferences or Journals
6. The reports shall be printed on A4 size with 1.5 spacing and Times New Roman with font size 12, outer cover of the report (wrapper) has to be soft bound and in Ivory color for PG circuit Programs and Light Blue for Non-Circuit Programs

Course Outcomes: After completing the course, the students will be able to

CO1: Conceptualize, Design and Implement solutions for specific problems. CO2: Communicate the solutions through presentations and technical reports.
CO3: Apply project and resource managements skills, professional ethics and societal concerns
CO4: Synthesize self-learning, sustainable solutions and demonstrate life-long learning

Scheme of Continuous Internal Examination

Evaluation shall be carried out in three reviews. The evaluation committee shall consist of Guide, Professor, Associate Professor/Assistant Professor.

Phase *	Activity	Weightage
I	Selection of Project Title, Formulation of Problem Statement and Objectives	20 %
II	Design, Implementation and Testing	40 %
II	Experimental Result & Analysis, Conclusions and Future Scope of Work, Report Writing and Paper Publication	40 %

* Phase wise rubrics to be prepared by the respective departments

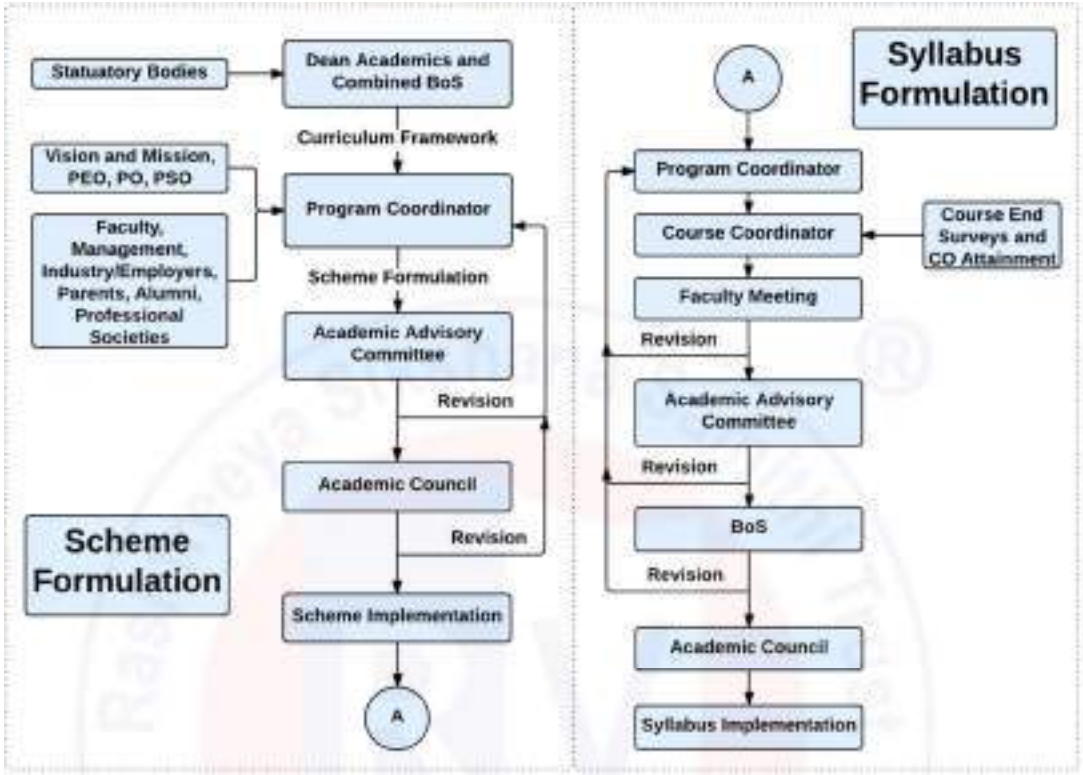
Scheme for Semester End Evaluation (SEE):

Major Project SEE evaluation shall be conducted in two stages. This is initiated after fulfilment of submission of Project Report and CIE marks.
Stage-1 Report Evaluation: Evaluation of Project Report shall be done by the Guide and an External examiner.
Stage-2 Project Viva-voce: Major Project Viva-voce examination is conducted after receipt of evaluation reports from Guide and External examiner.

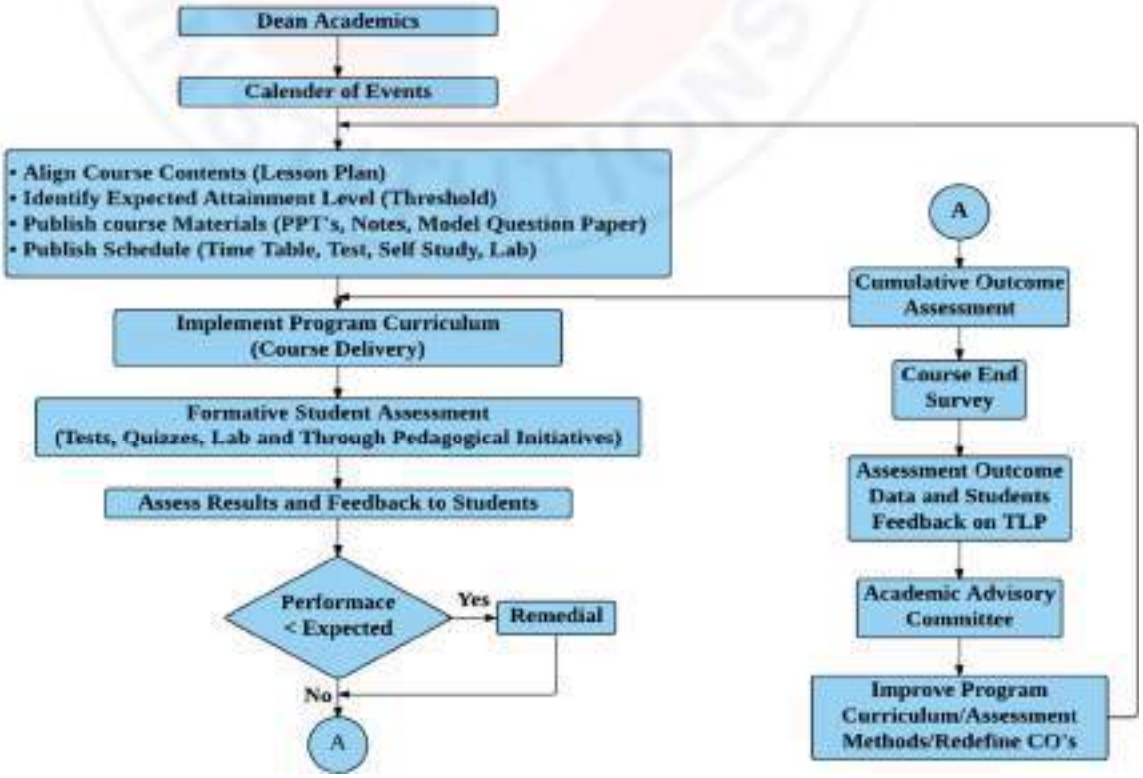
SEE procedure is as follows:

Report Evaluation	Internal Examiner: 100 Marks	**= 200**	
	External Examiner: 100 Marks	200 / 2 = **100**	**A**
Viva-Voce	Jointly evaluated by Internal Guide & External Evaluator	**= 100**	**B**
	Total Marks = (A + B) / 2 =	**100**	

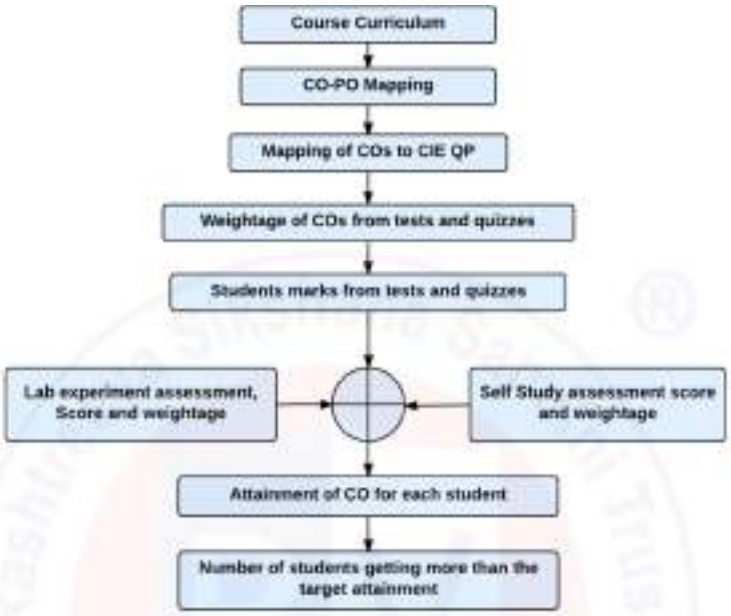
Curriculum Design Process



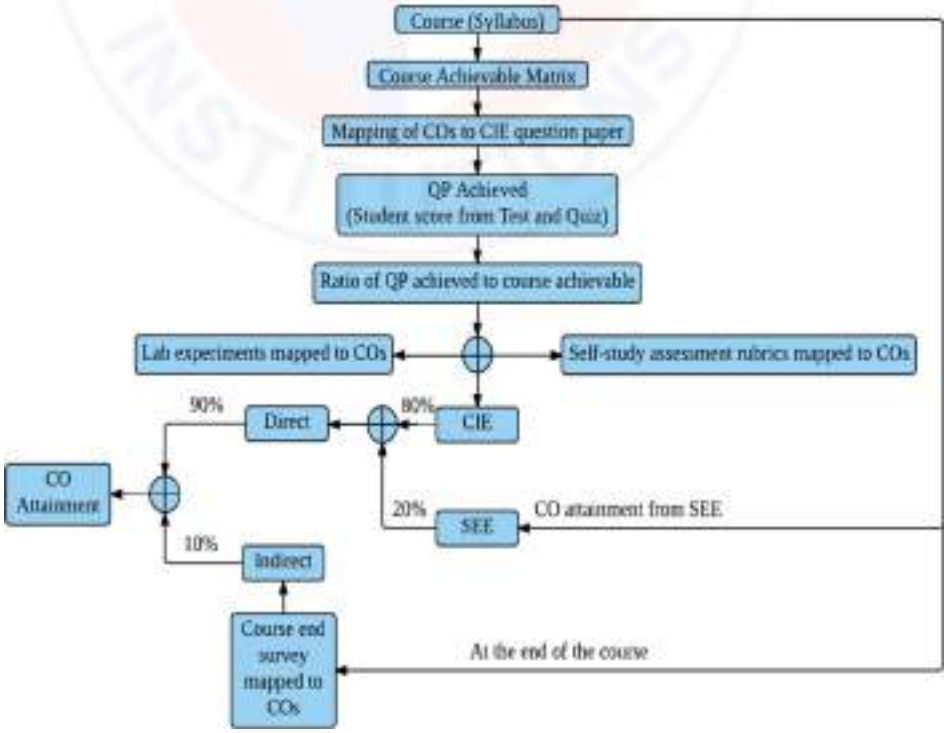
Academic Planning And Implementation



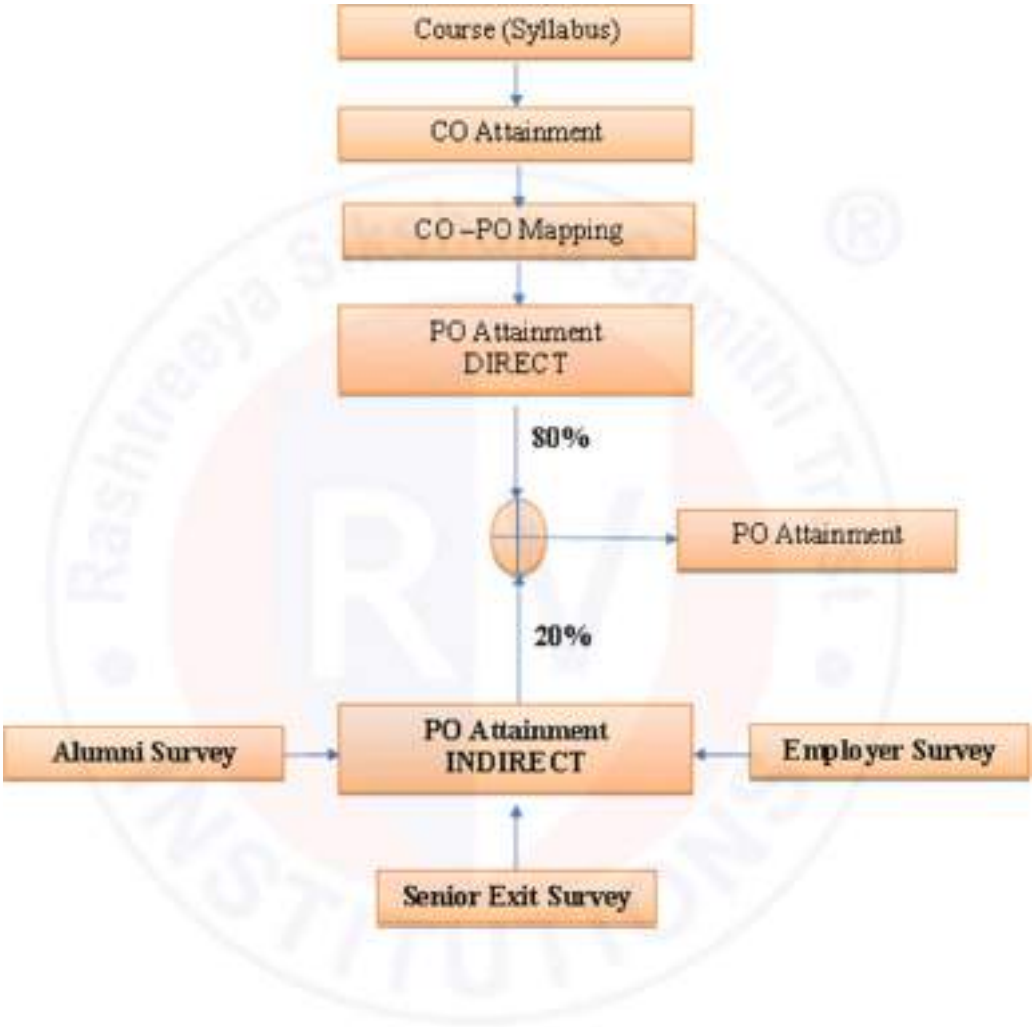
Process For Course Outcome Attainment



Final CO Attainment



Program Outcome Attainment Process



INNOVATIVE TEAMS OF RVCE

1. Ashwa Racing : Ashwa Mobility Foundation (AMF) is a student R&D platform that designs and fabricates Formula-themed race cars and future mobility solutions to tackle urban transportation problems.
2. Astra Robotics Team : Involved in the design, fabrication, and building of application-specific robots.
3. Coding Club : To facilitate students in acquiring the skills, confidence, and opportunities to change their world using coding. The club aims to help students become successful in GSoC, ACM-ICPC, and other recognized coding competitions.
4. Entrepreneurship Development Cell : E-Cell is a student-run body that aims to promote entrepreneurship by conducting workshops, speaker sessions, and discussions on business and its aspects. The organization possesses a mentor board to help startups grow.
5. Frequency Club Team : This team contributes to both software and hardware domains, mainly focusing on Artificial Intelligence, Machine Learning, and its advances.
6. Team Garuda : Design and development of a supermileage urban concept electric car. Indigenous development of E-mobility products.
7. Team Jatayu : Aims to build a low-cost Unmanned Aerial Vehicle capable of autonomous navigation, obstacle avoidance, object detection, localization, classification, and air drop of a package of optimum weight.
8. Solar Car : Aims to build a roadworthy solar electric vehicle to contribute to a green and sustainable environment.
9. Team Antariksh : A Space Technology Student Club whose goal is to understand, disseminate, and apply engineering skills for innovation in the field of Space technology, including the development of operational rockets of various altitude platforms.
10. Team Chimera : Building a Formula Electric Car through research and development in E-Mobility.Electrifying Formula Racing.
11. Helios Racing Team : Involved in the design, manufacturing, and testing of All-Terrain Vehicles and other supportive tasks for the functioning of the team. Participating in BAJA competitions organized by SAE in India and the USA.
12. Team Hydra : Developing autonomous underwater vehicles for various real-world applications such as water purification, solid waste detection and disposal, etc.
13. Team Krushi : Aims to develop low-cost equipment to help farmers in cultivating and harvesting. Uses new technology applications to reduce labor time and cost for farmers. Aims at developing implements for tractors.
14. Team Vyoma : Design, fabrication, and testing of radio-controlled aircraft and research on various types of unmanned aerial vehicles.
15. Team Dhruva : Organizing activities like quizzes based on astronomy, stargazing, and telescope handling sessions. Construction of a standard observatory and working on small projects with organizations like ICTS, IIA, ARIES, etc.
16. Ham Club : To popularize Amateur Radio as a hobby among students, alongside exploring technical innovations in the communications domain. Intended to provide human capital for service to the nation during times of natural calamities.

Cultural Activity Teams

1. AALAP (Music club)
2. DEBSOC (Debating society)
3. CARV (Dramatics club)
4. FOOTPRINTS (Dance club)
5. QUIZCORP (Quizzing society)
6. ROTARACT (Social welfare club)
7. RAAG (Youth club)
8. EVOKE (Fashion team)
9. f/6.3 (Photography club)
10. CARV ACCESS (Film-making

NSS of RVCE

NCC of RVCE

VISION

Leadership in Quality Technical Education, Interdisciplinary Research & Innovation, with a Focus on Sustainable and Inclusive Technology

MISSION

- To deliver outcome based Quality education, emphasizing on experientiallearning with the state of the art infrastructure.
- To create a conducive environment for interdisciplinary research and innovation.
- To develop professionals through holistic education focusing on individual growth, discipline, integrity, ethics and social sensitivity.
- To nurture industry-institution collaboration leading to competency enhancement and entrepreneurship.
- To focus on technologies that are sustainable and inclusive, benefiting all sections of the society.

QUALITY POLICY

Achieving Excellence in Technical Education, Research and Consulting through an Outcome Based Curriculum focusing on Continuous Improvement and Innovation by Benchmarking against the global Best Practices.

CORE VALUES

Professionalism, Commitment, Integrity, Team Work, Innovation